Chapter 2

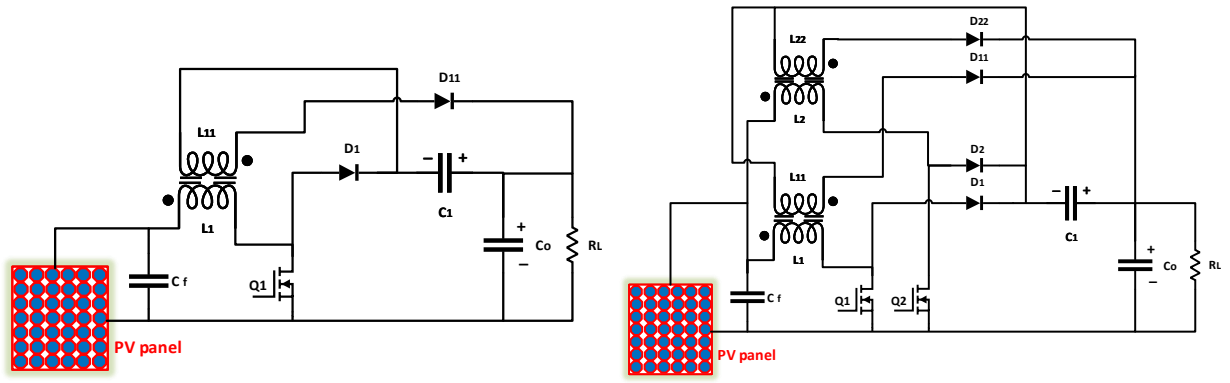
A High Gain Boost Converter for Solar Power Generation

2.1 Introduction

Electrification of the household is improving the standard of living in remote and rural areas. A highly distributed solar energy generation system can fulfill the increasing demand for electrical power [98]. The photovoltaic (PV) panels generally have low voltage and high current ratings in highly distributed solar power generation systems. Thus to address this problem, a step-up DC-DC converter is employed [99]. The conventional boost converter is generally used for the step-up operation. The major problems associated with conventional boost converters in the solar energy system are as follows:

- The voltage stress on the switch is the same as the output voltage [33].
- The high duty ratio needed to achieve high step-up gain increases the conduction loss [100].
- High voltage stress and high operating duty lead to the reverse-recovery problem in the diodes. [40]

In the past two decades, different converter topologies of high gain DC-DC converters have been proposed. These converter topologies mainly focus on reducing voltage stress and the working duty of the switch to mitigate the aforementioned drawbacks of the conventional boost converter. Moreover, a high gain DC-DC converter ensures transformerless integration of low voltage renewable resources like solar and fuel cells to the



(a) (b)

Figure 2.1: (a)-Topology of the proposed converter. (b)-Two-phase interleaved converter topology.

grid [46, 101–103]. The development of a high gain converter for the integration of the PV generation system with a DC microgrid is primary focus of this chapter.

In this chapter, an interleaved coupled inductor-based DC-DC converter is presented for solar power integration to a microgrid. The major highlights of the proposed converter are [104]:

- The components count per phase is low.
- The voltage stress across all the semiconductor devices is low, reducing the on-state losses and cost.
- The use of coupled inductor reduces the size of the system.
- Energy in the leakage inductance is utilized as well, increasing the efficiency of the converter.

The chapter has been organized as follows; The circuit description and converter's operation are explained in section II. The design of the two-phase interleaved converter is dealt with in section III. section IV presents the simulated and hardware results obtained with discussions. The presented work is concluded in Section V.

2.2 Circuit Description and Converter Operation

The proposed converter has high gain and efficiency, owing to its low device count and reduced voltage stresses across switches and diodes. The single-phase converter topology of the modified boost converter is presented in Figure 2.1a, showing the components required per phase as mentioned in Table 1.1. The two-phase topology of the proposed converter with a common capacitor is shown in Figure 2.1b. The two-phase interleaved converter consists of switches - Q_1 and Q_2, coupled inductors - $(L_1 \parallel L_{11})$ and $(L_2 \parallel L_{22})$, Diodes - D_1, D_{11}, D_2 and D_{22}. The converter has a input filter capacitor C_f, output filter capacitor C_o and a common coupling capacitor C_1. The working of the converter is described in the following six modes of operation.

2.2.1 Mode-1

In this mode both the switches Q_1 and Q_2 are in 'ON' state. Thus, Inductor L_1 in phase-1 is charging through Q_1 and Inductor L_2 in phase-2 is chanrging through Q_1. Consequently the mutual inductors L_{11} and L_{22} are charging capacitor C_1 through diodes D_{11} and D_{22}. The output capacitor C_o is discharging in the load R_L. The converter operation in mode-1 is depicted in Figure 2.2a.

2.2.2 Mode-2

The converter operation in mode-2 is depicted in Figure 2.2b. In this mode of operation, the switch Q_1 is in the 'ON' state, and Q_2 is turned 'OFF', and the current in the leakage inductance of mutual inductor L_{22} is charging the capacitor C_1. The inductor L_2 is discharging in the capacitor C_1 and C_o through diode D_2. This mode continues as long as the leakage inductance of L_{22} continues discharging its energy in C_1.

2.2.3 Mode-3

The equivalent circuit of the converter in mode-3 is shown in Figure 2.2c. The states of switches are the same as in mode-2 with Q_1 in 'ON' and Q_2 in the 'OFF' state. The mutual inductor L_{22} is fully discharged, and the diode D_{22} is blocking the flow of current through it. Inductors L_1 and L_{11} are still charging through Q_1 and D_{11}.

2.2.4 Mode-4

The mode-4 of converter operation is shown in Figure 2.2d. In this mode the switch Q_1 is turned 'OFF', thus the inductor L_1 and L_2 both are discharging in the capacitor C_1 and C_o through diode D_1 and D_2 respectively. The inductor L_{11} keeps charging the capacitor C_1 due to the leakage inductance in it. This mode continues until all the energy in the leakage inductance of L_{11} is recovered in capacitor C_1.

2.2.5 Mode-5

Figure 2.2e depicts the converter operation in mode-5. In this mode of converter operation, both the mutual inductors L_{11} and L_{22} are fully de-energized. Inductors L_1 and L_2 are discharging in the capacitors C_1 and C_o. The capacitor C_o keeps discharging in the load resistance R_1 throughout all the modes of operation.

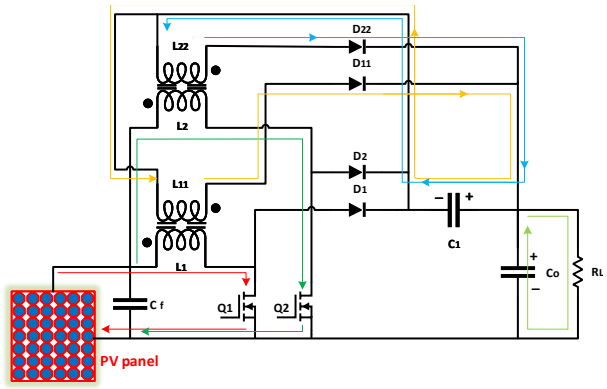
2.2.6 Mode-6

The converter operation in mode-6 is shown in Figure 2.2f. Turning the switch, Q_1 marks the starting of this mode of operation. The inductor L_2 starts charging through the switch Q_1, L_1 keeps discharging in capacitors C_1 and C_o. The increase in the current through L_2 induces a voltage in mutually coupled inductor L_{22} which turns the diode D_{22} 'ON' and C_1 starts charging.

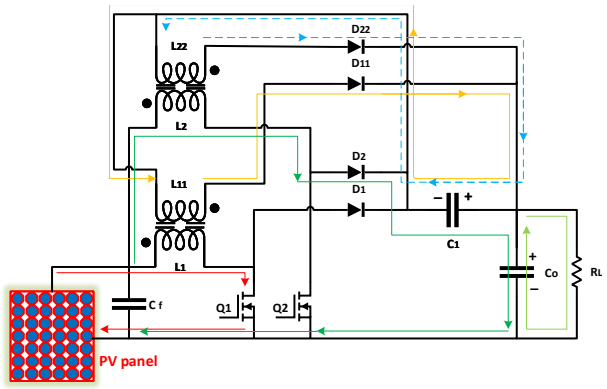
The working of the proposed interleaved modified boost converter is explained in the six modes of operations. Figure 2.3 depicts the key waveforms of the converter current and voltages during these six modes of operation for the presented two-phase interleaved converter. There are basically three stages of the converter operation per phase.

- When the switch is in the 'ON' state. For (DT_s) time period.
- when the switch is in the 'OFF' state with a non-zero current in L_{22}. For (D_1T_s) time period
- When the switch is in the 'OFF' state with zero current in L_{22}. For (D_2T_s) time period.

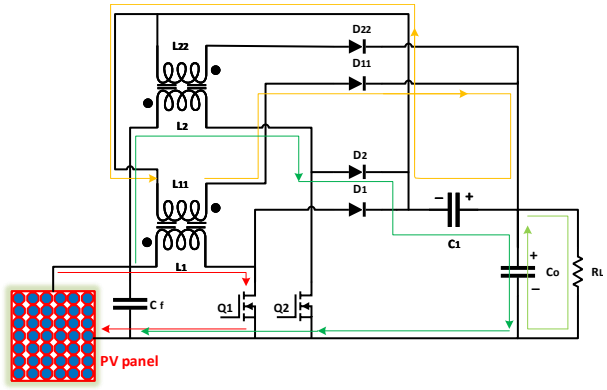
The equations representing the corresponding modes of operations of the converter at V_i input voltage and inductors L_1 and L_{11} having currents I_1 and I_{11}, capacitors C_1 and C_0



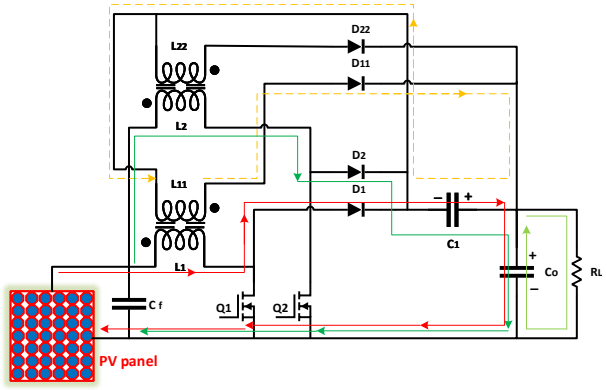
(a) Mode-1 of converter operation.



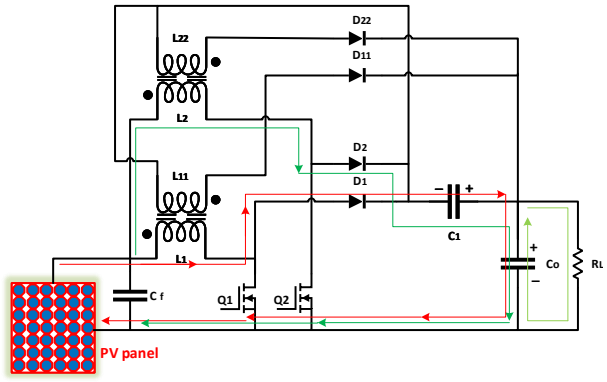
(b) Mode-2 of converter operation.



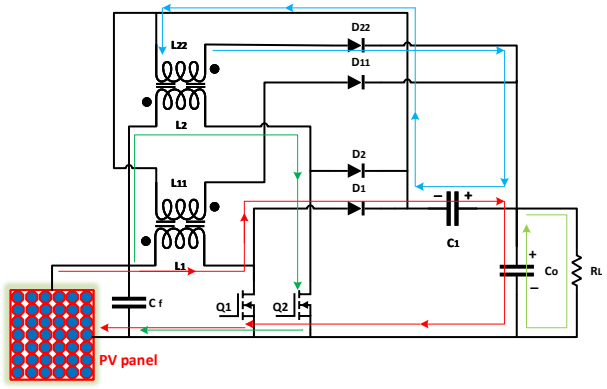
(c) Mode-3 of converter operation.



(d) Mode-4 of converter operation.



(e) Mode-5 of converter operation.



(f) Mode-6 of converter operation.

Figure 2.2: Graphical depiction of different modes of operation of the converter.

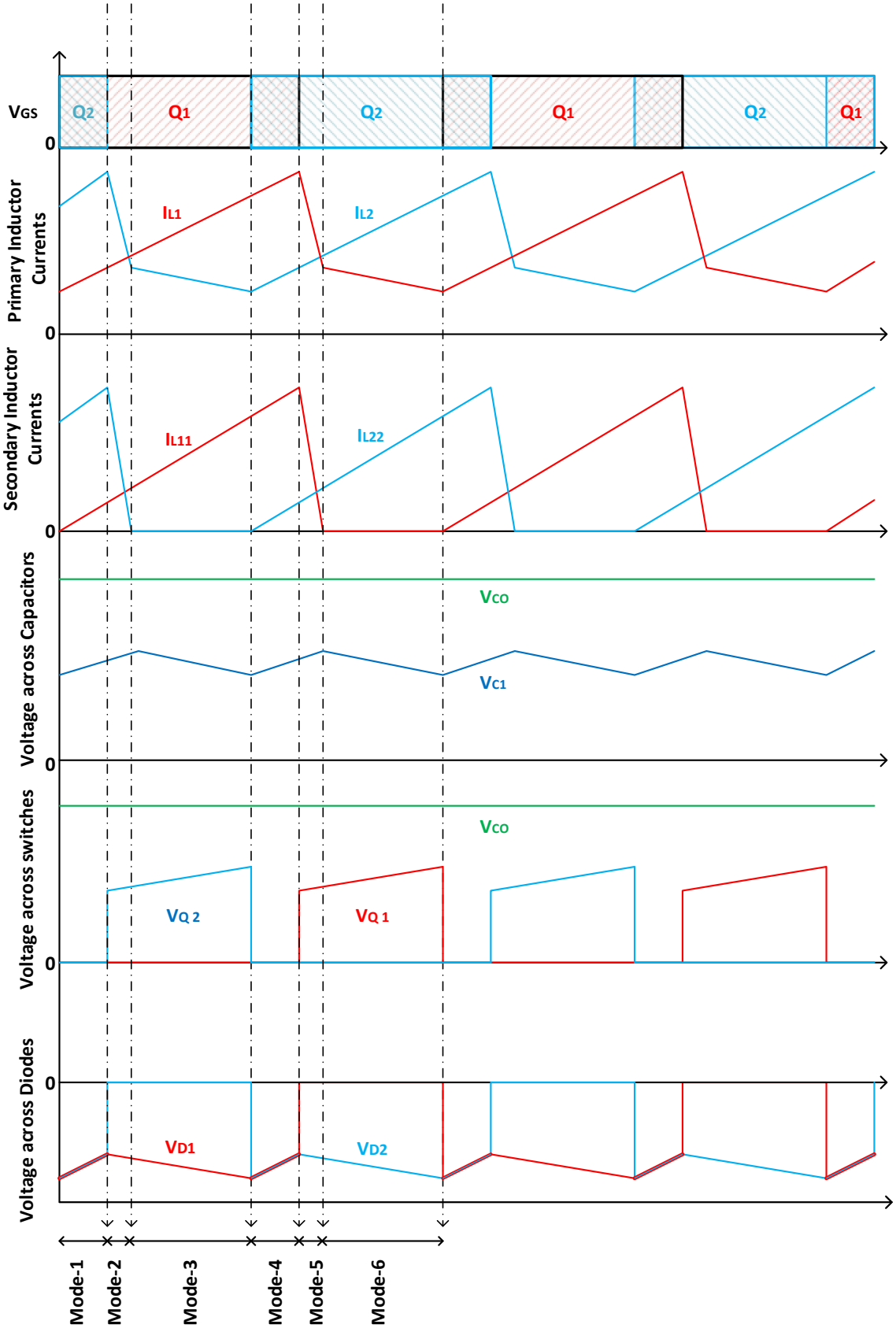


Figure 2.3: Key waveform of proposed converter.

having voltages V_c and V_o:

For DT_s:-

$$L_1\dot{I}_1 = M\dot{I}_{11} + V_i \tag{2.1}$$

$$L_{11}\dot{I}_{11} = M\dot{I}_1 - V_c \tag{2.2}$$

$$C_1\dot{V}_c = I_{11} \tag{2.3}$$

$$C_0\dot{V}_o = v_0/R \tag{2.4}$$

For D_1T_s:-

$$L_1\dot{I}_1 = M\dot{I}_{11} + V_i + V_c - V_o \tag{2.5}$$

$$L_{11}\dot{I}_{11} = M\dot{I}_1 - V_c \tag{2.6}$$

$$C_1\dot{V}_c = I_{11} - I_1 \tag{2.7}$$

$$C_0\dot{V}_o = v_0/R - I_1 \tag{2.8}$$

For D_2T_s:-

$$L_1\dot{I}_1 = M\dot{I}_{11} + V_i + V_c - V_o \tag{2.9}$$

$$L_{11}\dot{I}_{11} = 0 \tag{2.10}$$

$$C_1\dot{V}_c = -I_1 \tag{2.11}$$

$$C_0\dot{V}_o = v_0/R - I_1 \tag{2.12}$$

Assuming that the values of V_c and V_o are constant throughout the switching cycle, and the rate of change of inductor currents are different during different modes of operation. ΔI_1 and $\Delta I_1'$ are the rate of change of current in inductor L_1 during DT_s and D_1T_s respectively. ΔI_{11} and $\Delta I_{11}'$ are the rate of change of current in inductor L_{11} during DT_s and D_1T_s respectively. Then, from (1),(2),(5) & 6):

$$L_1\Delta I_1 = M\Delta I_{11} + V_iDT_s \tag{2.13}$$

$$L_{11}\Delta I_{11} = M\Delta I_1 - V_cDT_s \tag{2.14}$$

and,

$$L_1\Delta I_1' = M\Delta I_{11}' + (V_i + V_c - V_o)D_1T_s \tag{2.15}$$

$$L_{11}\Delta I_{11}' = M\Delta I_1' - V_cD_1T_s \tag{2.16}$$

Solving (13),(14),(15), and (16), the rates of change in currents are found as:

$$\Delta I_1 = \frac{[V_i - (ML_{11})V_c]DT_s}{L_1 - M^2/L_{11}} \tag{2.17}$$

$$\Delta I_1' = \frac{[V_i - V_o + (1 - M/L_{11})V_c]D_1T_s}{L_1 - M^2/L_{11}} \tag{2.18}$$

Applying charge-second balance on (2),(6) and (10),

$$M\Delta I_1 - V_cDT_s + M\Delta I_1' - V_cD_1T_s = 0$$

$$\implies V_c = \frac{M\Delta I_1 + M\Delta I_1'}{(D + D_1)T_s}$$

Solving using (17) and (18)

$$V_c = K\frac{V_i(D + D_1) - V_oD_1}{1 - KD_1 + KM(D + D_1)/L_{11}}$$

Where,

$$K = \frac{M}{(D + D_1)(L_1 - M^2/L_{11})}$$

The mutually coupled L_{11} is working in DCIM mode, thus the relation between D and D_1 is found by equating the total rise and fall of current across it.

$$D_1 = \frac{V_i - V_c(L_1/M)}{V_o - V_i - (1 - L_1/M)V_c}D$$

The expression of the output voltage is presented as a function of the working duty (D), input voltage (V_{in}), and voltage of the capacitor (C_1) as:

$$V_o = \frac{V_{in}}{D'} + V_c \tag{2.19}$$

2.3 Converter Design

The proposed converter has only one coupled inductor and one capacitor per phase, and an output filter capacitor. The methodology to calculate suitable values of these passive components is as follows:

The input voltage level is chosen as 120 V, output voltage as 300 V, output power as 900 W. It is essential to estimate the mutual inductor's coupling coefficient to calculate the value of input and mutually coupled secondary inductors. A tightly coupled inductor

is required for higher voltage gain and for reducing the switching stress on diodes and switches.

The design parameters of the converter are given in Table 2.1. The value of the coupling coefficient is chosen to be (k=0.8), solving (13) and (14) for ΔI_{11}, the following relation is found:

$$(\frac{M}{k^2} - M)\Delta I_{11} = V_i DT_s - V_c DT_s \frac{L_1}{M} \tag{2.20}$$

$$(L_1 \frac{dI_1}{dt} - V_i) = (V_i - \frac{L_1}{M} V_c) \frac{k^2}{1 - k^2} \tag{2.21}$$

since $M = k\sqrt{L_1 L_2}$ and N = $\sqrt{L_2/L_1}$

$$L_1 = \frac{k^2}{1 - k^2}(\frac{V_i}{k^2} - \frac{V_c}{Nk}) \frac{DT_s}{\Delta I_1} \tag{2.22}$$

Taking a 6 A current ripple at fully loaded condition and input voltage(V_i)= 120 V, value of k= 0.8, working frequency of 40 kHz, and turn ratio(N) of 1.4. At working duty of 50 % (D=0.5), and value of V_c= $k^2 N D V_i$= 53.76 V. The input inductor L_1 is calculated to be 580 µH.

The value of the input inductor is chosen to be ≈ 600 µH in order to keep the input inductor in CICM. Thus, depending on the turn ratio (N) of 1.4, the value of the secondary inductor is selected to be ≈ 1.2 mH.

The value of the intermediate capacitor C_1 is calculated so that it maintains a constant voltage throughout each switching cycle. The value of the output capacitor (C_o=100 µF) is calculated to have a voltage ripple of less than 2 percent at fully loaded condition. In the Mode-1 (From t=0 to t=DT_s), the total current is provided to the capacitor C_1 by the secondary inductor L_{11} thus,

$$C_1 \frac{\Delta V}{DT_s} = I_{11} \tag{2.23}$$

The Secondary Inductor is working in the DCIM mode thus, The total current provided in time period DT_S is half of total change in the current.

$$I_{11} = 0.5\Delta I_{11}$$

Table 2.1: DESIGN PARAMETERS

Parameter	Value
Input voltage	120 V
Output voltage	300 V
Power	900 W
Switching frequency	40 kHz
coupling coefficient	0.8

Table 2.2: REACTIVE COMPONENTS

Component	Value
Input inductor (L_1)	600 µH
Coupled inductor(L_{11})	1200 µH
intermediate capacitor (C_1)	22 µF
Output filter capacitor	100 µF

using (14), it can be written as:

$$L_{11}\Delta I_{11} = (M\frac{\Delta I_{11}}{DT_s} - V_c)DT_s$$
$$\implies \Delta I_{11} = \frac{NV_i - V_c}{L_{11}}DT_s$$

using (23), the value of C_1 can be calculated as follows:

$$C_1 = \frac{0.5(NV_i - V_c)}{L_{11}\Delta V f^2}D^2 \tag{2.24}$$

Taking the voltage ripple of 1 V and value of V_c at 53.76 V. The value of the capacitor C_1 is calculated to be 14.87 µF, a higher available value of 22 µF is chosen. The output capacitor is chosen as 100 µF to have minimum ripple content in the output voltage.

In the developed laboratory prototype, the selected values of reactive components are given in Table 2.2. The device specification is collated in Table 2.3

Table 2.3: DEVICE SPECIFICATIONS

component	Number	specification
MOSFETs	2	IRF200B211
Diodes	4	IDP15E65D2XKSA1
Gate driver	2	FOD3184
Capacitor(C_1)	1	UVR2D220MPD1TD
Capacitor(C_o)	1	MCKSK400M101K32S
Core	2	5943003801
PV emulator	1	ETS600X8D-PVF

2.4 Results and Discussion

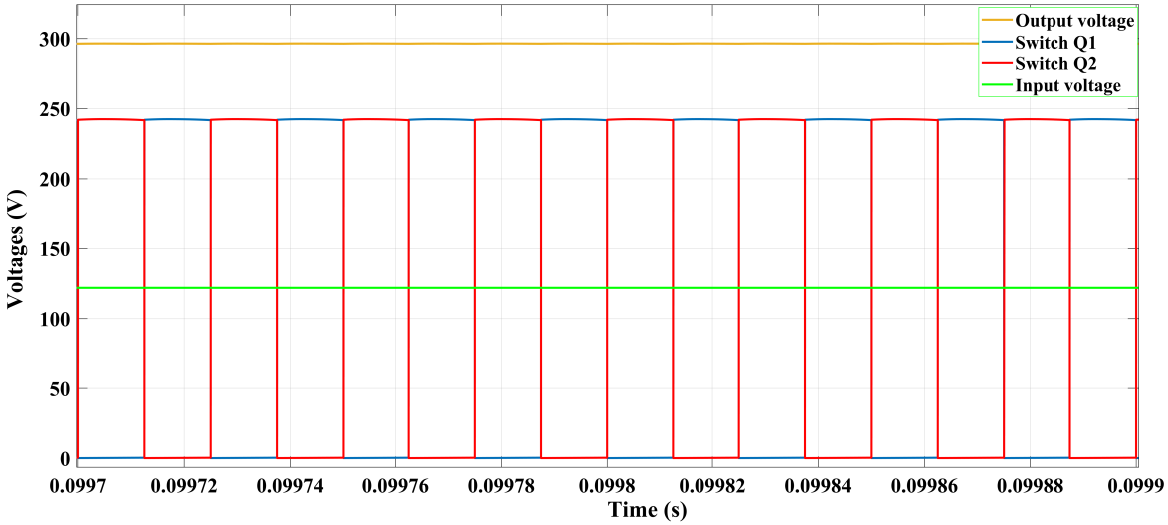


Figure 2.4: Simulated results showing the voltage stresses across switches and output voltage at 120 V input voltage and 50 % duty cycle.

To validate the working of the proposed converter under different input voltage and duty cycles, a Simulink/Matlab model of the converter is developed using the calculated parameters given in Table 2.2. A hardware prototype of the converter is developed and tested under varying conditions. The results obtained from the simulations and the hardware prototype tested in the laboratory are comparable and thus, verify the working principle and theory.

Figure 2.4 shows the simulated results of the converter at input voltage of 120 V and

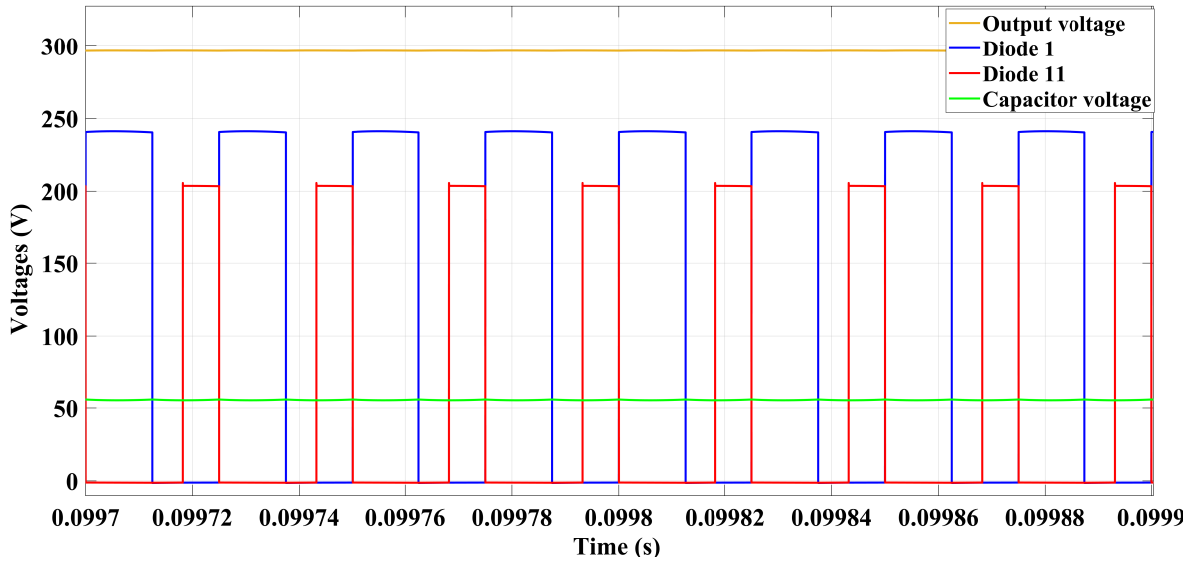


Figure 2.5: Simulated voltage stress of diodes D_1 and D_{11} with voltage across capacitor C_1 and C_o at 120 V input voltage and 50 % duty cycle.

50 % duty cycle. The output voltage and capacitor voltage obtained are 300 V and 55 V respectively. Tightening the coupling (k) of the inductors and increasing the turn ratio (N) increases the output voltage as well as the capacitor voltage. In this work, a turn ratio of 1.4 and a coupling coefficient of 0.8 are used.

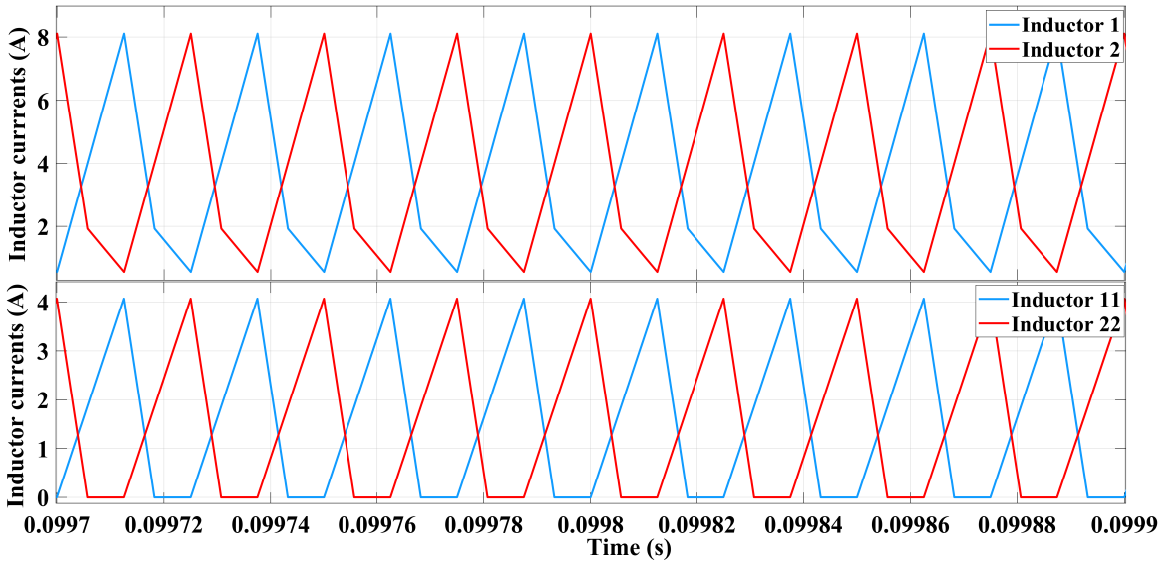


Figure 2.6: Simulated inductor currents of both the phases.

The voltage stress on the switches is shown in Figure 2.4 and voltage stress on diodes is shown in Figure 2.5 unlike conventional boost converter, the voltage stress is reduced to output voltage - capacitor voltage ($V_o - V_c$). Thus switches with lower voltage ratings

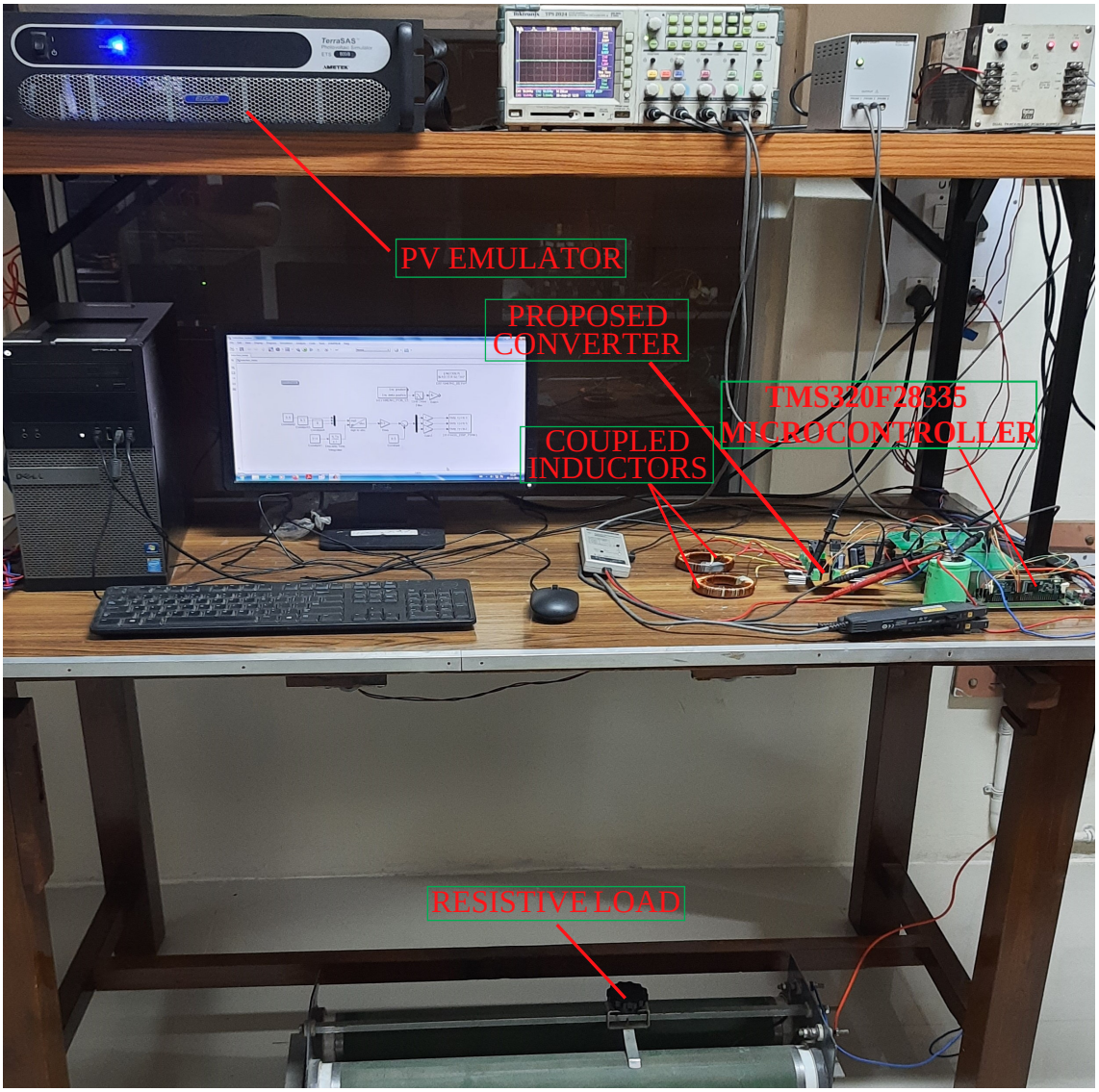


Figure 2.7: Experimental setup.

having lower on-resistance can be used in this converter, which increases the conversion efficiency.

The simulated inductor currents are presented in Figure 2.6. For efficient working of the proposed converter, it is desired that the input current is continuous while the coupled inductor works in discontinuous inductor current mode. Using interleaved converter decreases the high current ripple in the input current. In this work, a feasibility study with a two-phase interleaved converter is done. Increasing the phases will further decrease the current ripple.

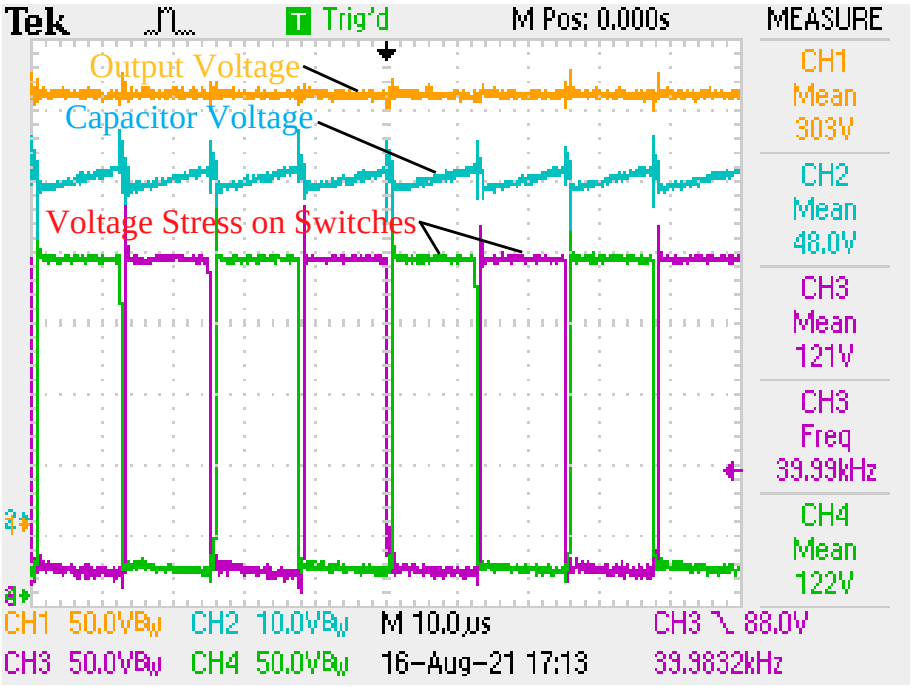


Figure 2.8: Voltage stresses across switches.

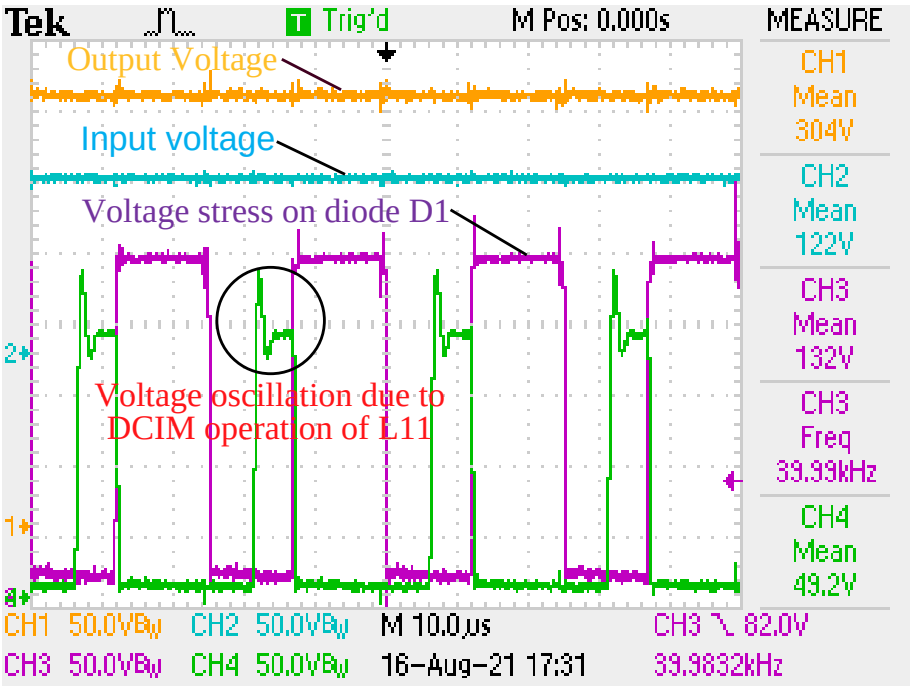


Figure 2.9: Voltage stresses across diodes.

The laboratory setup for testing the converter is shown in Figure 2.7. Figure 2.8 shows the converter characteristics obtained from the laboratory prototype of the developed converter. The input voltage is 120 V and working duty is at 50 %. The results obtained in Figure 2.4 are verified by these results obtained from the prototype. A small

error of less than 5 V in the output voltage is observed due to core saturation and an inaccurate switching model.

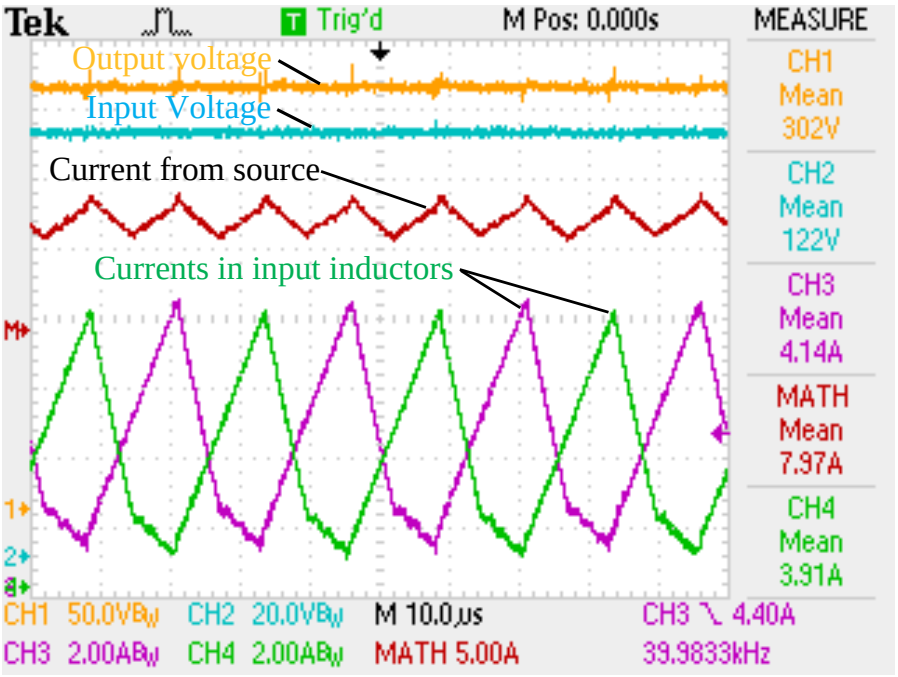


Figure 2.10: Output voltage (channel-1), input voltage (channel-2), current in L_1 (channel-3), current in L_2 (channel-4), input current (channel-MATH).

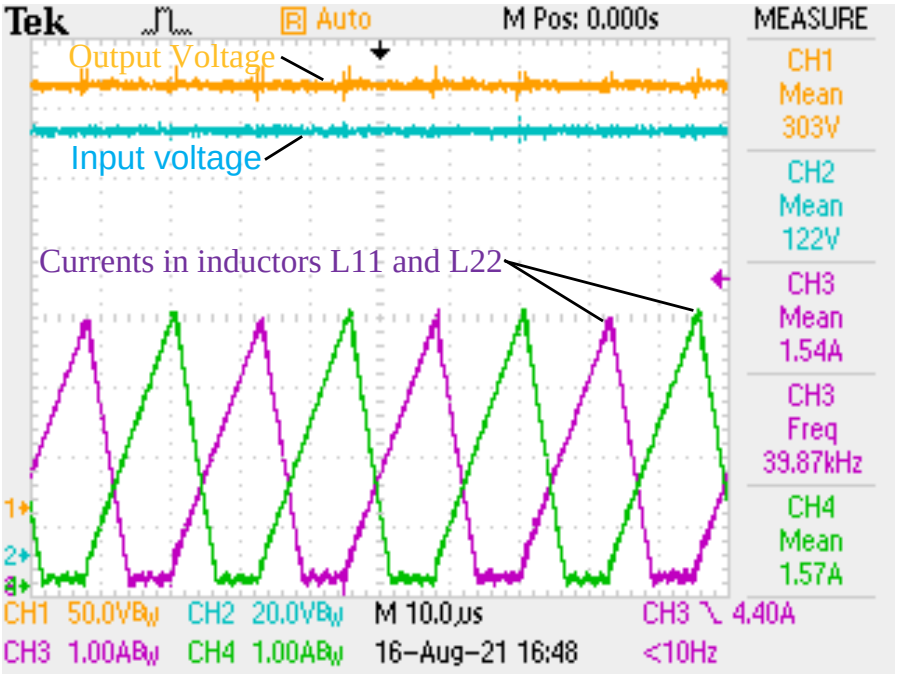


Figure 2.11: Output voltage, input voltage, and current in coupled inductors.

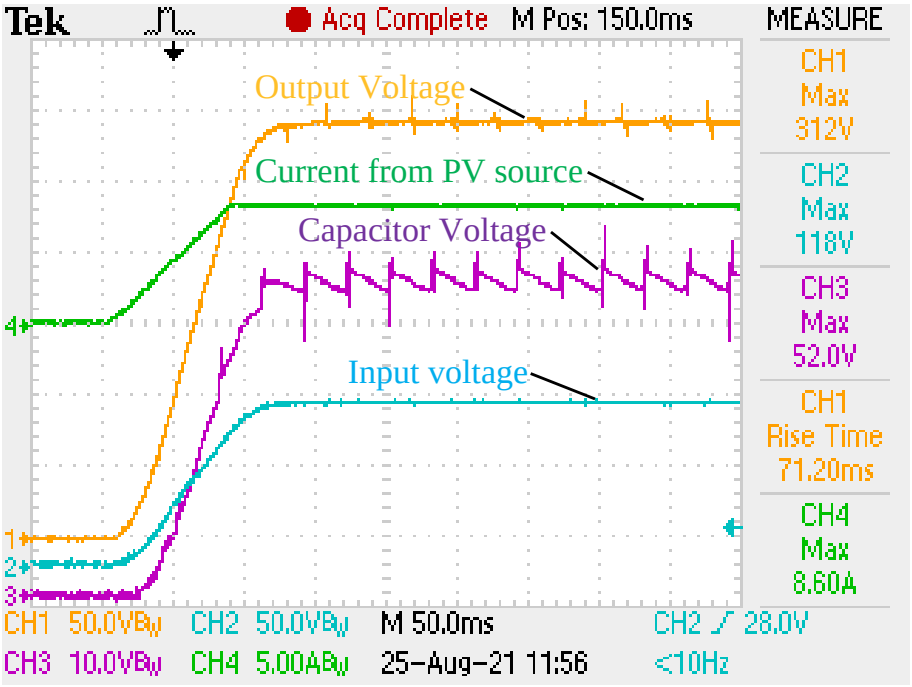


Figure 2.12: Maximum power point tracking (INC MPPT) –output voltage (channel-1), input voltage (channel-2), voltage across C_1 (channel-3), input current (channel-4).

A reduction in voltage stresses across the switches and diodes is verified by the hardware results presented in Figure 2.8 & 2.9. These results show that the value of the voltage stress on switches and diodes is significantly less than the output voltage. This reduction in the voltage stress is due to the voltage developed on the intermediate capacitor (C_1).

The inductor currents in L_1 and L_2 are shown in Figure 2.10. The input inductor in in CICM, while the coupled inductor is in DICM as desired. The voltage stress shown in this figure is representing the state of the switches("ON"/"OFF") as well and thus, this result validates working principle of the converter as explained in section II.

The voltage stress on the diodes D_1 & D_{11} are shown in Figure 2.9. The results are captured at the same input and control state of the converter. It is observed that the voltage stress on the diodes are reduced significantly as expected from discussion in section II and simulation results shown in Figure 2.5.

To validate the simultion results shown in Figure 2.6, the developed prototype is tested under the same conditions as in the simulation with input voltage of 120 V and duty cycle of 50 %. The obtained result is in accordance with the simulations and is shown in Figure 2.10 & 2.11.

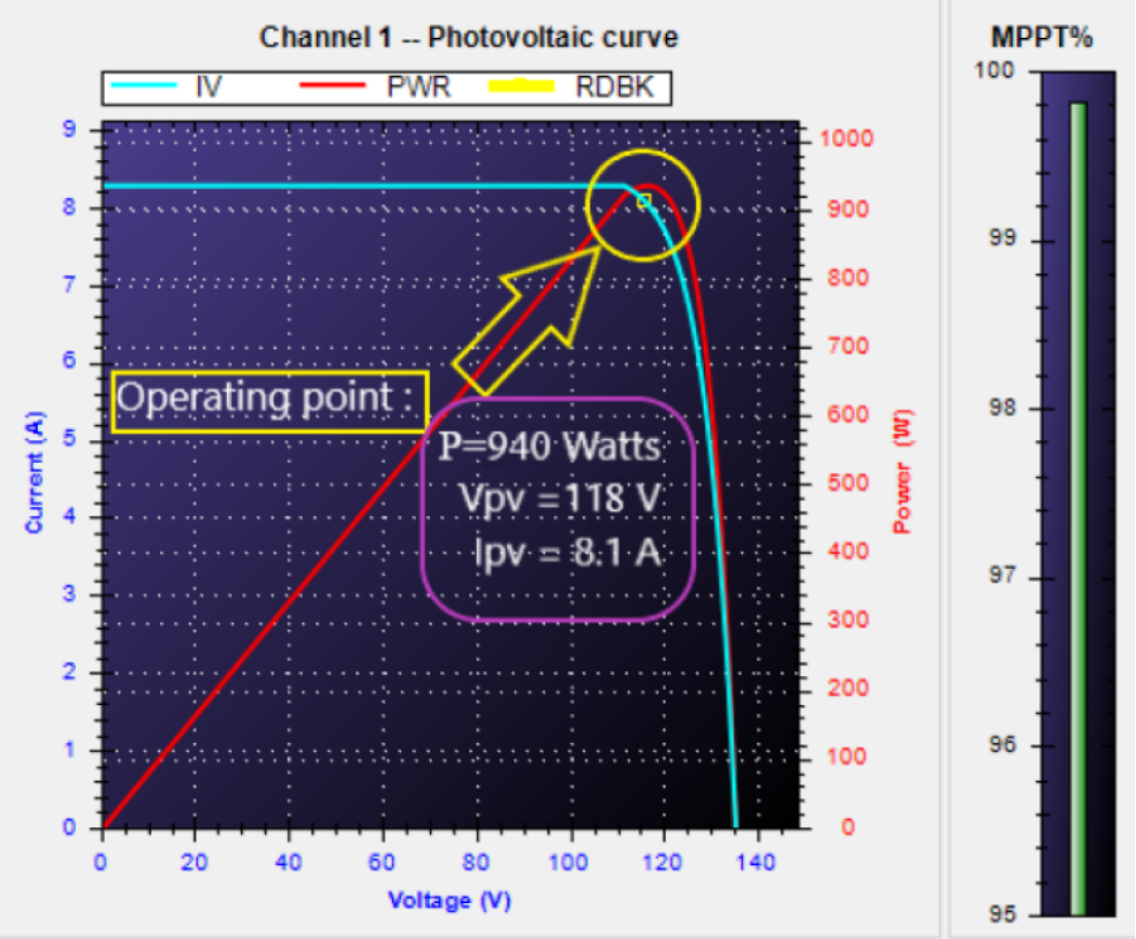


Figure 2.13: MPPT performance of the proposed system.

The converter operation with a solar PV panel is shown in Figure 2.12, Incremental conductance MPPT technique is used with the developed converter, and dynamics of the convergence to the maximum power point are captured and shown. The converter is connected to the solar panel supply abruptly to depict a sudden change in the irradiance. The solar panel characteristics are emulated for V_{OC}=135 V and I_{SC}= 8.5 A. The input voltage, output voltage, capacitor voltage, and input current are shown in this figure. The performance of the employed MPPT is shown in Figure 2.13. The operating point of the developed system is found to be within 99.8 % of the maximum power point.

The developed prototype is tested with varying input voltage from 70 V to 120 V and output power from 400 W to 900 W, the measured efficiency of converter is presented in Figure 2.14. With an increment in the input voltage, the capacitor voltage increases resulting in lower voltage stress across the switches, thus resulting in higher conversion efficiency.

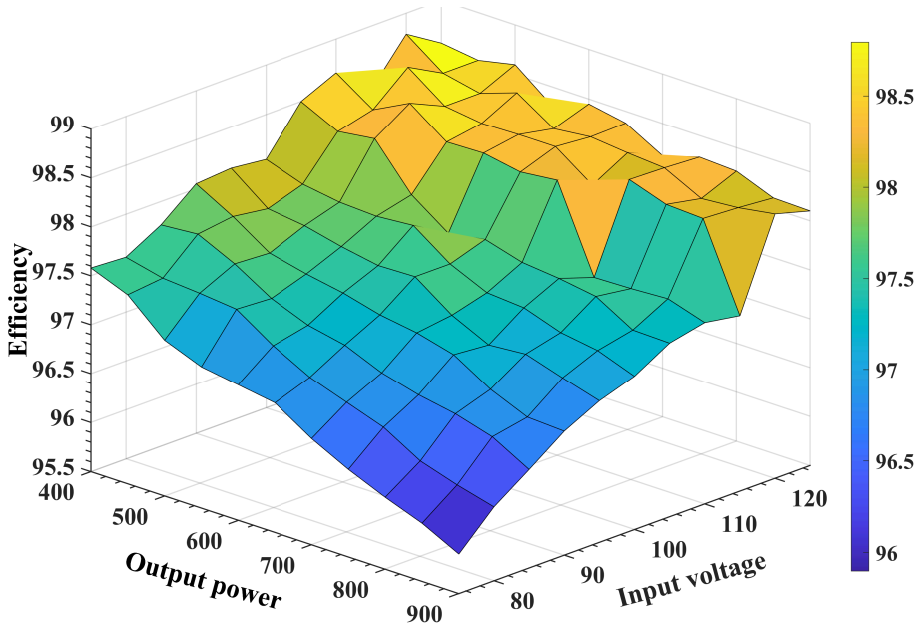


Figure 2.14: Converter efficiency at different input voltage and output power.

2.5 Summary

A modified boost two-phase interleaved converter is simulated in Matlab/Simulink and results are compared with the hardware results obtained from a laboratory-developed 900 W converter prototype. The common clamped capacitor and coupled inductors reduce the converter's size, cost, and losses. A high gain with low voltage stress is achieved, thus validating the proposed converter's suitability for integrating PV generation into a DC microgrid. At output voltage of 300 V and turn ratio (N) of the coupled inductor at 1.4, the maximum voltage stress on switches and diode D_1 is found to be 240 V, and on $D_1$1 less than 200 V. The voltage stress can be further reduced by using a high value of N and a higher coupling coefficient in the inductors. Conversion efficiency is found to be increasing with an increment in input voltage and decrement in output power. It is observed from the efficiency curve that a minimum efficiency of 95 % is achieved at 70 V and output power of 900 W, and 98 % efficiency is achieved at maximum loading of converter at 120 V and output power of 400 W.

A new converter is presented in the next chapter, which eliminates the input current-ripple, and further increase the voltage gain.