Chapter 3

Modelling and Analysis of Wide Operating Range Transformerless Interleaved Hybrid Converter

3.1 Introduction

In chapter 2, topology development and operation of transformerless minimum phase hybrid converter (TLMPHC) and transformerless interleaved hybrid converter (TLIHC) has been presented. The operational behaviour of both TLIHC and TLMPHC along with their experimental verifications have been explained in chapter 2. Moreover, a comparison between the TLIHC and TLMPHC in terms of various features such as leakage current minimization, wide operating range operation, inherent shoot-through capability and input current stresses have been discussed in chapter 2. This chapter presents the verification and analysis of all the key features of both the proposed hybrid converters TLMPHC and TLIHC during the steady-state conditions. The mathematical modelling and small signal analysis of both TLMPHC and TLIHC are discussed in this chapter. To check the performance of TLMPHC and TLIHC, a comparative study between them in terms of AC and DC voltage gain, voltage and current stresses and number of controlled and uncontrolled devices used are discussed in this chapter. The performance of TLIHC is also compared with some of the existing hybrid converters in terms of voltage and current stresses, number of elements used, DC and AC voltage gains and efficiency. The simulation and experimental verifications of TLMPHC and TLIHC are carried out for validating their performances. Finally, the limitations and applications of the proposed TLIHC are discussed.

3.2 Mathematical Modelling

The mathematical modeling of both the proposed hybrid converters TLIHC and TLMPHC are carried out by considering the entire circuit operation in two operating states. Further, from the key waveforms, it can be observed that both the proposed hybrid converters TLIHC and TLMPHC are operated in two states on the basis of the charging and discharging mode of passive components. The small signal analysis is required to verify the minimum phase property and close loop performance of the proposed TLIHC.

3.2.1 Mathematical Modeling of TLMPHC

From the operational waveforms, it can be observed that the two operating states of the proposed TLMPHC are shoot-through and non-shoot-through states. However, the non-shoot through state is nothing but a combined interval of both power and zero states. Further, to verify the simulation as well as developed prototype experimental results in the later part of this chapter, mathematical modeling of the proposed TLMPHC is carried out by considering the entire circuit as a single switch converter. The small signal analysis is required to verify the minimum phase property and close loop performance of the proposed TLMPHC.

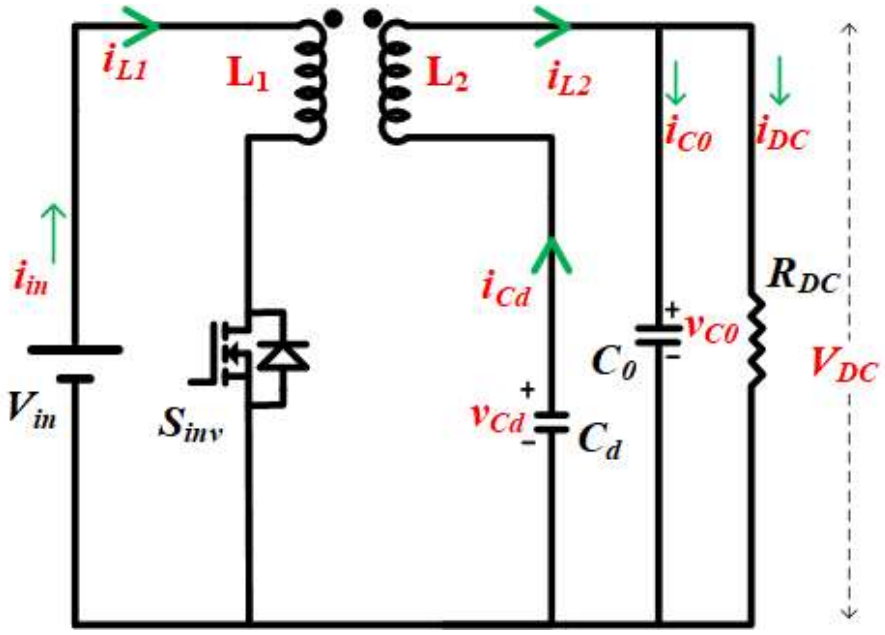
The proposed TLMPHC for steady state operation is considered as a single switch converter. For deriving the steady state expressions of TLMPHC, the inverter part (switches S_1-S_6, filter inductors L_{f1} and L_{f2} and AC load) is considered as a single switch (S_{inv}) along with an equivalent resistance (R_{eq}) connected across S_{inv}. During the steady state operation, the proposed TLMPHC is operates in two states: (i) S_{inv} is in ON position (shoot-through interval) and (ii) S_{inv} is in OFF position (power and zero intervals) as shown in Fig. 3.1 (a) and (b).

When S_{inv} is in ON position, the simplified circuit of TLMPHC is shown in Fig. 3.1 (a). The corresponding mathematical expressions are given as

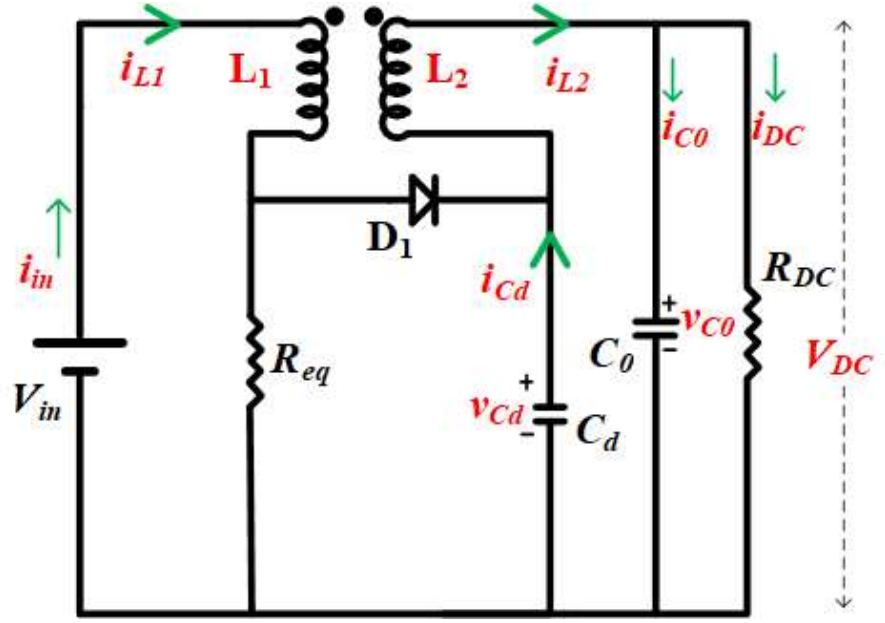
$$\left.\begin{aligned} L_1\left(\frac{di_{L1}}{dt}\right) - M\left(\frac{di_{L2}}{dt}\right) &= v_{in} \\ L_2\left(\frac{di_{L2}}{dt}\right) - M\left(\frac{di_{L1}}{dt}\right) &= v_{Cd} - v_{C0} \\ C_d\left(\frac{dv_{Cd}}{dt}\right) &= i_{L2} \\ C_o\left(\frac{dv_{C0}}{dt}\right) &= i_{L2} - \frac{v_{C0}}{R_{DC}} \end{aligned}\right\} \tag{3.1}$$

Similarly, when S_{inv} is in OFF position, the simplified circuit of TLMPHC is shown in Fig. 3.1 (b). The corresponding mathematical expressions are given as

$$\left.\begin{aligned} L_1\left(\frac{di_{L1}}{dt}\right) - M\left(\frac{di_{L2}}{dt}\right) &= v_{in} - v_{Cd} \\ L_2\left(\frac{di_{L2}}{dt}\right) - M\left(\frac{di_{L1}}{dt}\right) &= v_{Cd} - v_{C0} \\ C_d\left(\frac{dv_{Cd}}{dt}\right) &= i_{L2} - i_{L1} + \frac{v_{Cd}}{R_{eq}} \\ C_o\left(\frac{dv_{C0}}{dt}\right) &= i_{L2} - \frac{v_{C0}}{R_{DC}} \end{aligned}\right\} \tag{3.2}$$



(a)



(b)

Fig. 3.1 Simplified circuit of TLMPHC for the steady state operation **(a)** S_{inv} is in ON position and **(b)** S_{inv} is in OFF position.

By applying the volt-second balance principle to the inductor and charge-second balance principle to the capacitor in (3.1) and (3.2) for a complete switching cycle of T_S, the steady-state voltage and current expressions of TLMPHC are obtained as follows

$$\left.\begin{aligned} V_{C0} = V_{Cd} &= \frac{V_{in}}{1-D} \\ V_{AC}(pk) &= M_i \frac{V_{in}}{1-D} \\ I_{L1} &= \frac{V_{Cd}}{R_{eq}} + \frac{V_{C0}}{R_{DC}} \\ I_{L2} &= \frac{V_{C0}}{R_{DC}} \end{aligned}\right\} \tag{3.3}$$

3.2.2 Small Signal Analysis of TLMPHC

The S_{inv} ON time and OFF time expressions of the TLMPHC due to charging and discharging behaviour of passive components are derived in (3.1) and (3.2). The dynamic state equations of the TLMPHC are follows

$$K_1 \frac{dX}{dt} = A_1 * X + B_1 * U \tag{3.4}$$

$$K_2 \frac{dX}{dt} = A_2 * X + B_2 * U \tag{3.5}$$

where K_1 and K_2 are the coefficient matrices during ON time and OFF time of S_{inv}; A_1, A_2 are the state matrices during ON time and OFF time of S_{inv}; B_1, B_2 are the input matrices during ON time and OFF time of S_{inv}; X is the state variable vector and U is the input vector.

The state variable vector and input vector are

$$X = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{cd} \\ v_{C0} \end{bmatrix} \text{ and } U = \begin{bmatrix} V_{in} \\ D \end{bmatrix}$$

The ON time and OFF time coefficient matrices are

$$K_1 = K_2 = \begin{bmatrix} L_1 & -M & 0 & 0 \\ -M & L_2 & 0 & 0 \\ 0 & 0 & C_d & 0 \\ 0 & 0 & 0 & C_0 \end{bmatrix}$$

The ON time and OFF time input matrices are

$$B_1 = B_2 = \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix}$$

The ON time and OFF time state variable matrices are

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & -(\frac{1}{R_{DC}}) \end{bmatrix} \text{ and } A_2 = \begin{bmatrix} 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & -1 \\ -1 & 1 & \frac{1}{R_{eq}} & 0 \\ 0 & 1 & 0 & -\frac{1}{R_{DC}} \end{bmatrix}$$

By multiplying duty ratio (D) to (3.4) and D' to (3.5) and summing them to obtain the state equation as

$$K\frac{dX}{dt} = A * X + B * U \tag{3.6}$$

where coefficient matrix $K = DK_1 + D'K_2 = K_1 = K_2$, input matrix $B = DB_1 + D'B_2 = B_1 = B_2$ and state variable matrix $A = DA_1 + D'A_2$ gives

$$A = \begin{bmatrix} 0 & 0 & -D' & 0 \\ 0 & 0 & 1 & -1 \\ -D' & 1 & \frac{D'}{R_{eq}} & 0 \\ 0 & 1 & 0 & -(\frac{1}{R_{DC}}) \end{bmatrix}$$

To obtain the steady state expressions of (3.3), the derivative term of (3.6) is assumed to be zero. The steady state, state variable vector (X_C) is

$$X_C = -inv\,(A) * B * U \tag{3.7}$$

For determining the dynamic behavior of the state variables, the input signals are

$$\left.\begin{array}{c} v_{in} = V_{in} + \hat{v}_{in} \\ d = D + \hat{d} \\ x = X + \hat{x} \end{array}\right\} \tag{3.8}$$

Considering constant input voltage V_{in}, the small-signal average transfer function of the state variable for the proposed TLMPHC is

$$\text{TF} = [0 \quad 0 \quad 0 \quad 1] \times [SI - K^{-1}A]^{-1} \times K^{-1}[(A_1 - A_2)X_C + (B_1 - B_2)V_{in}] \tag{3.9}$$

where $SI = \begin{bmatrix} S & 0 & 0 & 0 \\ 0 & S & 0 & 0 \\ 0 & 0 & S & 0 \\ 0 & 0 & 0 & \text{S} \end{bmatrix}$

The control to dc output transfer function is

$$\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)} = [0 \quad 0 \quad 0 \quad 1] \times [SI - K^{-1}A]^{-1} \times S_9 \tag{3.10}$$

where $S_9 = K^{-1}(A_1 - A_2)X_C$, as $B_1 = B_2$

Hence, the obtained control to dc output transfer function ($\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)}$) is

$$\frac{A_3 s^3 + A_2 s^2 + A_1 s^1 + A_0}{B_4 s^4 + B_3 s^3 + B_2 s^2 + B_1 s^1 + B_0} \tag{3.11}$$

where $A_3 = 2R_{DC}C_d M^2 V_{C0} + -R_{DC}C_d I_{L2} M^2 R_{eq} + R_{eq} M C_d L_1 R_{DC}$

$A_2 = R_{DC}(1-D)I_{L1}M^2 + R_{DC}C_d D R_{eq} V_{Cd} M - R_{DC}(1-D)I_{L1}L_1 L_2 - 2R_{DC}C_d D L_1 R_{eq} V_{C0}$

$A_1 = -R_{DC}(1-D)L_2 V_{Cd} + R_{DC}(1-D)^2 I_{L2} L_2 R_{eq} - R_{DC}(1-D)^2 I_{L1} L_1 R_{eq} + R_{DC}(1-D)DI_{L2}MR_{eq}$

$A_0 = -2R_{DC}(1-D)^2 R_{eq} V_{Cd} - R_{eq}(1-D)^2 D V_{C0}$

$B_4 = C_d C_o R_{DC} R_{eq}(L_1 L_2 - M^2)$

$B_3 = C_d R_{eq}(L_1 L_2 - M^2) + (1-D)L_1 L_2 R_{DC}(C_d + C_o)$

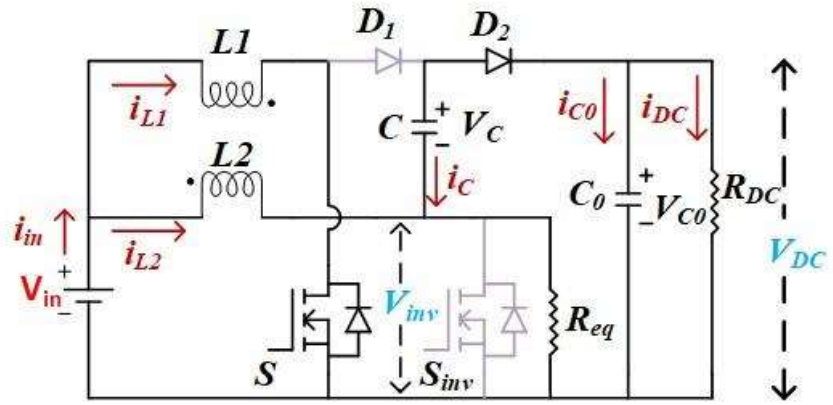
$B_2 = D(L_1 L_2 - M^2) + C_d D^2 L_1 R_{eq} R_{DC} + C_0(1-D)^2 L_2 R_{eq} R_{DC} + C_0(1-D)^2 L_1 R_{eq} R_{DC} + 2C_0(1-D)DMR_{eq}R_{DC}$

$B_1 = L_2(1-D)^2 R_{eq} + 2MR_{eq}(1-D) + L_1 R_{eq} D$

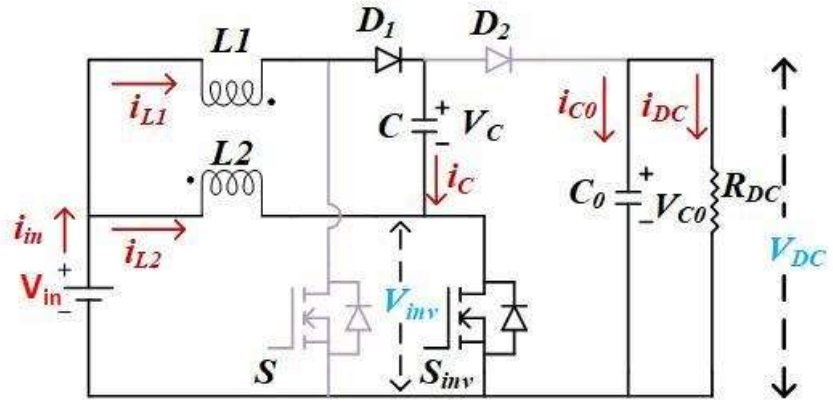
$B_0 = (1-D)^2 R_{DC} R_{eq}$

3.2.3 Mathematical Modelling of TLIHC

The two operating states of the TLIHC are the shoot-through and non-shoot-through states. The non-shoot through state is the combined interval of both power and zero states. As, the proposed TLIHC is an interleaved hybrid converter, for mathematical modelling, the entire circuit is realized as the complementary operation of two controlled switches (S and S_{inv}). So, for the mathematical modelling the inverter part ($S_1 - S_6$, L_{f1}, L_{f2} and R_{AC}) of the proposed TLIHC is replaced by S_{inv} and R_{eq}. The simplified circuit obtained is shown in Fig. 3.2 for two operating conditions: i) S ON and S_{inv} OFF and ii) S OFF and S_{inv} ON.



(a)



(b)

Fig. 3.2 Equivalent circuits of the proposed TLIHC for mathematical modelling. **(a)** S ON and S_{inv} OFF **(b)** S OFF and S_{inv} ON.

For the operating condition, S ON and S_{inv} OFF (non-shoot through interval), the equivalent circuit is shown in Fig. 3.2 (a) and the corresponding mathematical equations are as follows

$$\left.\begin{aligned} L_1\left(\frac{di_{L1}}{dt}\right) - M\left(\frac{di_{L2}}{dt}\right) &= v_{in} \\ L_2\left(\frac{di_{L2}}{dt}\right) - M\left(\frac{di_{L1}}{dt}\right) &= v_{in} + v_C - v_{C0} \\ C\left(\frac{dv_C}{dt}\right) &= -i_{L2} - \frac{v_C}{R_{eq}} + \frac{v_{C0}}{R_{eq}} \\ C_0\left(\frac{dv_{C0}}{dt}\right) &= i_{L2} + \frac{v_C}{R_{eq}} - \left(\frac{R_{eq}+R_{DC}}{R_{eq}R_{DC}}\right)V_{C0} \end{aligned}\right\} \quad (3.12)$$

where M is the mutual inductance between input inductors L_1 and L_2.

In state space form the above (3.12) is represented as

$$K_1\dot{X} \quad = \quad A_1X \quad + \quad B_1U \tag{3.13}$$

where K_1 is the coefficient matrix during S ON and S_{inv} OFF; A_1 is the state matrix during S ON and S_{inv} OFF; B_1 is the input matrix during S ON and S_{inv} OFF; X is the state variable vector and U is the input vector.

The state variable vector and input vector are

$$X = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_c \\ v_{C0} \end{bmatrix} \text{ and } U = \begin{bmatrix} V_{in} \\ D \end{bmatrix}$$

$$K_1 = \begin{bmatrix} L_1 & -M & 0 & 0 \\ -M & L_2 & 0 & 0 \\ 0 & 0 & C & 0 \\ 0 & 0 & 0 & C_0 \end{bmatrix} \text{ and } A_1, B_1 \text{ are}$$

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 0 & -1 & \frac{-1}{R_{eq}} & \frac{1}{R_{eq}} \\ 0 & 1 & \frac{-1}{R_{eq}} & \frac{R_{eq}+R_{DC}}{R_{eq}R_{DC}} \end{bmatrix} \; and \; B_1 = \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix}$$

Similarly, for the operating condition S OFF and S_{inv} ON (shoot-through interval), the equivalent circuit is shown in Fig. 3.2 (b) and the corresponding mathematical equations are as follows

$$\left.\begin{aligned} L_1\left(\frac{di_{L1}}{dt}\right) - M\left(\frac{di_{L2}}{dt}\right) &= v_{in} - v_C \\ L_2\left(\frac{di_{L2}}{dt}\right) - M\left(\frac{di_{L1}}{dt}\right) &= v_{in} \\ C\left(\frac{dv_C}{dt}\right) &= i_{L1} \\ C_0\left(\frac{dv_{C0}}{dt}\right) &= -\frac{v_C}{R_{DC}} \end{aligned}\right\} \tag{3.14}$$

In state space form of (3.14) is represented as

$$K_2\dot{X} \quad = \quad A_2X \quad + \quad B_2U \tag{3.15}$$

where K_2 is the coefficient matrix during S OFF and S_{inv} ON; A_2 is the state matrix during S OFF and S_{inv} ON; B_2 is the input matrix during S ON and S_{inv} OFF. K_2, A_2 and B_2 are

$$K_2 = \begin{bmatrix} L_1 & -M & 0 & 0 \\ -M & L_2 & 0 & 0 \\ 0 & 0 & C & 0 \\ 0 & 0 & 0 & C_0 \end{bmatrix}, A_2 = \begin{bmatrix} 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_{DC}} \end{bmatrix} \text{ and } \mathrm{B}_2 = \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix}$$

The state variable vector X and input vector U are same as that of during the non-shoot through state (S ON and S_{inv} OFF).

3.2.4 State Space Averaging of TLIHC

The large signal model is obtained using the state space averaging technique as follows:

$$\left.\begin{matrix} K\dot{X} = AX + BU \\ Y = CX \end{matrix}\right\} \tag{3.16}$$

where coefficient matrix $K = DK_1 + D'K_2$, input matrix $B = DB_1 + D'B_2$ and state variable matrix $A = DA_1 + D'A_2$. The matrices K, B and A are

$$K = \begin{bmatrix} L_1 & -M & 0 & 0 \\ -M & L_2 & 0 & 0 \\ 0 & 0 & C & 0 \\ 0 & 0 & 0 & C_0 \end{bmatrix}, B = \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} \text{ and}$$

$$A = \begin{bmatrix} 0 & 0 & \frac{-(D*M)-(L_2*(D-1))}{M^2-L_1*L_2} & \frac{(D*M)}{M^2-L_1*L_2} \\ 0 & 0 & \frac{-((D-1)*M)-(L_1*D)}{M^2-L_1*L_2} & \frac{(L_2*D)}{M^2-L_1*L_2} \\ \frac{1-D}{C} & \frac{-D}{C} & \frac{-D}{C*R_{eq}} & \frac{D}{C*R_{eq}} \\ 0 & \frac{D}{C_0} & \frac{D}{C_0*R_{eq}} & \frac{-1}{C_0*R_{DC}} - \frac{D}{C_0*R_{eq}} \end{bmatrix}$$

The output matrix (C) is

$$C = [0\ 0\ 0\ 1]$$

Using the obtained large signal state space model of the proposed TLIHC and by applying $\dot{X} = 0$ in (3.16), the derived steady state values of the system are

$$\left.\begin{matrix} V_C = \frac{V_{in}}{1-D} \\ V_{C0} = V_{DC} = \frac{V_{in}}{D(1-D)} \\ V_{AC}(pk) = M_i \frac{V_{in}}{D} \\ I_{L1} = \frac{V_{in}}{R_{DC}D(1-D)^2} \\ I_{L2} = \frac{V_{in}(R_{DC}D(1-D)+R_{eq})}{R_{eq}R_{DC}D(1-D)} \end{matrix}\right\} \tag{3.17}$$

For determining the dynamic behaviour of the state variables, the input signals are

$$\left.\begin{aligned} v_{in} &= V_{in} + \hat{v}_{in} \\ d &= D + \hat{d} \\ x &= X + \hat{x} \end{aligned}\right\} \tag{3.18}$$

Considering constant input voltage V_{in}, the small-signal average transfer function $(\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)})$ of the state variable for the proposed TLIHC can be obtained by using the following relation,

$$\text{TF} = (\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)}) = C\,(sI - A)^{-1}\,F \tag{3.19}$$

where F=$\begin{bmatrix} 0 & 0 & \frac{-(M+L_2)}{M^2-L_1*L_2} & \frac{(M)}{M^2-L_1*L_2} \\ 0 & 0 & \frac{-(M+L_1)}{M^2-L_1*L_2} & \frac{(L_2)}{M^2-L_1*L_2} \\ \frac{-1}{C} & \frac{-1}{C} & \frac{-1}{C*R_{eq}} & \frac{1}{C*R_{eq}} \\ 0 & \frac{1}{C_0} & \frac{1}{C_0*R_{eq}} & -\frac{1}{C_0*R_{eq}} \end{bmatrix} X_{steady}$

Hence, the obtained transfer function $(\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)})$ is given as

$$\frac{a_3s^3+a_2s^2+a_1s^1+a_0}{b_4s^4+b_3s^3+b_2s^2+b_1s^1+b_0} \tag{3.20}$$

where

$a_3 = R_{DC}CM^2V_C + R_{DC}CM^2V_{C0} - R_{DC}CL_1L_2V_C - R_{DC}CL_1L_2V_{C0} - R_{DC}CI_2M^2R_{eq} + R_{DC}CI_2L_1L_2R_{eq}$

$a_2 = R_{DC}DI_1M^2 + R_{DC}CDR_{eq}V_CM - R_{DC}DI_1L_1L_2 - R_{DC}CDL_1R_{eq}V_C - R_{DC}CDL_1R_{eq}V_{C0}$

$a_1 = -R_{DC}(1-D)^2L_2(V_C+V_{C0}) - R_{DC}(1-D)DL_2V_C + R_{DC}(1-D)^2I_2L_2R_{eq} - R_{DC}(1-D)^2I_1L_1R_{eq} - R_{DC}(1-D)DI_1MR_{eq} + R_{DC}(1-D)DI_2MR_{eq}$

$a_0 = R_{DC}(1-D)D^2R_{eq}V_{C0} - R_{DC}(1-D)^2DR_{eq}V_C - R_{DC}(1-D)^2DR_{eq}V_{C0}$

$b_4 = CC_0R_{DC}R_{eq}(L_1L_2 - M^2)$

$b_3 = CR_{eq}(L_1L_2 - M^2) - M^2R_{DC}(C+C_0) + DL_1L_2R_{DC}(C+C_0)$

$b_2 = D(L_1L_2 - M^2) + CD^2L_1R_{eq}R_{DC} + C_0(1-D)^2L_2R_{eq}R_{DC} + C_0D^2L_1R_{eq}R_{DC} + 2C_0(1-D)DMR_{eq}R_{DC}$

$b_1 = L_2(1-D)^2DR_{DC} + L_2R_{eq}(1-D)^2 + 2MR_{eq}(1-D)D + L_1R_{eq}D^2$

$b_0 = (1-D)^2D^2R_{DC}R_{eq}$

3.3 Key Features

Both TLIHC and TLMPHC has some important features like: they provide simultaneous AC and DC outputs from a single DC input voltage, minimize the harmful common mode leakage current when it is connected to the grid or its inverter output neutral is grounded and achieve minimum phase property.

3.3.1 Simultaneous DC and AC outputs

From the circuit point of view, it is observed that the proposed TLMPHC is a boost derived type transformerless hybrid converter, where the controlled switch of boost converter is replaced by a modified voltage source inverter. Therefore, it provides well-regulated DC and AC outputs simultaneously using a single DC input, within the operating condition of $D + M_i \leq 1$. Further, as the proposed TLMPHC has inherent shoot-through capability, it improves the quality of AC output voltage. The AC and DC gains of the TLMPHC are

$$\frac{(V_{AC})_{peak}}{V_{in}} = \frac{M_i}{1-D} \tag{3.21}$$

$$\frac{V_{DC}}{V_{in}} = \frac{1}{1-D} \tag{3.22}$$

Similarly, the AC and DC power expressions are

$$P_{ac} = 0.5 \frac{V_{in}^2}{(1-D)^2 * R_{AC}} * M_i^2 \tag{3.23}$$

$$P_{dc} = \frac{V_{in}^2}{(1-D)^2 * R_{DC}} \tag{3.24}$$

where R_{AC} and R_{DC} are the AC and DC load resistances respectively and V_{in} is the input voltage.

From the circuit point of view, it is observed that two boost converters are interleaved parallelly to build the proposed TLIHC, where the lower rating boost converter switch is replaced by a modified voltage source inverter. Further, from the circuit operation, it can be concluded that the duty ratio (D) is decided by the switch-on interval of switch (S) and modulation index (M_i) by the power interval (switch-on state of either switches S_1 and S_5 or switches S_3 and S_6 of the inverter part). Both the switching operations occur during the non-shoot through state. So, the values of D and M_i can be increase independently to achieve wide operating range of D and M_i. Hence, the

proposed TLIHC can regulate both the DC and AC loads simultaneously from a single DC source at the operating conditions $D + M_i \geq 1$ and $D + M_i \leq 1$. Further, due to the inherent shoot-through capability of the proposed TLIHC, the quality of AC output voltage is improved. The DC and AC gains of the TLIHC are

$$\frac{V_{DC}}{V_{in}} = \frac{1}{D(1-D)} \tag{3.25}$$

$$\frac{(V_{AC})_{peak}}{V_{in}} = \frac{M_i}{D} \tag{3.26}$$

Similarly, the DC and AC power expressions are

$$P_{dc} = \frac{V_{in}^2}{D^2(1-D)^2 R_{DC}} \tag{3.27}$$

$$P_{ac} = 0.5 \frac{V_{in}^2}{D^2 R_{AC}} M_i^2 \tag{3.28}$$

3.3.2 Leakage Current Minimization

In case of both TLIHC and TLMPHC, as there is no galvanic isolation (transformer) between the PV system and the inverter output neutral, a high frequency common mode voltage appears across the parasitic capacitance (C_{PV}). This leads to the flow of common mode leakage current in the system, when either they are connected to the grid or their inverter neutral point is grounded. To minimize the common mode leakage current within the limits (< 300 mA), the total common mode voltage (v_{tcm}) across the PV panel to ground parasitic capacitance should be constant during all the operating intervals (power, zero and shoot-through intervals). As the inverter parts of both the converters TLIHC and TLMPHC are same, the leakage current analysis model for both the converters are similar. Fig. 3.3 shows the inverter parts of both TLIHC and TLMPHC for evaluation of common mode leakage current. If the negative terminal (N) of input voltage/solar panel (V_{in}) is considered as the reference point, output of the inverter bridge with reference to terminal 1 and 2 is shown in Fig. 3.3. According to the definition given in [28] and [87], the common mode voltage (V_{cm}) and differential mode voltage (V_{dm}) of the inverter can be calculated as follows

$$\left.\begin{aligned} V_{cm} &= \frac{V_{1N}+V_{2N}}{2} \\ V_{dm} &= V_{1N} - V_{2N} \end{aligned}\right\} \tag{3.29}$$

From (3.29), V_{1N} and V_{2N} can be expressed in terms of V_{cm} and V_{dm} are as follows

$$\left.\begin{aligned} V_{1N} &= V_{cm} + \frac{V_{dm}}{2} \\ V_{2N} &= V_{cm} - \frac{V_{dm}}{2} \end{aligned}\right\} \tag{3.30}$$

As the outputs of the inverter bridge concerning to the reference point (N) are V_{1N} and V_{2N} respectively, the total common mode voltage appears across the C_{PV} is found out by simplifying Fig. 3.3 into its equivalent circuit, where all the low valued parasitic parameters are neglected.

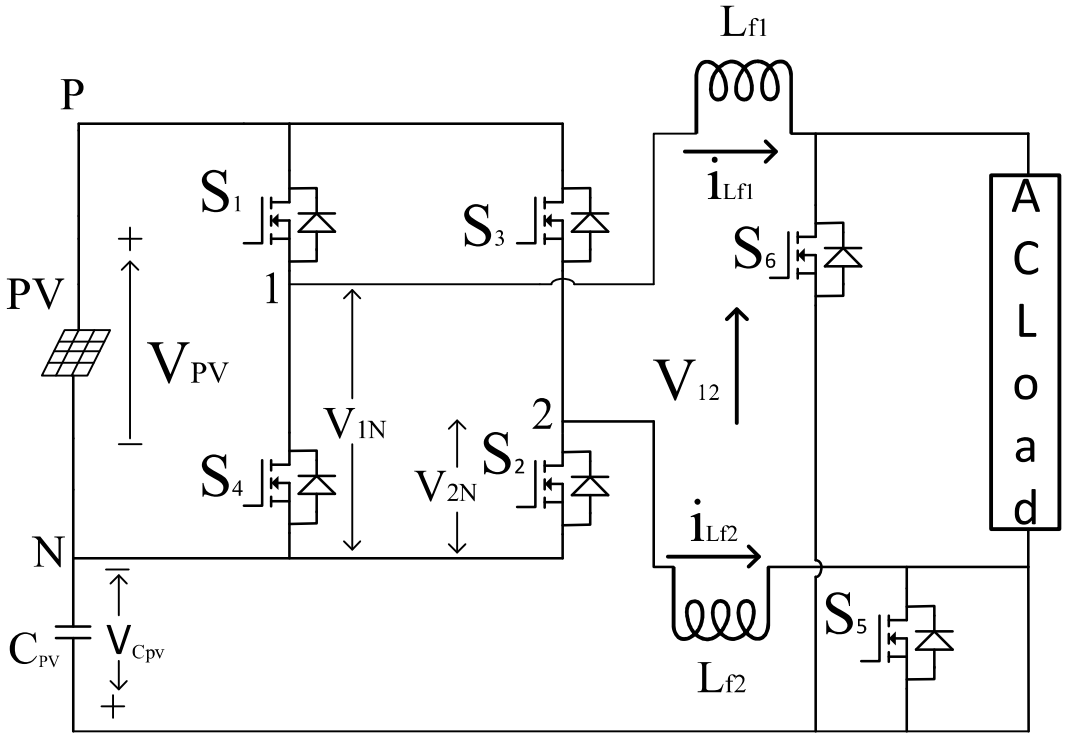


Fig. 3.3 Inverter part of both TLMPHC and TLIHC in stand-alone mode for evaluation of common mode leakage current.

For developing a simplified total common mode voltage model, the inverter parts of both TLIHC and TLMPHC is shown in Fig. 3.3. This can be converted into Thevenin's equivalent circuit across C_{PV} for medium frequency range (< 50 KHz) as shown in Fig. 3.4.

By applying KVL in Fig. 3.4, for determining the current (i) flowing through the filter inductor is

$$-v_{cm} - \frac{v_{dm}}{2} - iL_{f1} - iL_{f2} + v_{cm} - \frac{v_{dm}}{2} = 0 \tag{3.31}$$

The total common mode voltage (v_{tcm}) is

$$v_{tcm} = v_{cm} + v_{sm} \tag{3.32}$$

where $v_{sm} = v_{dm}\frac{L_{f2}-L_{f1}}{2(L_{f2}+L_{f1})}$

During the entire positive half cycle of AC output voltage, current through the filter inductor L_{f2} is zero. Thus, during this half cycle, L_{f2} is considered as zero from the circuit operation point of view. Similarly, for the entire negative half cycle, the filter inductor L_{f1} is considered as zero. So, v_{sm} is given as

$$v_{sm} = \begin{cases} -\frac{V_{dm}}{2} & \text{for entire positive half cycle} \\ \frac{V_{dm}}{2} & \text{for entire negative half cycle} \end{cases} \tag{3.33}$$

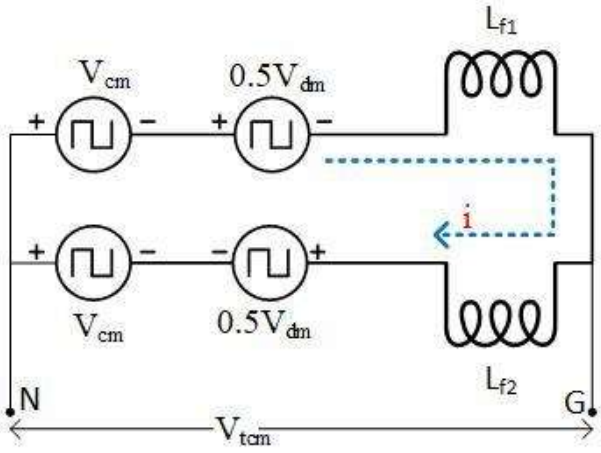


Fig. 3.4 Thevenin's equivalent model for total common mode voltage.

During the zero and shoot-through intervals $v_{1N} = v_{2N} = 0$. As the filter inductor current freewheels through the lower switches of the inverter bridge during the zero and shoot-through intervals, both the switches of either leg are in switch-on position. Therefore, during these two intervals also V_{tcm} becomes zero. The v_{tcm} of TLIHC and TLMPHC during different states of a switching cycle are given in Table 3.1 and 3.2 respectively. It can be observed from Table 3.1 that V_{tcm} is zero during the entire switching cycle. Hence, the flow of common mode leakage current is minimized in TLIHC. Similarly, from Table 3.2 it can be observed that the v_{tcm} is zero during the entire switching cycle of the TLMPHC. In this way, the common mode leakage current is minimized in both TLIHC and TLMPHC.

From operation of the proposed TLMPHC and TLIHC total common mode voltage (V_{tcm}) expression (3.31), it can be observed that even though both the converters are symmetrical filter-based topologies, they can minimization the leakage current in case of asymmetrical filter-based topology also. This is because of the fact that for the entire positive half cycle L_{f1} is zero and for the entire negative half cycle L_{f2} is zero. In addition, due to the developed SPWM-based switching technique the common mode voltage term nullifies the differential mode voltage term and hence, V_{tcm} becomes constant (zero) which results reduced common mode leakage current. Therefore, in both the cases, V_{tcm} is more dependent on V_{cm}. On the other hand, in case of the DC output (for the proposed TLMPHC and TLIHC), C_{PV} is not considered, as the DC output negative terminal is not grounded similar to AC output neutral point. Hence, the common mode leakage current problem does not exist for DC output, unlike the AC output.

Table 3.1 Analysis of Total Common mode Voltage of TLIHC in a Complete Switching Cycle

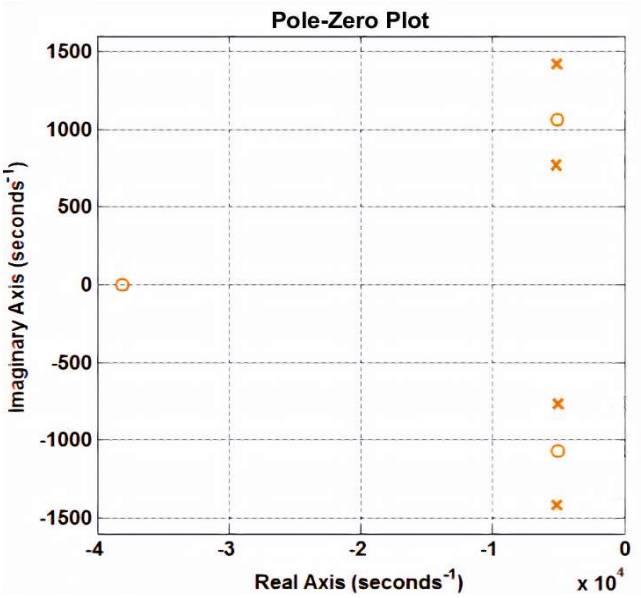
Operating intervals during positive and negative half cycles		S_1	S_2	S_3	S_4	S_5	S_6	v_{1N}	v_{2N}	v_{cm}	v_{dm}	V_{sm}	V_{tcm}
Positive half cycle of AC output	Shoot-through	ON	OFF	OFF	ON	ON	OFF	0	0	0	0	0	0
	Zero	OFF	OFF	OFF	OFF	ON	OFF	0	0	0	0	0	0
	Power	ON	OFF	OFF	OFF	ON	OFF	$\frac{v_{in}}{D}$	0	$\frac{v_{in}}{2D}$	$\frac{v_{in}}{D}$	$-\frac{v_{in}}{2D}$	0
Negative half cycle of AC output	Shoot-through	OFF	ON	ON	OFF	OFF	ON	0	0	0	0	0	0
	Zero	OFF	OFF	OFF	OFF	OFF	ON	0	0	0	0	0	0
	Power	OFF	OFF	ON	OFF	OFF	ON	0	$\frac{v_{in}}{D}$	$\frac{v_{in}}{2D}$	$-\frac{v_{in}}{D}$	$-\frac{v_{in}}{2D}$	0

Table 3.2 Analysis of Total Common mode Voltage of TLMPHC in a Complete Switching Cycle

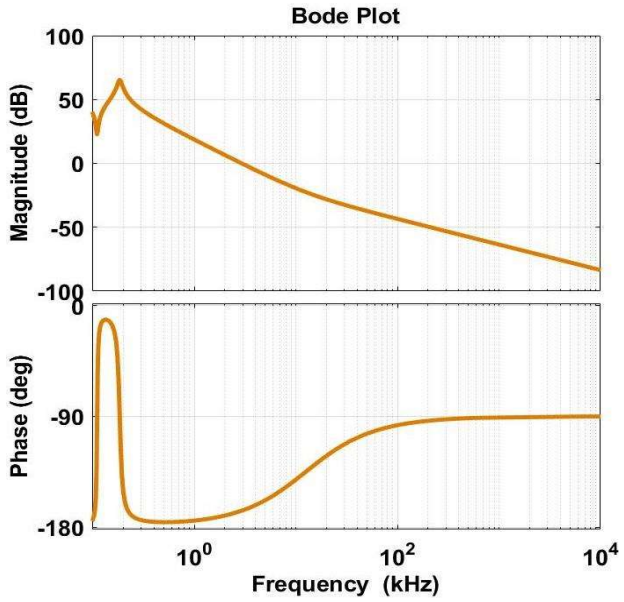
Operating intervals during positive and negative half cycles		$\mathbf{v_{1N}}$	$\mathbf{v_{2N}}$	$\mathbf{v_{cm}}$	$\mathbf{v_{dm}}$	$\mathbf{v_{sm}}$	$\mathbf{v_{tcm}}$
Positive half cycle of AC output	Shoot-through	0	0	0	0	0	0
	Zero	0	0	0	0	0	0
	Power	$\frac{v_{in}}{1-D}$	0	$\frac{v_{in}}{2(1-D)}$	$\frac{v_{in}}{1-D}$	$-\frac{v_{in}}{2(1-D)}$	0
Negative half cycle of AC output	Shoot-through	0	0	0	0	0	0
	Zero	0	0	0	0	0	0
	Power	0	$\frac{v_{in}}{1-D}$	$\frac{v_{in}}{2(1-D)}$	$-\frac{v_{in}}{1-D}$	$-\frac{v_{in}}{2(1-D)}$	0

3.3.3 Minimum Phase Behaviour

For the control to output transfer function $\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)}$ (as given in (3.11) of section 3.2.2), the pole-zero and bode plots of TLMPHC are shown in Fig. 3.5 (a) and (b) respectively. From the pole-zero plot, it can be observed that all the zeros of $\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)}$ lies in the left side of $j\omega$–axis. Further, from the phase plot of Fig. 3.5 (b), it can be observed that there is no phase dip at frequencies corresponding to zeros. As, in case of non-minimum phase system, zeros lie in the right side of $j\omega$–axis, there is no phase dip at frequencies corresponding to zeros. So, from the pole-zero plot and phase plot, it can be concluded that the proposed TLMPHC has no RHPZ and the minimum phase property of TLMPHC is achieved. Further, from the operating modes of TLMPHC as shown in Fig. 2.3, the minimum phase property is verified as the DC output capacitor (C_0) is not discharged during the shoot-through state (switch-on state of boost converter).



(a)



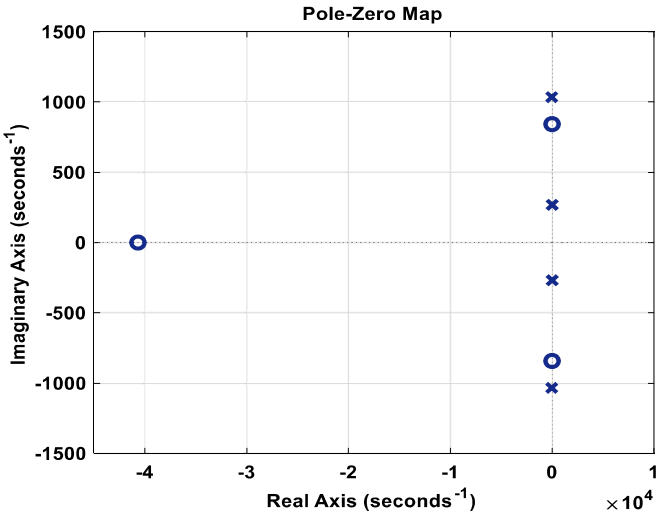
(b)

Fig. 3.5 Minimum phase behavior of TLMPHC **(a)** Pole-zero plot and **(b)** Bode plot.

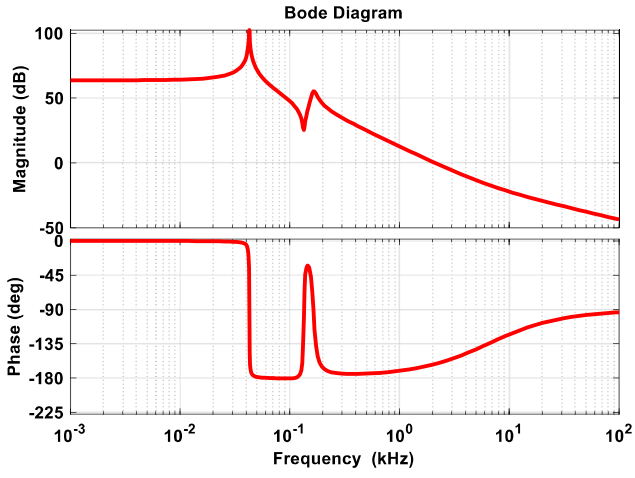
To verify the minimum phase behaviour of the TLIHC in more details, the Routh-Hurwitz (RH) criterion for the numerator coefficients of $\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)}$ (i.e., $a_{0\to3}$) should be satisfied. According to RH criteria the coefficients $a_{0\to3}$ and also $a_1a_2 - a_0a_3$ should be greater than zero to achieve minimum phase behaviour. From the numerator coefficients of (3.9), it can be observed that except a_0, all other coefficients and $a_1a_2 - a_0a_3$ are satisfied the greater than zero condition only when

$L_1L_2 > M^2$; i. e., only when both the coils are not tightly coupled (co-efficient of coupling $K \neq 1$). On the other hand, it can also be observed that the condition $a_0 > 0$ is satisfied only when $V_{C0} > \frac{1-D}{D}(V_C + V_{C0})$.

For the control to output transfer function $\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)}$ (as given in section 3.2.4), the pole-zero and bode plots of TLIHC are shown in Fig. 3.6 (a) and (b) respectively. From the pole-zero plot, it can be observed that all the poles and zeros of $\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)}$ lies in the left side of $j\omega$–axis. The left half plane poles represent the stability of the system and the elimination of right half plane zeros make the system minimum phase.



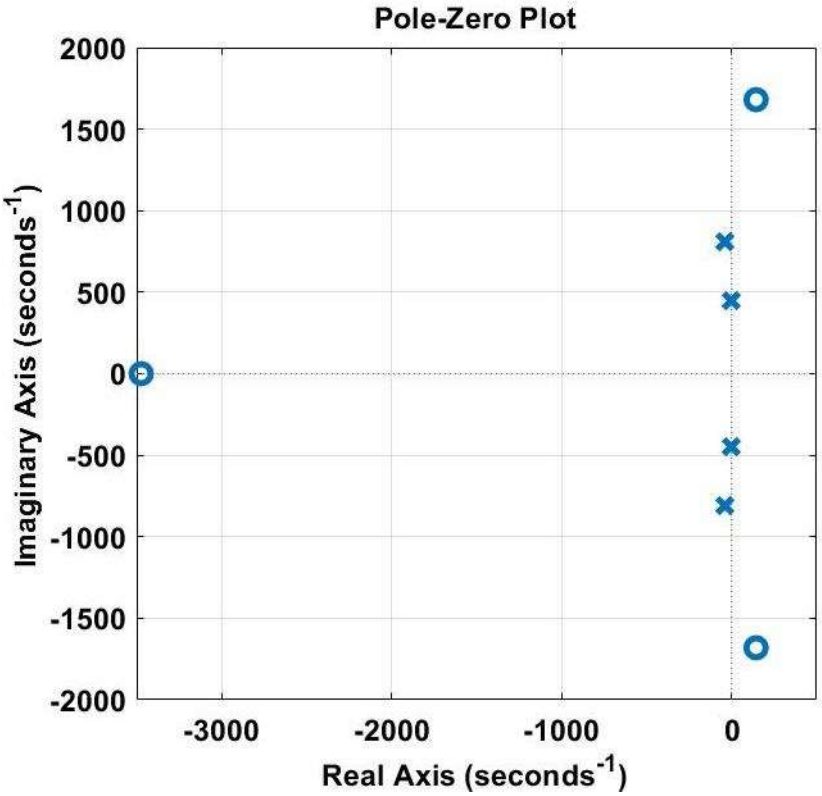
(a)



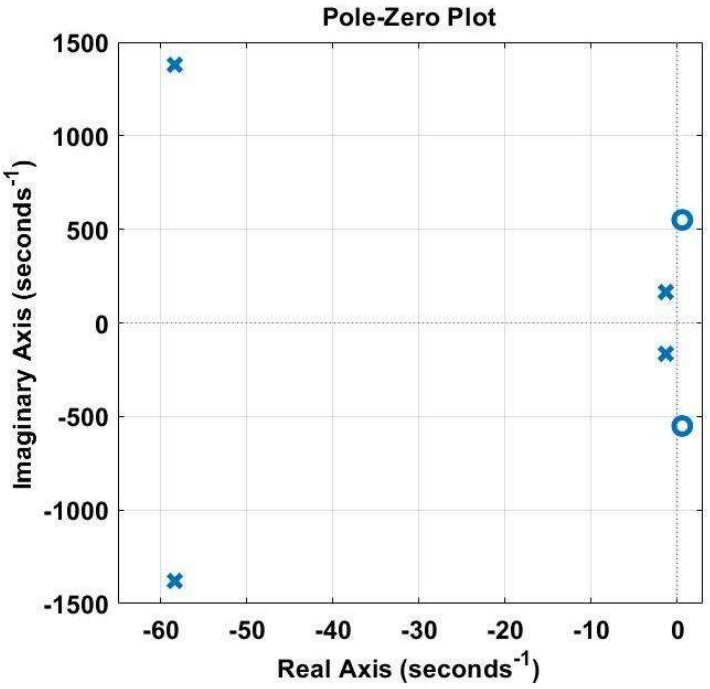
(b)

Fig. 3.6 Minimum phase behavior of TLIHC **(a)** Pole-zero plot and **(b)** Bode plot.

From the RH criteria conditions, it can be observed that the proposed TLIHC achieves minimum phase behaviour, when the duty ratio (D) is more than 0.61 (from the condition $a_0 > 0$). Similarly, the value of D beyond 0.85 due to insufficient discharging time for inductor L_1 and charging time for DC link capacitor (C), the proposed TLIHC fails to achieve minimum phase property. Further from the phase plot of Fig. 3.6 (b), it can be observed that there is no phase dip at frequencies corresponding to the zeros. Fig. 3.7 shows the pole-zero plot of TLIHC for D = 0.6 and D = 0.86. From the figure it can be observed that for both the values of D one pair of complex conjugate zeros are lies in the right plane of $j\omega$-axis. So, from the pole-zero plot and phase plot, it can be concluded that the proposed TLIHC has no RHPZ and the minimum phase property is achieved for the operating condition 0.61 < D ≤ 0.85.



(a)

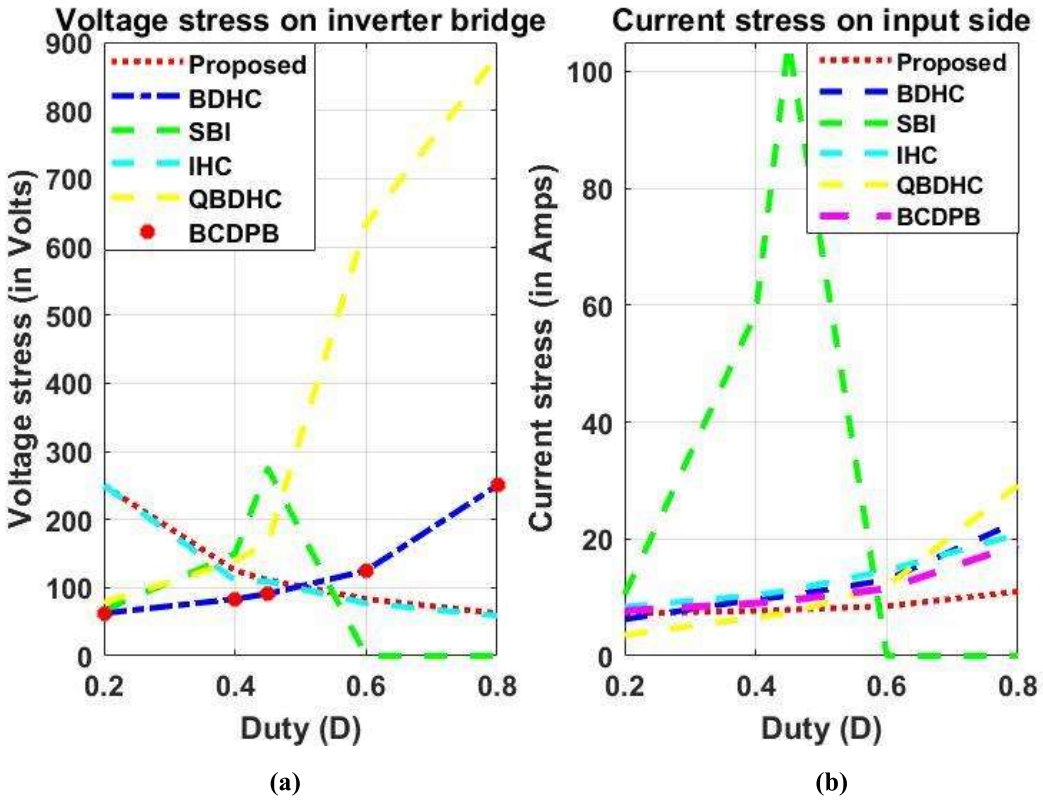


(b)

Fig. 3.7 Pole-zero plot of TLIHC **(a)** For D = 0.6 and **(b)** For D = 0.86 in zoom view.

3.4 Performance Analysis

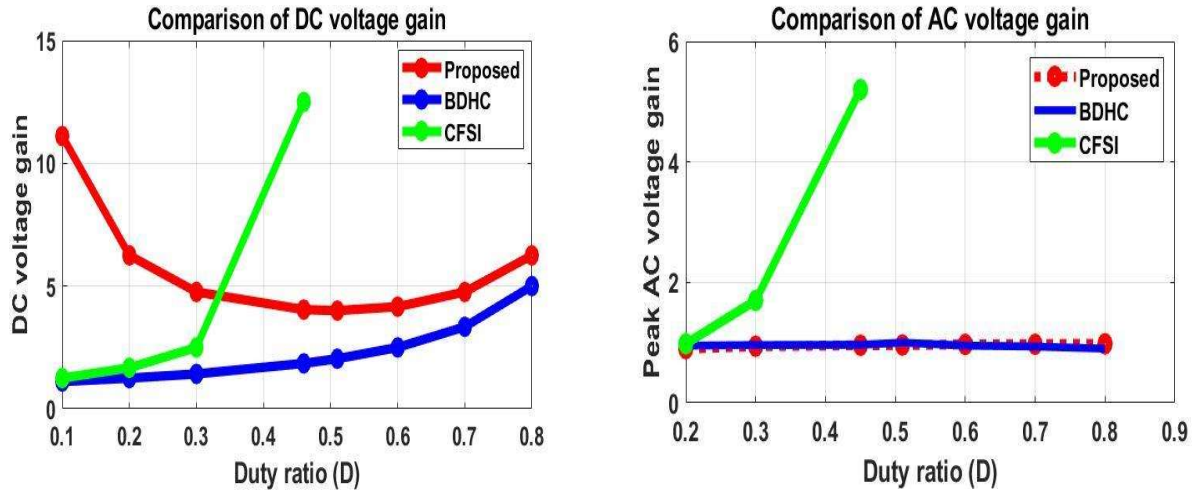
A comparison of voltage stress on inverter bridge among the proposed TLIHC and five other similar topologies is shown in Fig. 3.8 (a). It can be observed from Fig. 3.8 (a) that the proposed TLIHC has comparable voltage stress across the inverter bridge as compared to the interleaved hybrid converter (IHC). However, the voltage stress is lower in case of the proposed TLIHC as compared to the other reported hybrid topologies at higher duty ratio (D ≥ 0.5). Therefore, lower rated inverter switches are used in proposed TLIHC in comparison to other topologies. Fig. 3.8 (b) shows a comparison of current stress on the input side inductor among the proposed TLIHC and five other similar topologies. It can be observed from the Fig.3.8 (b) that the current stress on the input side/input side inductor is minimum in case of the proposed TLIHC. So, the core size and chances of core saturation is reduced in case of TLIHC. It can also be noticed that the maximum current stress is observed in case of the switched boost inverter (SBI), when it operates near to 0.5 duty ratio. In addition, it can be observed from Fig. 3.8 that the voltage stress of IHC is comparable with the proposed TLIHC. However, the input current stress is higher in case of IHC, when it is compared with the proposed TLIHC.



(a) **(b)**

Fig. 3.8 Comparison of **(a)** voltage stress on inverter bridge and **(b)** current stress on input side.

The comparison of DC voltage gain and AC voltage gain among the proposed TLIHC and other two similar topologies, boost derived hybrid converter (BDHC) [58] and current-fed switched inverter (CFSI) [57] are shown in Fig. 3.9. It can be concluded from Fig. 3.9 (a) that the proposed TLIHC has higher DC voltage gain as compared to BDHC and CFSI at lower and higher duty ratios (D). The CFSI has higher DC voltage gain, when it is operated at $0.35 \leq D \leq 0.5$. As the DC voltage gain of CFSI is $\frac{1}{1-2D}$, for the positive output voltage, the operating constraint is $D \leq 0.5$. Similarly, from Fig. 3.9 (b), it can be observed that the AC voltage gain of CFSI is more than that of BDHC and CFSI. The proposed TLIHC and BDHC have comparable AC voltage gain at all values of D. At the same time, the voltage stress on the DC switch of the proposed TLIHC is same as that of BDHC (i. e., $\frac{V_{in}}{1-D}$), whereas the voltage stress on the inverter bridge of the proposed TLIHC (i. e., $\frac{V_{in}}{D}$) is less as compared to BDHC and CFSI. In addition, one important operating constraint, in case of BDHC and CFSI is that $D + M_i \leq 1$. So, both D and M_i cannot increase simultaneously beyond 0.5.



(a) **(b)**

Fig. 3.9 Comparison of voltage gain. **(a)** DC voltage gain and **(b)** AC voltage gain.

Table 3.3 Performance Comparison Between TLIHC and TLMPHC

Features	TLIHC	TLMPHC
DC Voltage gain	$\frac{1}{D(1-D)}$	$\frac{1}{1-D}$
AC voltage gain	$\frac{M_i}{D}$	$\frac{M_i}{1-D}$
Voltage stress on boost converter switch	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$
Voltage stress on inverter bridge	$\frac{V_{in}}{D}$	$\frac{V_{in}}{1-D}$
Current stress on input side	$\frac{7-6D}{1-D} I_{DC}$	$I_{DC} + \frac{V_{DC}}{R_{AC}}$
No. controlled and uncontrolled devices	7 and 2	6 and 1

To summarize the advantages of the proposed TLIHC, a comparison between the proposed TLIHC and TLMPHC in terms of voltage gains, voltage and current stresses and number of controlled and uncontrolled semiconductor devices are given in Table 3.3. From Table 3.3, it can be observed that the DC voltage gain of TLIHC is more than that of TLMPHC by a factor of $\frac{1}{D}$. While, because of the presence of DC link capacitor, the voltage stress on the switches in case of TLIHC are same as that of TLMPHC. The AC voltage gain with wide operating range of M_i of TLIHC is comparable with that of TLMPHC. Further, the voltage stresses on the inverter bridge are less in case of TLIHC as compared to TLMPHC at higher D. Though the number of controlled and

uncontrolled devices are more in case of TLIHC, but the conduction period of one of the uncontrolled devices and two controlled devices are low.

During the shoot-through state operation of TLIHC and TLMPHC, as both the switches of either of the inverter bridge legs are in switch-on positions, the voltage stress on the inverter bridge during the period is zero. Similarly, current stress on the input side is the maximum current that flows in the input side. The maximum current flowing in the input side is during the shoot-through state.

3.5 Verifications of Steady-State Response

In this section, simulation and experimental verifications of steady-state response of both TLMPHC and TLIHC are discussed.

3.5.1 Simulation and Experimental Verifications of TLMPHC

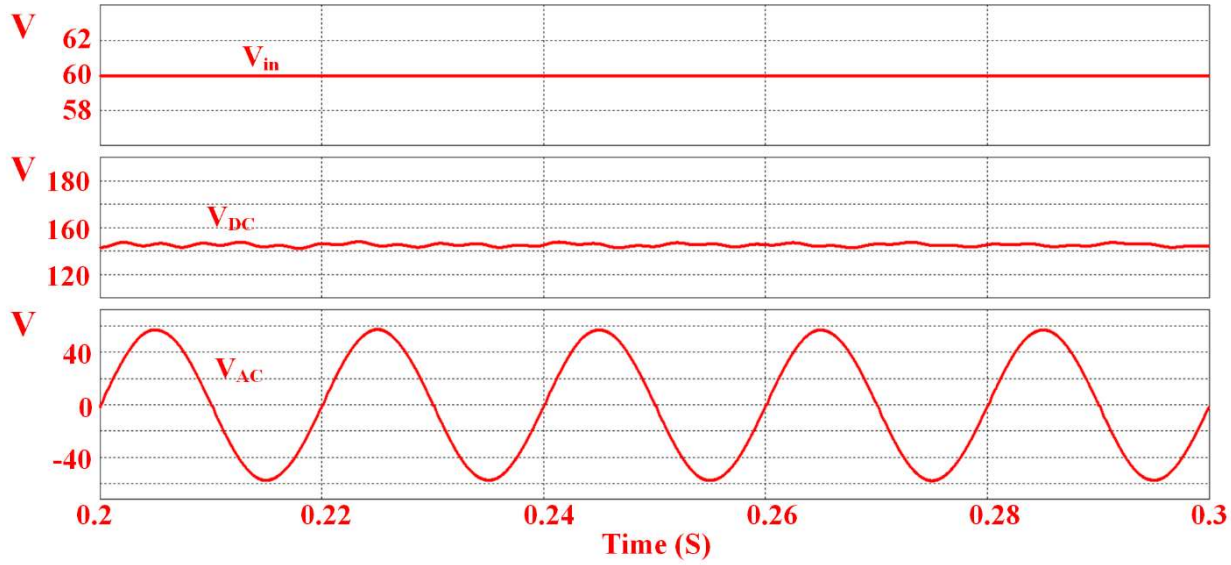
The performance of the proposed TLMPHC is verified through simulation and experimentation. The various operating parameters of TLMPHC and their attributes for both simulation and experimental studies are given in Table 3.4.

Table 3.4 Various Operating Parameters and Attributes of TLMPHC

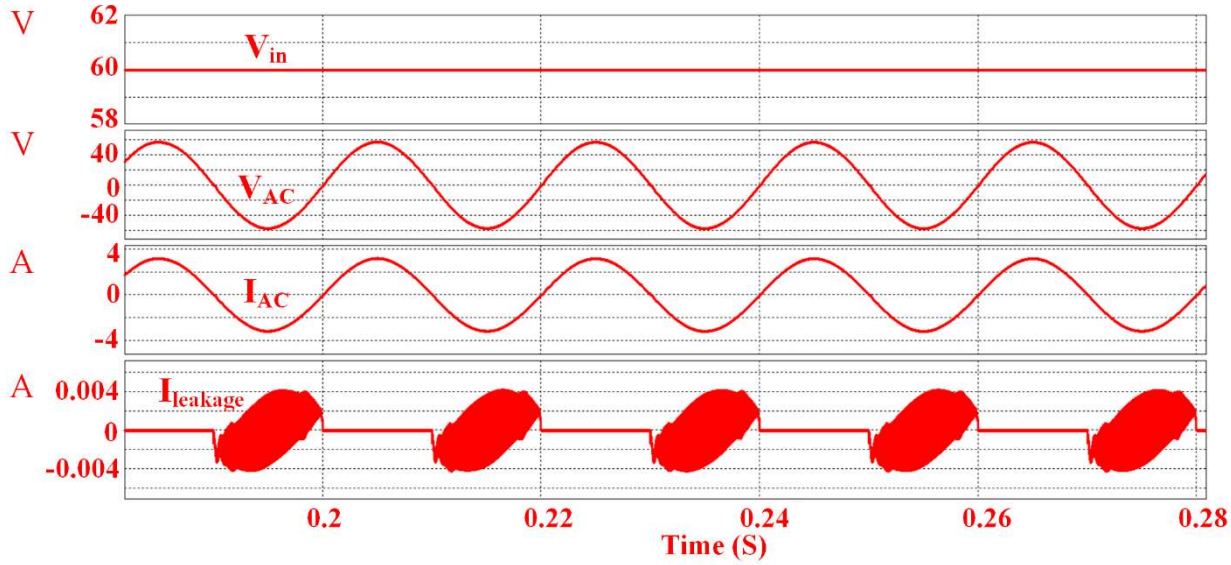
Parameters	Attributes
Input voltage (V_{in})	60 V
DC output power (P_{DC})	225 W
AC output power (P_{AC})	115 W
Duty ratio (D)	0.58
Modulation index (M_i)	0.4

The simulation results for steady-state operation of TLMPHC are shown in Fig. 3.10. From Fig. 3.10 (a), it can be noted that the DC output voltage (V_{DC}) = 142.85 V and AC output voltage (V_{AC}) = 40.53 V (rms value) for an input voltage V_{in} = 60 V. Fig. 3.10 (b) shows an AC output current

(I_{AC}) of 2.838 A (rms value) along with an average of 2 mA leakage current and AC output voltage (V_{AC}) of 40.53 V (rms value) for the same input voltage.



(a)



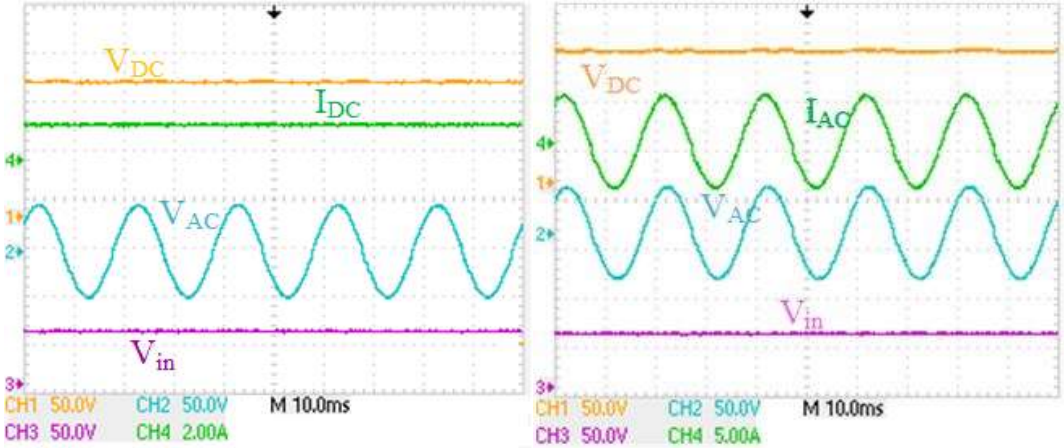
(b)

Fig. 3.10 Simulation results for steady-state operation of TLMPHC **(a)** V_{in}, V_{DC}, and V_{AC} and **(b)** V_{in}, V_{AC}, I_{AC}, and $I_{leakage}$. **[Y-axis has voltage/current values, having units "V" or "A"]**

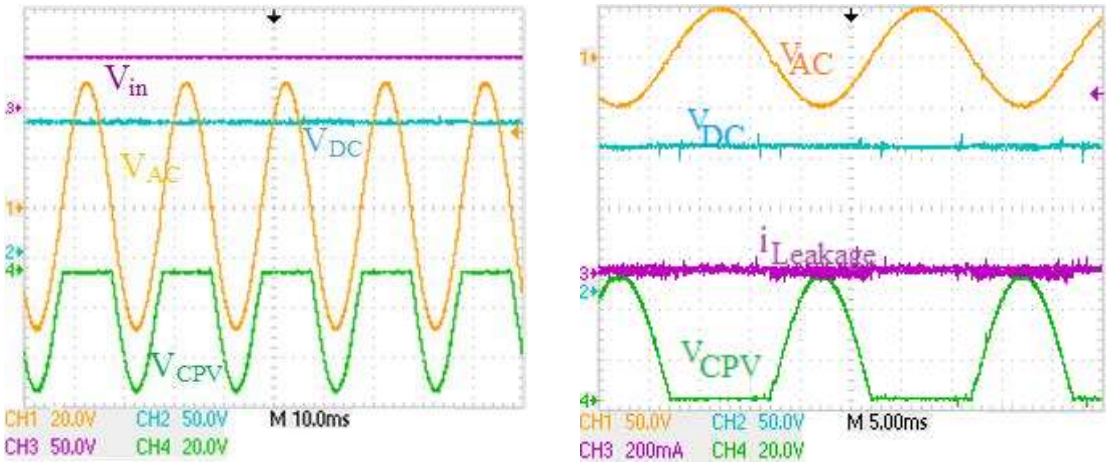
The photograph of the experimental set-up of the proposed TLMPHC is shown in Fig. 3.11. The experimental results of TLMPHC are shown in Fig. 3.12 and 3.13. Fig. 3.12 (a) shows the input DC voltage V_{in} = 60 V, output DC voltage V_{DC} = 143 V, fundamental AC output voltage V_{AC} (rms)

= 40.5 V and output DC current I_{DC} = 1.6 A. In Fig. 3.12 (b) output AC current I_{AC} (rms) = 2.838 A. The Fig. 3.12 (c) shows the voltage across the solar parasitic capacitor (V_{Cpv}), whereas Fig. 3.12 (d) shows the leakage current of TLMPHC. It can be observed that an average leakage current of 15 mA is circulating in the circuit. The current through filter inductor L_{f1} is observed in Fig. 3.13 (a) and it can be concluded that only during the positive half cycle, current is flowing through the filter inductor L_{f1}. Fig. 3.13 (b) shows the harmonic spectrum of AC output voltage. The measured value of the total harmonic distortion (THD) is 2.43 %.

Fig. 3.11 Photograph of the experimental set-up of TLMPHC

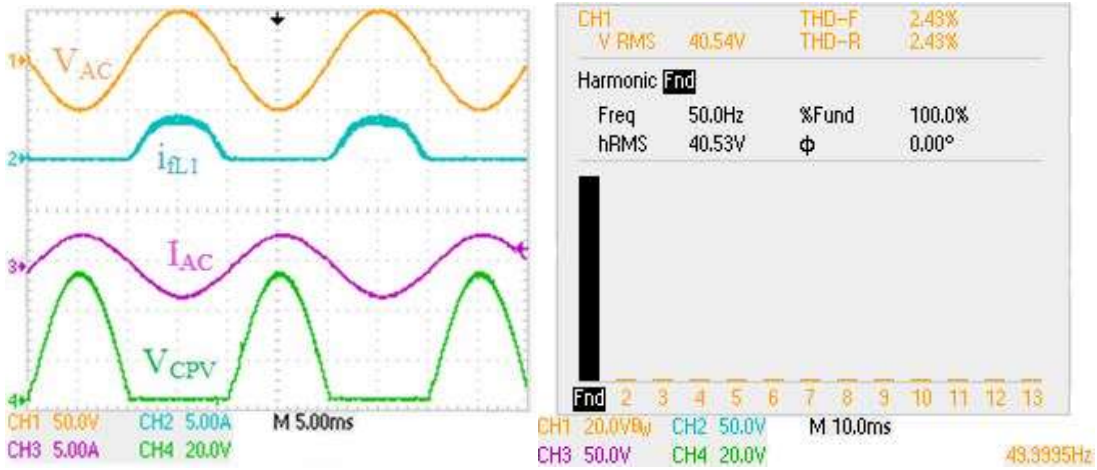


(a) **(b)**



(c) **(d)**

Fig. 3.12 Experimental results of TLMPHC for steady-state operation. **(a)** V_{in}, V_{DC}, V_{AC}, and I_{DC}, **(b)** V_{in}, V_{DC}, V_{AC}, and I_{AC}, **(c)** V_{in}, V_{DC}, V_{AC}, and V_{CPV} and **(d)** V_{DC}, V_{AC}, V_{CPV}, and $I_{leakage}$



(a) **(b)**

Fig. 3.13 Experimental results of TLMPHC **(a)** V_{AC}, V_{CPV}, I_{AC}, and I_{fL1} and **(b)** Harmonic spectrum of AC output voltage.

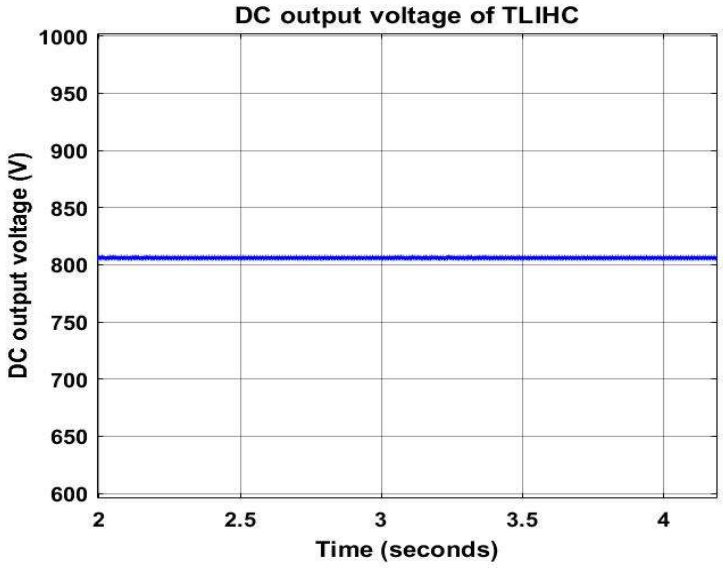
3.5.2 Simulation and Experimental Verifications of TLIHC

The various operating parameters of TLIHC and their attributes for simulation and experimental studies are given in Table 3.5.

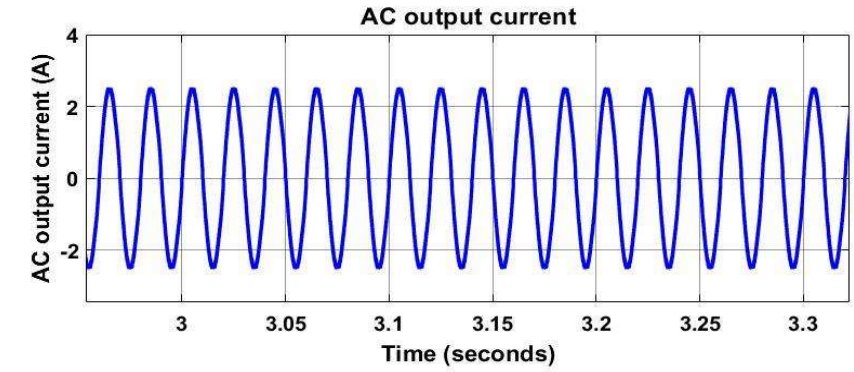
Table 3.5 List of Parameters and Attributes of TLIHC

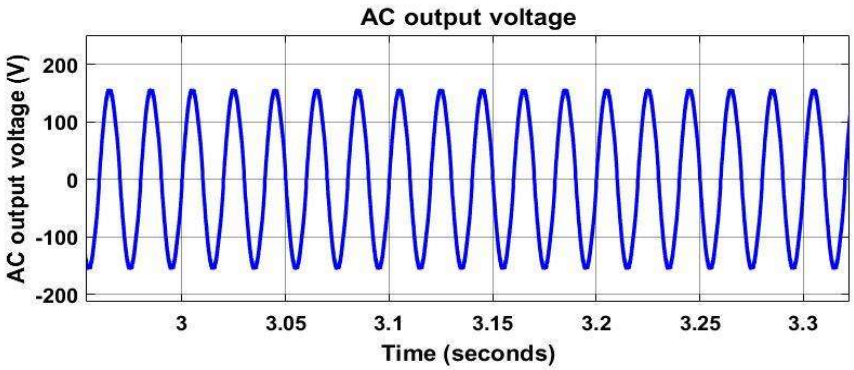
Parameter	**Attributes**
Power rating ($P_{DC} + P_{AC}$)	950 W
Input voltage (V_{in})	170 V
DC output voltage (V_{DC})	809 V
AC output voltage (V_{AC})	110 V (rms)
Switching frequency	50 kHz
Line frequency	50 Hz
DC Load (R_{DC})	800 Ω
AC Load (R_{AC})	60 Ω
Duty ratio (D) and modulation index (M_i)	0.7 and 0.638

The simulation results are shown in Fig. 3.14. From Fig. 3.14 (a) it can be observed that the DC output voltage V_{DC} = 1062 V for an input voltage V_{in} = 170 V and duty ratio D = 0.8. The AC output voltage V_{AC} = 127 V and AC output current I_{AC} = 4.7 A for the same input voltage as observed from Fig. 3.14 (b). However, Fig. 3.14 (c) shows the DC link capacitor voltage (V_C).

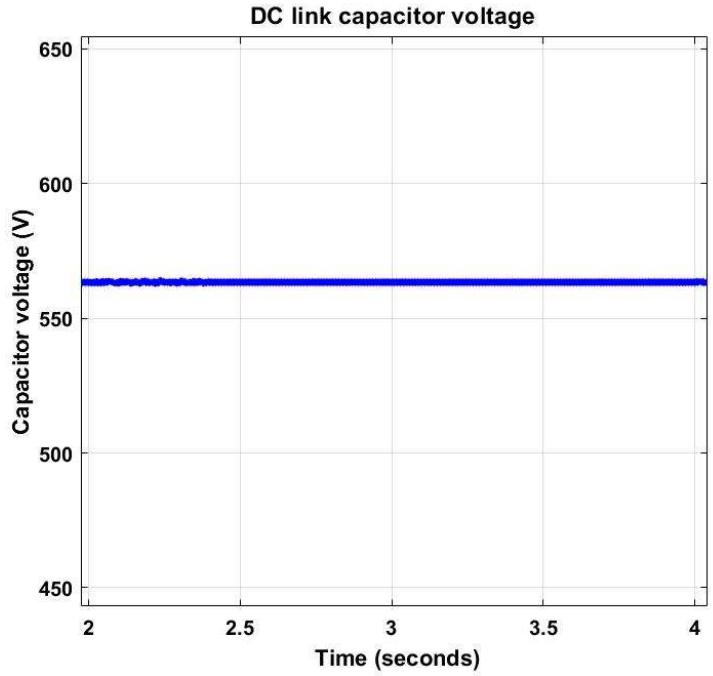


(a)





(b)



(c)

Fig. 3.14 Simulation results for steady-state operation of TLIHC. **(a)** DC output voltage (V_{DC}), **(b)** AC output voltage (V_{AC}) and AC output current (I_{AC}) and **(c)** DC link capacitor voltage (V_C).

The photograph of the experimental set-up of the proposed TLIHC is shown in Fig. 3.15. The experimental results of TLIHC are shown in Fig. 3.16, 3.17, 3.18 and 3.19. Fig. 3.16 (a) shows the output DC voltage $V_{DC} = 800$ V, fundamental AC output voltage V_{AC}(rms) = 110 V and input current I_{in}(avg) = 6.1 A for input voltage $V_{in} = 170$ V. Fig. 3.16 (b) shows output DC current $I_{DC} = 0.932$ A for the same values of V_{in}, V_{DC} and V_{AC}. Fig. 3.16 (c) shows the output AC current I_{AC}(rms) =1.84 A for the same voltage values. Fig. 3.16 (d) shows voltage across the parasitic capacitor (V_{Cpv}) and the leakage current ($I_{leakage}$) for the same voltage values of V_{in} and V_{AC}. The harmonic spectrum of AC output current is shown in Fig. 3.17. The steady state experimental results of the proposed TLIHC for two different sets of values of D and M_i are shown in Fig. 3.18. For $D = 0.5$ and $M_i = 0.4$, the steady state experimental result is given in Fig. 3.18 (a) where V_{in} = 170 V, V_{DC} = 680 V, V_{AC}(rms) = 96.5 V and I_{AC}(rms) = 1.82 A. Similarly, for $D = 0.83$ and $M_i = 0.77$, the steady state experimental results are given in Fig. 3.18 (b) (V_{in} = 130 V, V_{DC} = 920 V, V_{AC}(rms) = 85.6 V, and I_{AC} (rms) = 1.82 A.

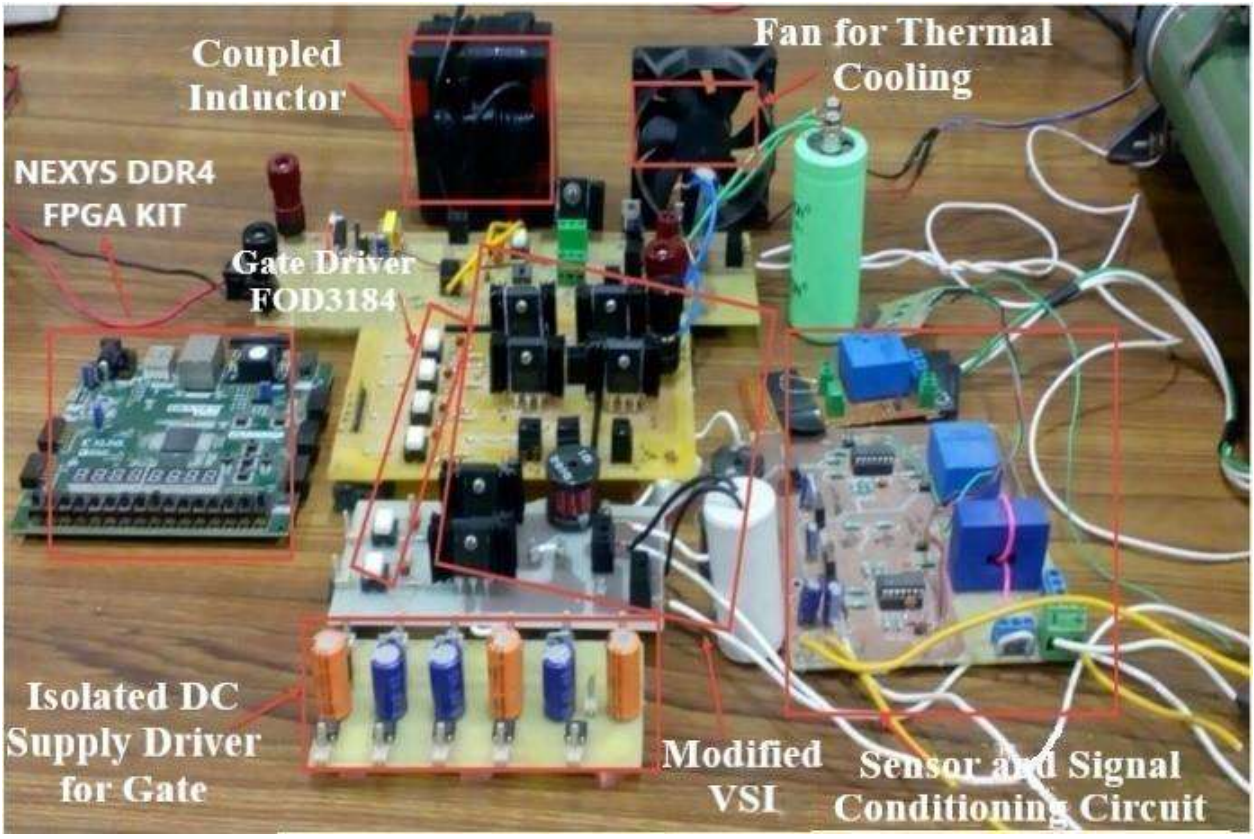


Fig. 3.15 Photograph of the experimental set-up of TLIHC.

Fig. 3.19 (a) shows the AC output current I_{AC}(rms) = 2.34 A at non-unity power factor load for the same values of V_{in}, V_{DC} and V_{AC}. From the Fig. 3.19 (a), it can be observed that the proposed TLIHC is operating at 0.88 lagging power factor. The harmonic spectrum of AC output current for non-unity power factor is shown in Fig. 3.19 (b). It is observed that the THD of unity and non-unity power factor load is found to be 1.71 % and 1.99 %, respectively.

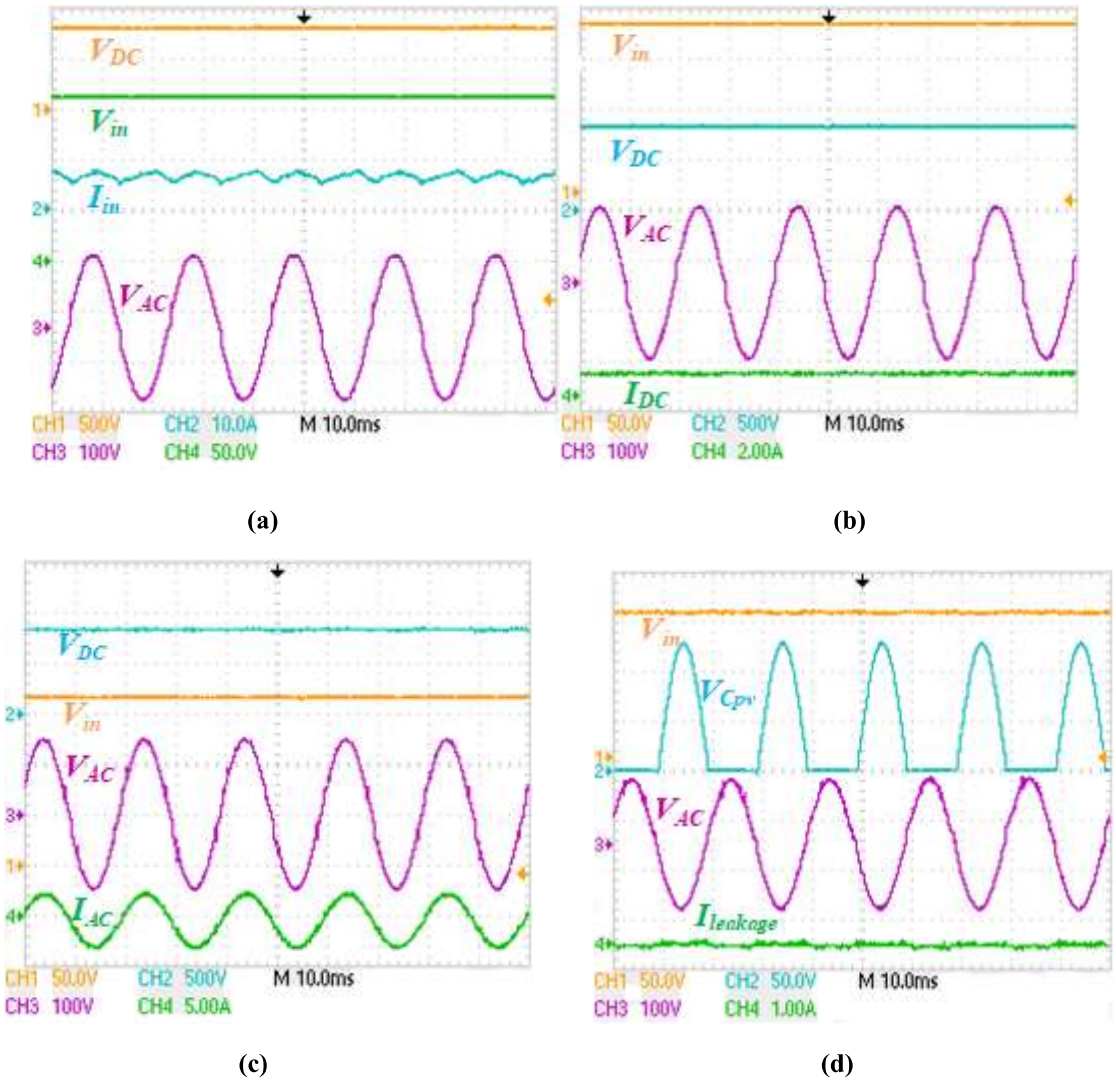


Fig. 3.16 Steady-state experimental results of the proposed TLIHC. **(a)** Input voltage V_{in}, output DC voltage V_{DC}, fundamental output AC voltage V_{AC} and input current I_{in}, **(b)** Output DC current I_{DC} along with V_{in}, V_{DC} and V_{AC}, **(c)** Output AC current I_{AC} along with V_{in}, V_{DC} and V_{AC} and **(d)** Common mode voltage (V_{Cpv}) across the PV parasitic capacitor (C_{pv}), common mode leakage current profile through the C_{pv} along with V_{in} and V_{AC}.

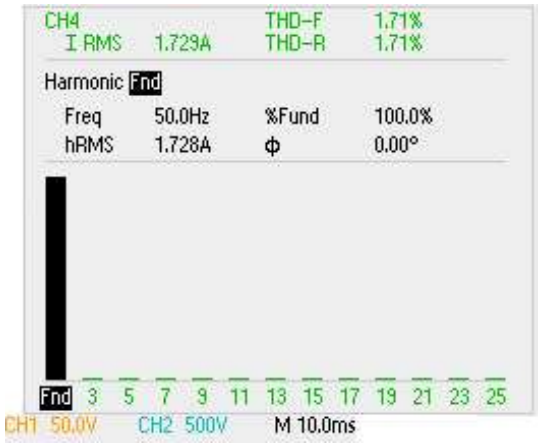
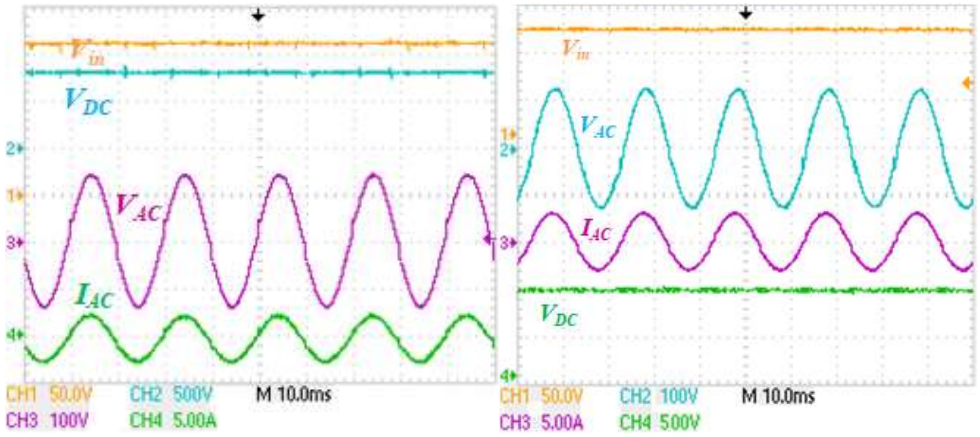
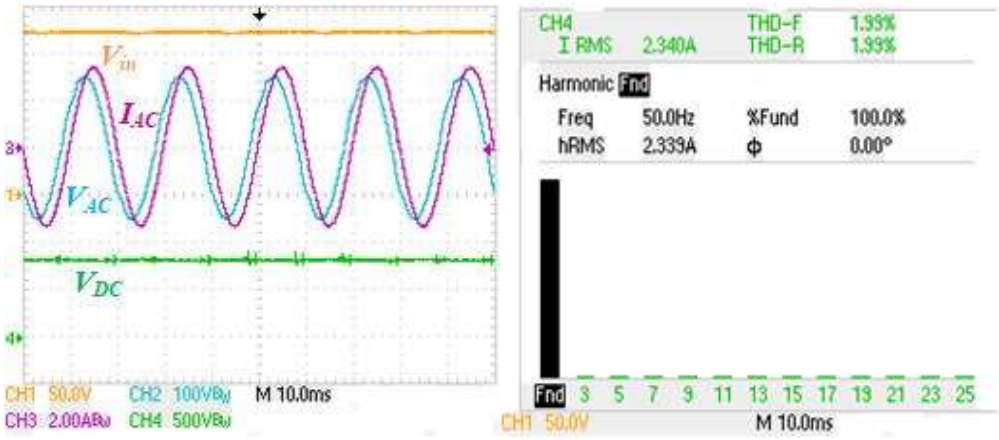


Fig. 3.17 Harmonic spectrum of output AC current of the proposed TLIHC.



(a) **(b)**

Fig. 3.18 Steady-state experimental result of the proposed TLIHC. **(a)** For $D = 0.5$ and $M_i = 0.4$ and **(b)** For $D = 0.83$ and $M_i = 0.77$.



(a) **(b)**

Fig.3.19 For non-unity power factor loading of the proposed TLIHC. **(a)** Output AC current I_{AC} along with V_{in}, V_{DC} and V_{AC} and **(b)** Harmonic spectrum of output AC current.

3.6 Loss Distribution and Efficiency Comparison

In this section, the loss distribution among the various components like power semiconductor devices and passive elements of both TLMPHC and TLIHC are discussed. Also, the efficiency comparison among the proposed TLIHC and other existing topologies are discussed.

3.6.1 Loss Distribution of TLMPHC

To calculate the power losses of TLMPHC; switches, diodes and elements used in the proposed hybrid converter is given in Table 3.6. The power losses are calculated based on the loss calculation equations [108]-[110].

Table 3.6 Components Used in TLMPHC

Switch (MOSFET)	Quantities	Parasitic capacitance (C_{ds})	Switched-on resistance (R_{sw})
IRFM360	4	500 µF	0.2 Ω
IRFP260N	2	442 µF	0.04 Ω
Diode	Quantities	On state resistance of diode (r_D)	
RURG8060	1	0.033 Ω	
C_d	1	470 µF (0.53 Ω)	
C_0	1	270 µF (0.6 Ω)	

1. *Losses in switches:*

The switching losses are calculated by using the expression

$$P_{switch} = f_s C_{ds} V_b^2 \tag{3.34}$$

where f_s is the switching frequency of the switch, C_{ds} is the parasitic capacitance between the drain and source terminals and V_b is the maximum blocking voltage of the switch.

The conduction losses of switches are calculated by using the expression

$$P_{cond\_sw} = I_{sw\,(max)}^2 R_{sw} D \tag{3.35}$$

where $I_{sw\,(max)}$ is the maximum value of current flowing through the switch, R_{sw} is the on-state resistance of the switch and D is the duty ratio of the switch.

The total loss in the switch is $P_{switch} + P_{cond\_sw}$

2. *Losses in diode:*

The conduction loss in the diode (D_1) is calculated as

$$P_{Cond\_D} = \frac{1}{T_s}\int_0^{T_s}(V_{FD}I_{D(avg)} + r_d I_{D(rms)}^2)dt \quad (3.36)$$

where V_{FD} is the forward voltage drop and I_D is the current through the diode.

3. *Losses in inductors:*

The winding resistance of the coupled inductor L_1 and L_1 are r_{L1} and r_{L2} respectively. The winding loss of the inductor depends on the inductor resistance. It is calculated as

$$P_{wind\_L} = r_L I_{L(rms)}^2 \quad (3.37)$$

4. *Losses in capacitors:*

In case of capacitors (C_d and C_0), the power loss depends on the equivalent series resistance of capacitors (r_{Cd} and r_{C0}). The loss in the capacitor is expressed as

$$P_{rC} = \frac{1}{T_s}\int_0^{T_s} r_C i_C^2 dt \quad (3.38)$$

The total loss in the TLMPHC is expressed as

$$P_{Total\_loss} = P_{sw} + P_{Cond\_sw} + P_{Cond\_D} + P_{wind\_L} + P_{rC} \quad (3.39)$$

The loss distribution among the elements of the proposed TLMPHC is shown in Fig. 3.20. The efficiency is calculated for D = 0.58, M_i = 0.4 and at the power level of 340 W, and the efficiency ($\eta = \frac{P_{output}}{P_{output} + P_{Total\_loss}}$) of TLMPHC is obtained as 89.6%.

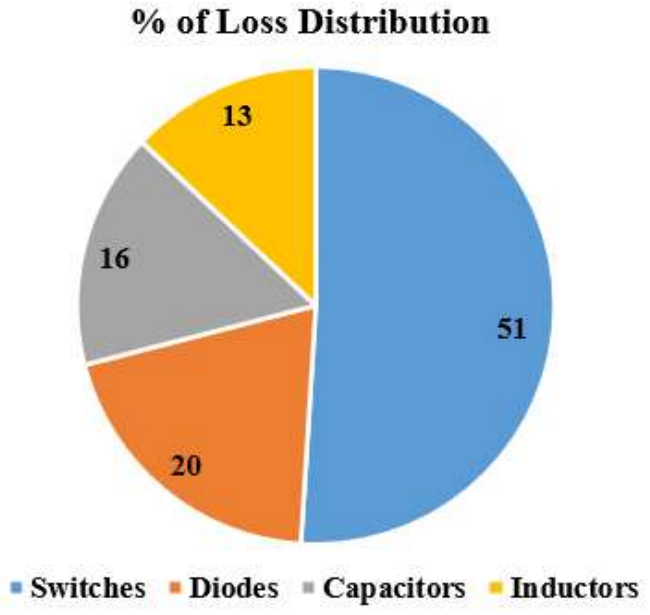


Fig. 3.20 Loss distribution among the elements of TLMPHC.

3.6.2 Loss Distribution of TLIHC

The power losses in the proposed TLIHC occurs due to the switching and conduction losses in power semiconductor devices and passive elements. Moreover, the power loss in the elements of TLIHC occurs mainly due to its operation in the power and shoot-through intervals. However, the power losses in the inverter bridge of TLIHC during the zero interval is negligible [109]-[112]. The power loss calculations in the proposed TLIHC are carried out at rated power by considering the non-idealities like: 1) dc resistance of inductors $r_{L1} = 320$ mΩ and $r_{L2} = 280$ mΩ, 2) equivalent series resistance of the capacitor $r_C = 300$ mΩ and 3) ON state saturation voltage and on state resistance of the power semiconductor devices. The power semiconductor devices used in the proposed TLIHC are listed in Table 3.7.

Table 3.7 Lists of Power Semiconductor Devices Used in TLIHC

Switch (MOSFET)	**Quantities**	**ON state saturation voltage ($V_{DS(on)}$)**	**ON state resistance (R_{sw})**
R6030KNX	1 (S)	3 V	0.13 Ω
IRFP360	4 ($S_1 - S_4$)	2 V	0.2 Ω
IRFP260N	2 (S_5 and S_6)	2 V	0.04 Ω
Diodes	**Quantities**	**ON state resistance of diode (r_D)**	**Forward voltage drops (V_{FD})**
RURG8060	1 (D_2)	0.033 Ω	1.34 V
RHRG30120	1 (D_1)	0.08 Ω	2.6 V

i. Losses in switches

Switching losses:

The switching loss of the proposed TLIHC is calculated as

$$P_{sw} = \frac{1}{2} V_s I_s \left(t_r + t_f\right) f_s \tag{3.40}$$

where V_s is the voltage stress on the switch, I_s is the current stress, t_r is the rise time, t_f is the fall time and f_s is the switching frequency of the switch.

The required current and voltage stresses for the calculation of switching loss in the H-bridge switches are given as follows:

$$\left.\begin{aligned} V_{inv} &= \frac{V_{in}}{D} \\ I_{inv} &= I_{L1} + I_{L2} \end{aligned}\right\} \tag{3.41}$$

where $I_{inv} = I_{ST} = I_{L1} + I_{L2}$, $I_{L2} = \frac{V_{in}}{R_{DC}D(1-D)^2}$ and $I_{L2} = \frac{V_{in}(R_{DC}D(1-D)+R_{eq})}{R_{eq}R_{DC}D(1-D)}$

The switching loss in the H-bridge switches is found to be 15.28 W.

The controlled switch (S) is in switch-on position only during the non-shoot through interval. Hence, the required current and voltage stresses for the calculation of switching loss in S can be written as follows:

$$\left.\begin{aligned} V_S &= \frac{V_{in}}{1-\mathrm{D}} \\ I_S &= I_{L1} \end{aligned}\right\} \tag{3.42}$$

The switching loss in the switch S is found to be 6.35 W.

The switching losses in the switches S_5 and S_6 are negligible as these two switches operate at lower frequency (50 Hz).

Further, as the switching loss depends on the voltage and current stresses of the switches and these stresses are less in the case of the proposed TLIHC, the switching loss is reduced. The total switching loss (P_{S_SW}) in the controlled switches (S and $S_1 - S_6$) of the proposed TLIHC is found to be 21.63 W. The switching loss in the controlled switches (S and $S_1 - S_6$) is shown in Fig. 3.21.

Conduction losses:

The conduction loss in the controlled switch S during entire switching cycle is given as

$$P_{con\_S} = I^2{}_{s\_max} r_{DS(on)} D + I_{S\_avg} V_{DS(on)} \tag{3.43}$$

where $r_{DS(on)}$ is the on-state resistance of the switch, $V_{DS(on)}$ is the drain to source voltage during switch-on condition and I_{S_avg} is the average current stress.

The conduction loss in the controlled switch S is found to be 11.2 W.

The conduction loss in the controlled switches ($S_1 - S_4$) during the shoot-through interval is calculated as

$$P_{con} = I^2{}_{rms} r_{DS(on)} + I_{avg} V_{DS(on)} \tag{3.44}$$

The required average and rms values of current for the calculation of conduction loss in the controlled switches ($S_1 - S_4$) during the shoot-through interval are given as follows:

$$\left.\begin{aligned} I_{avg\_STI} &= \frac{1}{T_{ac}}\int_0^{T_{ac}}(i_{L1}+i_{L2})\frac{1-D}{2}dt = (I_{L1}+I_{L2})\frac{1-D}{2} \\ I_{rms\_STI} &= \left(\frac{1}{T_{ac}}\int_0^{T_{ac}}(i_{L1}+i_{L2})^2\frac{1-D}{2}dt\right)^{\frac{1}{2}} \end{aligned}\right\} \quad (3.45)$$

The conduction loss in the controlled switches ($S_1 - S_4$) during the power interval is given as

$$P_{con\_(S_1-S_4)} = \frac{2}{\pi}\int_0^{\pi}\left[r_{DS(on)} \times i_{ac}^2 \times \frac{1+M_i}{2}\right] d\omega t \quad (3.46)$$

The total conduction loss in the controlled switches ($S_1 - S_4$) is 17.2 W.

Similarly, the conduction loss in the controlled switches S_5 and S_6 during the entire switching cycle is given as

$$P_{con\_(S_5\ and\ S_6)} = \frac{1}{\pi}\int_0^{\pi}\left[r_{DS(on)} \times i_{ac}^2\right] d\omega t \quad (3.47)$$

The total conduction loss in the controlled switches S_5 and S_6 is found to be 2.14 W.

The anti-parallel diode of switch S_4 is in the forward biased condition during the zero and shoot-through states of the positive half cycle, whereas the anti-parallel diode of switch S_2 is in the forward biased condition during the zero and shoot-through states of the negative half cycle. The conduction loss for the anti-parallel diodes is given as

$$P_{con\_anti\_D} = \frac{2}{\pi}\int_0^{\pi}[V_{SD} \times i_{ac}^2 \times (1-M_i)]\, d\omega t \quad (3.48)$$

The total conduction loss in the anti-parallel diodes is found to be 3.04 W.

As the number of switches in the conduction path is less during the power flow of the proposed TLIHC, the conduction loss is reduced. The total conduction loss (P_{S_con}) in the controlled switches (S and $S_1 - S_6$) of the proposed TLIHC is found to be 33.58 W. The conduction loss in the controlled switches (S and $S_1 - S_6$) is shown in Fig. 3.21.

ii. Losses in Diodes

Conduction losses:

The conduction losses in the diodes D_1 and D_2 can be calculated as

$$P_{D\_con} = V_{FD} * I_{D_{avg}} + I^2{}_{D\_rms} r_D \quad (3.49)$$

The required values of current for the calculation of conduction loss in the diodes are given as follows:

$$\left.\begin{array}{ll} i_{D1} = I_{L1} & DT_s < t < T_s; STI \\ i_{D2} = I_{L2} - I_{inv} & 0 < t < DT_s; nSTI \end{array}\right\} \quad (3.50)$$

The conduction losses in the diodes D_1 and D_2 are found to be $P_{D1\_con} = 4.1$ W and $P_{D2\_con} = 3.341$ W, respectively. The total conduction loss (P_{D_con}) in the diodes is shown in Fig. 3.21.

Switching losses:

The switching loss in the diodes D_1 and D_2 can be calculated as

$$P_{D\_swi} = 2 * f_{si} * Q_{rr} * V_D \quad (3.51)$$

where f_{si} can be expressed as $\frac{f_{tr}}{f_{AC}}$, where f_{tr} is the frequency of the carrier signal and f_{AC} is the frequency of the reference signal

The voltages across D_1 and D_2 are given as

$$\left.\begin{array}{c} V_{D1} = \frac{V_{in}}{D(1-D)} \\ V_{D2} = \frac{V_{in}}{D} \end{array}\right\} \quad (3.52)$$

The switching losses in the diodes D_1 and D_2 are found to be $P_{D1\_swi} = 4.3$ W and $P_{D2\_swi} = 0.51$ W, respectively. The total switching loss (P_{D_swi}) in the diodes is shown in Fig. 3.21.

iii. Losses in Passive Components

Losses in inductors:

According to the expression (3.36), the power loss in the inductor coils (L_1 and L_2) can be calculated and the required values of current for the calculation of power loss in the inductors are given as

$$\left.\begin{array}{l} I_{L1\_rms} = \left(\frac{1}{T_{ac}} \int_0^{2\pi} i^2{}_{L1}\, d(t) * d(wt)\right)^{\frac{1}{2}} \\ I_{L2\_rms} = \left(\frac{1}{T_{ac}} \int_0^{2\pi} i^2{}_{L2}\, d(t) * d(wt)\right)^{\frac{1}{2}} \end{array}\right\} \quad (3.53)$$

The power losses in the inductors (L_1 and L_2) are found to be $P_{L1} = 7.46$ W and $P_{L2} = 4.35$ W, respectively. The total power loss (P_L) in the inductors is shown in Fig. 3.21.

Losses in capacitor:

According to the expression (3.37), the power loss in the capacitor C can be calculated and the required value of current for the calculation of power loss in the capacitor is given as

$$i_c = \begin{cases} -(I_{L2} - I_{inv}) & 0 \le t \le DT_s \quad ; nSTI \\ I_{L1} & DT_s \le t \le T_s \quad ; STI \end{cases} \tag{3.54}$$

The power loss in the capacitor C is found to be $P_C = 6.72$ W and it is shown in Fig. 3.21.

The total power loss in the proposed TLIHC is 86.171 W. The efficiency of the proposed TLIHC is obtained from the equation, $\eta = \frac{P_{output}}{P_{output} + P_{Total\_loss}} = 91.06$ %.

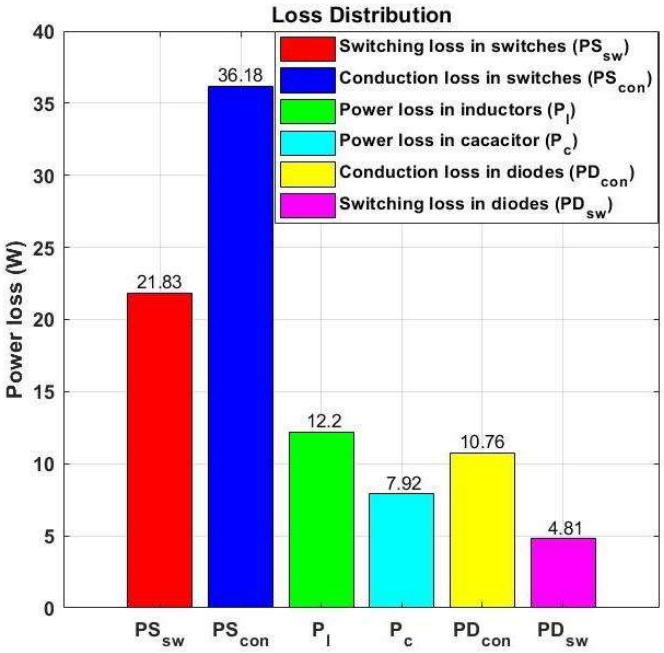


Fig. 3.21 Power loss distribution in the elements of the proposed TLIHC.

3.6.3 Efficiency Comparison

Fig. 3.22 shows the efficiency comparison among the proposed TLIHC and other existing topologies. It can be observed from Fig. 3.22 that the proposed TLIHC and the IHC have a better efficiency profile. But in case of IHC, the maximum efficiency is achieved at low power ratings. The two major losses (switching loss and conduction loss) which decide the efficiency are less in case of the proposed TLIHC. The proposed TLIHC has a better efficiency profile at higher power

ratings compared to other topologies. The maximum efficiency of the proposed TLIHC is 91.18 % at 980 W.

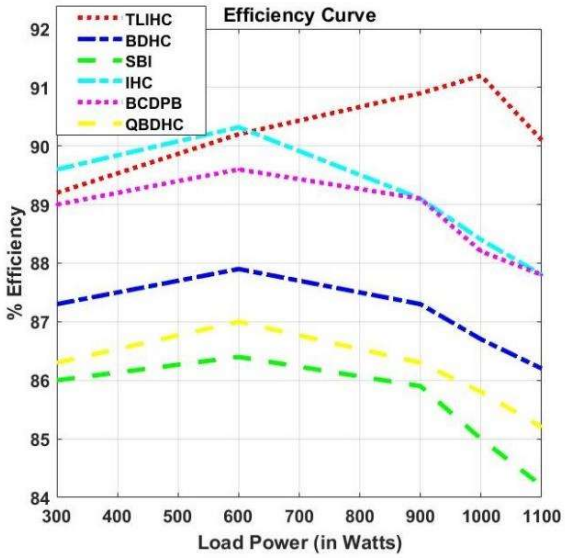


Fig. 3.22 Efficiency analysis at different loading conditions.

3.7 Limitations and Applications

Though the proposed TLIHC has few operating constraints, still it has some well-defined PV powered base applications depending upon the DC and AC voltage levels.

3.7.1 Limitations

The proposed TLIHC has some limitations in its circuit operation point of view which are as follows:

- Operating modes of the proposed TLIHC is broadly divided into two states (non-shoot through and shoot-through states). The non-shoot through state is again divided into two intervals (power interval and zero interval). As, both the power and zero intervals belong to non-shoot through state/interval, the duration of the power state is less than that of the non-shoot through state. Further, the duration of the non-shoot through state is decided by the duty ratio of the switch S, which is D of the proposed TLIHC. The duration of the power interval is decided by M_i. So, the limitation of the proposed TLIHC is that M_i must be less than D.

- In case of the proposed TLIHC, the DC link voltage/inverter input voltage (V_{inv}) is $V_{inv} = V_{DC} - V_C = \frac{V_{in}}{D}$ and AC output voltage $V_{AC}(pk) = M_i \frac{V_{in}}{D}$. So, at higher D, the AC output voltage decreases because of reduce in the DC link voltage.
- The DC voltage gain of the proposed TLIHC is $\frac{1}{D(1-D)}$. Higher DC gain is achieved, when TLIHC is operated either at $D < 0.4$ or $D > 0.6$.

3.7.2 Applications

The proposed TLIHC gives both DC and AC outputs simultaneously from a single DC input source. The AC output voltage of TLIHC (110 V rms value) is connected to the grid or it is directly utilized in home appliances (not recommended for highly inductive loads). According to the DC output voltage levels, TLIHC can be used for different applications such as

- When the DC output level is 750 V, it can be used in European railway electrification systems and modern tram systems. For this level of the DC output voltage, the input voltage (V_{in}) is 170 V, the duty ratio is 0.65 and the modulation index is 0.59.
- When the DC output voltage level is 1000 V, it can be used in insulation resistance testing.

3.8 Summary

In this chapter, mathematically modelling and analysis of both TLMPHC and TLIHC has been discussed in comprehensive manner. The minimum phase behaviour of the proposed TLIHC has been validated for the operating condition $0.61 < D \leq 0.85$, whereas the RHPZ is eliminated from the control-to-DC output voltage transfer function irrespective of any referral value of D in case of TLMPHC. Further, the simultaneous DC and AC outputs feature has been verified for both TLMPHC and TLIHC, where the $D + M_i \geq 1$ operating condition is only verified for TLIHC. In addition, as both TLMPHC and TLIHC achieves constant (zero) total common mode voltage during all the three operating intervals (power, zero and shoot-through intervals), the reduced common mode leakage current has been verified for both the cases. The quality of the AC output

current is improved in case of TLMPHC and TLIHC as the THD value is within the specified limits of IEEE standard. The power losses in the various elements of the proposed TLMPHC and TLIHC has been calculated to determine their efficiencies. A comparative study in terms of DC as well as AC voltage gain, voltage and current stresses and efficiency with other conventional hybrid converters has also been carried out in this chapter. Finally, the limitations and applications of the proposed TLIHC is presented in this chapter.