Chapter-2

Optimization of back ITO layer as the sandwiched reflector for exploiting longer wavelength lights in thin and flexible (30 μm) single junction c-Si solar cells

CHAPTER CONTENTS

2.1. Introduction:

Cost-effectiveness, reliability, and efficiency are the three most important factors that should go hand in hand to utilize solar photovoltaics over other renewable energy sources successfully. Nowadays, many reports can be found on perovskite, dye-sensitized, organic/polymer, inorganic-organic hybrid type advanced solar cells [124-127] with notably high efficiency and flexible structure in some cases. However, there are several predicaments regarding reliability which is restricting the significant commercialization of such cells. The other kind of solar cell mainly includes silicon-based technology. Conventional amorphous silicon (a-Si:H) cells are less expensive due to low material consumption and lower thermal budget [128-129]. However, light-induced degradation (LID) is a critically opposing factor for such cells [130-132]. The advanced variants of amorphous/crystalline solar cells like heterojunction with an intrinsic thin layer (HIT), interdigitated back contact (IBC), and passivated emitter rear cell (PERC) [133-135] include a very complicated process flow involving multi-layer of the both amorphous and crystalline form of silicon and so, yet to get popularity for wide commercialization. For these reasons, thick (~180 μm) wafer-based single-junction monocrystalline or multi-crystalline solar cells hold the lion's share of the PV industry to date. There are some challenges too in conventional ~180 μm silicon cell technology that should deal with proper care to make solar PV a prime source for renewable energy. The high capital cost, excessively thick absorber layer, and lack of flexibility in the device structure make it less attractive for future technologies. However, the reliability factor, in this case, is notably higher than the other form of solar cells. *Shockley* reported [136,137] that a ~30 μm thick c-Si wafer is sufficient to fabricate single-junction solar cells. This encouraged a group of researchers to develop new technologies for thin crystalline amorphous kinds of solar cells with both homo and

heterojunctions. Interesting work has been reported by *Wang* et al. on steel-supported thin silicon solar cells grown by reduced pressure chemical vapor deposition (RPCVD) that yielded 16.2% efficiency [138]. The Interuniversity Microelectronics Centre (IMEC) of Belgium has recently reported around 16% efficient epitaxially grown ~30 µm silicon solar cells [139]. Many PV industries like Solexel, Crystal Solar, Amberwave, and Astrowatt, to name a few, have reported some benchmark efficiency on thin silicon solar cells fabricated using epitaxial and exfoliation techniques [110-144]. Very recently, Lee et al. reported ~50 µm thick "kerfless" wafer-based solar cells with 15.2% efficiency [145]. Using a porous silicon layer transfer process, *Petermann* et al. fabricated a ~43 µm thick epitaxially grown silicon solar cell that resulted in 19% efficiency [146]. Fabrication of silicon micro-cells is another attractive pathway toward the development of high-efficiency thin silicon cells. Yao et al. fabricated an assembly of silicon micro-cells by micromachining of Si (111) wafers which came out with the best efficiency of 11.7% under AM 1.5D radiation [147]. However, to date, there are limited references on such single junction (homo-junction) crystalline wafer-based solar cells with a notable conversion efficiency that can go in line with mainstream fabrication flow lines. On the other hand, in 2019, the international technology roadmap for photovoltaic (ITRPV) predicted that there would be a considerable lowering in the substrate thickness for wafer-based mono- and multi-crystalline solar cells within 2029. Here, we have started with an extreme case, i.e., ~30 µm wafer thickness. In an attempt to achieve the sweet point of these four factors, viz. cost-effectiveness, reliability, efficiency, and device flexibility, this work has been taken as a pilot scheme to make a single junction c-Si solar cell prototype based on ~30 µm wafer obtained by scaling down technique due to the lack of commercially available thin wafers. A thirty (30) micrometer (µm) thin c-Si wafer is known to pass through a portion of light in the

longer wavelengths (>700 nm) owing to the fact of its absorption coefficient in the order 10^3/cm at this point [148,149]. So, a thin indium tin oxide (ITO) layer has been introduced in between the aluminum back contact and p-Si layer for proper management of lights with longer wavelengths [150] as well as to block the dangling bonds on the silicon surface to minimize the defects. The efficiency of the cell and the role of thickness has been studied thoroughly and validated through theoretical modeling. Starting with the primary p-n junction device, four solar cell devices with different architecture were fabricated in batches using the thin (~30 μm) wafer for stepwise improvement of efficiency. If a solar cell can be made using $1/6^{th}$ of the material than the conventional system without compromising much with reliability and efficiency, a drastic cost reduction can be expected along with the additional advantage of the flexibility of the device. This will also help us to adhere to the ITRPV predictions. The present report has the following thrust areas: (i) to develop thin c-Si wafer-based single-junction solar cells with a flexible structure to facilitate the concept of future roll-to-roll electronics, (ii) to propose some optical management that is required to overcome the light losses (mainly longer wavelengths) in thin wafers without compromising with the conventional Al BSF structure, and (iii) the entire cell fabrication technique should be in-line with presently available fabrication technology for the ease of commercialization.

2.2 Materials and methods:

2.2.1. Device fabrication:

Commercially available (Just Solar, China) p-type and ~180 μm thick <100> monocrystalline Si wafers were taken to produce 30 μm wafers by scaling down technique through alkali etching. 3-inch × 3-inch of such wafers were vertically

mounted in a beaker containing 10% aqueous AR grade NaOH solution at a temperature of 85°C and quickly removed after 55 minutes and washed thoroughly with deionized water followed by isopropanol. This gives a ~30 µm thin c-Si substrate. Improvement in throughput will be achieved by developing and commercializing a proper technique for the fabrication of thin silicon wafers, which is not covered in the present discussion. For a systematic analysis, cells with four different structures have been fabricated as shown in Fig.2.1.

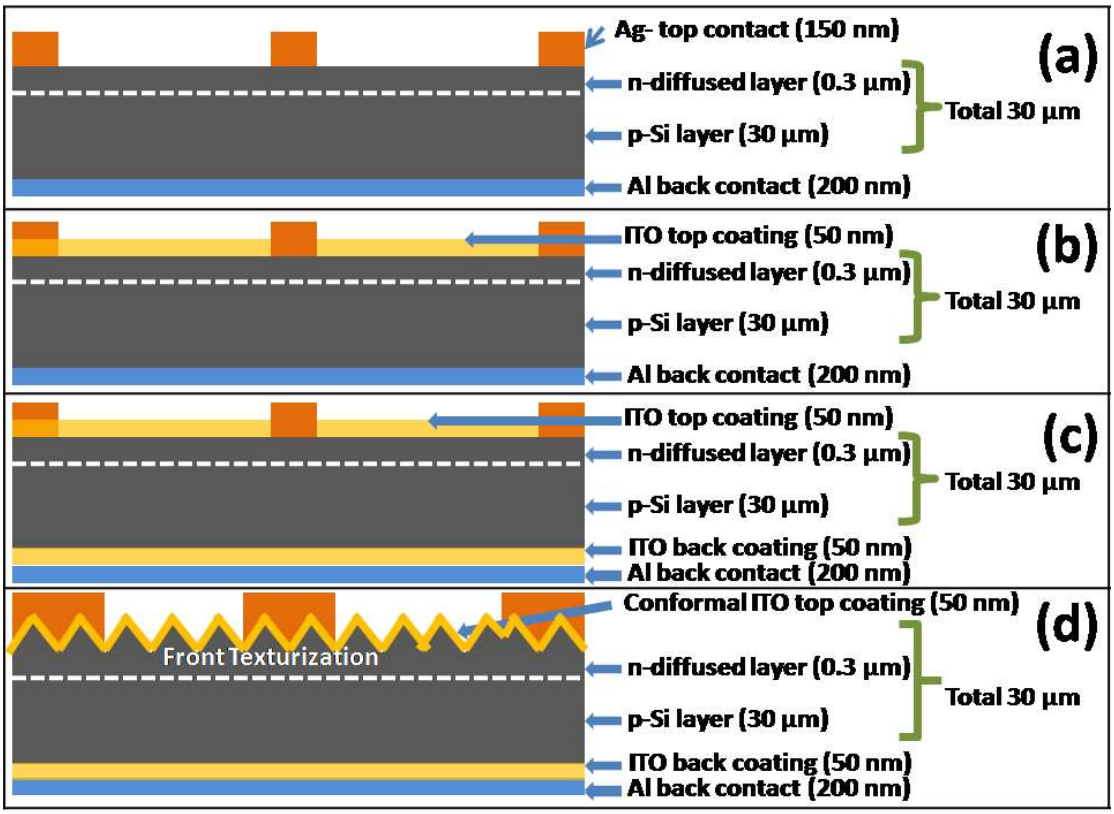

Fig.2.1: Structures adopted for fabricating the 30 µm wafer-based solar cells starting from the basic p-n junction.

These cells will be referred to as “Cell 1”, “Cell 2”, “Cell 3” and “Cell 4” hereafter. Each structure was treated with different conditions for in-depth study and condition optimization. The final cells with top “e-mask” and bottom metal contacts were fabricated on a 1 cm × 1 cm area. Flexibility with nearly 120° and 90º bending angles were gained for 3-inch × 3-inch wafers and 1 cm × 1 cm finished cells,

respectively. The metallic Al support on the back case gives an advantage in this. The following steps were adopted to fabricate the cells:

Step 1: One side of the wafer was coated with 85 – 90 nm SiN_x layer in a plasma-enhanced chemical vapor deposition (PECVD) chamber under 1 torr pressure, 400°C temperature, RF 30 watt power for 10 minutes with a gas flow (sccm) ratio of 45:45:65 for NH_3:H_2:SiH_4. This was done to restrict both side diffusion and removed after the diffusion process is over. The n-diffusion in the thin p-type wafer was done using the following standard recipe:

Initially, the furnace temperature was raised to 700°C in 1 hour followed by loading of the thin wafers (10 numbers, back-to-back) at a nitrogen flow of 6 standard liters per minute (SLPM) and the temperature was again raised to 810°C and a stabilization time of 10 minutes was provided. Pre-deposition was initiated at this temperature with 10 SLPM nitrogen flow, followed by 0.5 SLPM flow for both oxygen and $POCl_3$. The treatment time was 20 minutes. Further ramping up of temperature to 830°C was done and after 5 minutes of stabilization, nitrogen and oxygen were introduced at a flow rate of 10 SLPM. The temperature ramps down from 830 to 800°C was carried out for 20 minutes at an exhaust pressure of 14 Pa followed by low-temperature oxidation at 8 SLPM flow of oxygen for 15 minutes. Further ramp down of temperature 800 to 700°C was done at 6 SLPM of nitrogen flow followed by sample unloading. Finally, the SiN_x coating was removed by treating with 10% HF solution at room temperature for 5 minutes.

Step 2: Each wafer was cut into approximately 10 mm × 10 mm small units using Nd:YAG laser (λ = 1064 nm) and top metallic Ag contacts were taken on the n-side using ‘E-mask’ through thermal evaporation at 150°C. The contact thickness was 150 nm.

Step 3: Firing of the samples was done in a three-zone belt furnace with a temperature profile 450°C/650°C/750°C with a belt speed of 3900 mm/minute.

Step 4: A 50 nm thick layer of indium tin oxide (ITO, SnO_2:In = 90:10) on the n-side and upon the 'E-mask' was deposited using RF sputtering (base pressure: 3.5×10^{-5} mbar, process pressure: 2.0×10^{-5} mbar, temperature: 180°C, Ar:O_2 = 99:1 sccm, deposition rate: 3.5 nm/minute, pulsed DC mode at 330 V, frequency: 5 kHz, duty cycle: 50% and target to source distance: 6 cm), aiming to the enhancement of front current collection as well as anti-reflection purpose. As this ITO layer was deposited on the emitter side at an elevated temperature, the sheet resistance was found to be 10 – 12 Ω/sq.

Step 5: On a batch of a sample, on the p-side of the diffused wafers, ITO layers with three different thicknesses; viz. 50, 100, and 150 nm were deposited to improve the back carrier collection using the same RF sputtering technique.

Step 6: Finally, a 200 nm thick metallic Al layer was deposited on the back ITO layer using the thermal evaporation technique to make the back contact. The process temperature was 150°C. After going through this step, the sheet resistance of the top 50 nm thick ITO layer becomes 6 – 8 Ω/sq.

There are two conventional ways to make contacts from the emitter side of diffused emitter solar cells: (i) by screen printing and co-firing and (ii) metal deposition by shadow masking. For screen printing and co-firing, the fingers and busbars can penetrate through the emitter layer and result in good ohmic contact. For shadow masking (the case here), the chances of penetration of the evaporated metal contacts through the emitter layer is less than the screen printing technique. On the other hand, generally, the gap between the fingers of the e-mask is higher than the gaps between the

fingers of screen-printed contacts. So, to have good ohmic contact and better carrier collection from the entire emitter surface, ITO coating has been done. This ITO layer also gives additional advantages like anti-reflection from the top and dangling bond blocking effects.

2.2.2. Characterization:

Topographical and cross-sectional image of the thin wafer was captured using a field emission scanning electron microscope (FESEM, JEOL JSM 7610F operated at 15.0 KV and secondary electron imaging mode). Atomic force microscopy (AFM) was done using a NT-MDT Solver Next atomic force microscope within 100 nm × 100 nm scan area and 0.5 Hz scan speed. The crystallographic parameters were evaluated using a Bruker D8 X-ray diffractometer (XRD) with Bragg-Brentano goniometer, θ-2θ scanning mechanism within 20 to 80 degrees with a scan rate of 0.5 degrees/sec and Cu K_α radiation source. Optical reflectance was measured using a Bentham PVE-300 Series spectral response unit. The current density–voltage (J–V) characteristics were measured with the help of a Cell Tester CT-50AAA from PET, California, USA. Both reflectance and J–V characteristics were measured under AM 1.5G simulated radiation. COMSOL® 5.0 Multiphysics was used to validate light management-related phenomena in the back ITO layer.

2.3. Results and discussions:

2.3.1. Structural properties of thin wafers:

The thickness of the wafer after scaling down was established by taking a cross-sectional micrograph which is presented in Fig.2.2a. This indicates the formation of uniform ~30 μm wafer by alkali etching (indicated between two arrows in Fig.2.2a). A topographical atomic force microscopic (AFM) image at high resolution (100 nm×100 nm) was also captured (Fig.2.2b) to check for any deformities that might be present in

the surface, and interestingly, it has been found that the surface of the thin wafer does not contain any pinholes, cavities or cracks. The average roughness was about 8.8 nm, which is also indicating to a surface that does not contain any major structural deformities/variations. These facts make the post-etched wafer acceptable for device fabrication.

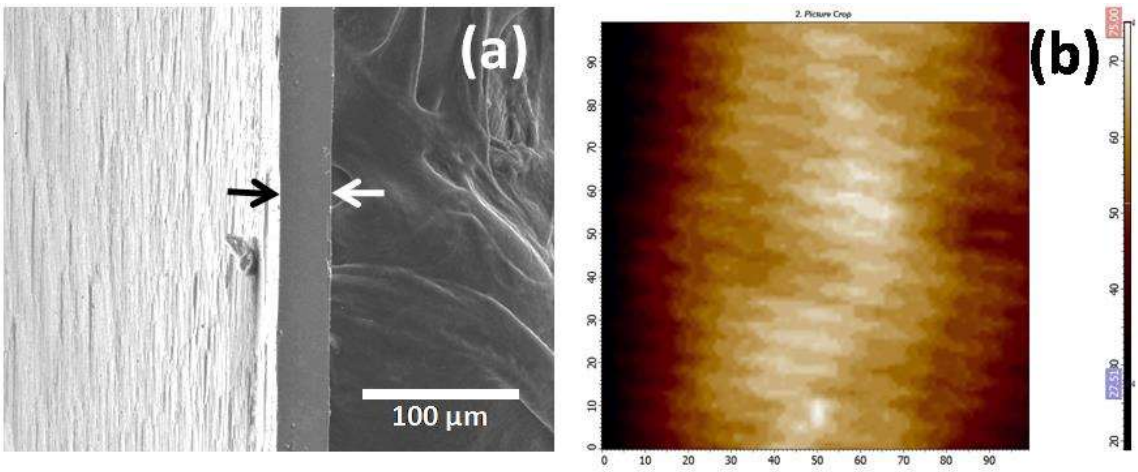

Fig.2.2: (a) cross-sectional SEM image of the thin wafer showing the thickness and (b) AFM image of the post-etched silicon wafer.

X-ray diffraction (XRD) analysis with both thick (~180 µm) and thin (~30 µm) monocrystalline p-type Si was carried out to check the presence of any detrimental change in the crystallographic parameter that might take place during the alkali etching. Fig.2.3a and 2.3b are representing the small-angle XRD patterns of thick and thin Si wafers without n-diffusion, respectively. Only one major diffraction from the <400> plane was observed in all cases (Fig.2.3) indicating the monocrystalline nature of the substrate. It is evident from Fig.2.3a and 2.3b that, a slight increase in full width at half maximum (FWHM or β) value occurs after thinning the sample with a 0.08-degree shifting of the peak center (69.10° to 69.18°) to the higher 2θ region. The FWHM was found to increase by an amount of 0.06 (from 69.07° to 69.13° in 2θ) after thinning the sample that indicates the formation of defects in the wafer with lowering the thickness.

The defect density in both thick and thin wafers was calculated using the standard equation $D = (\beta^2/9b^2)$, where D is the defect density, β is the FWHM and 'b' is the Burger vector for Si, i.e. 3.83×10^{-10}. Using this equation, the ratio of defect density in a thin and thick silicon

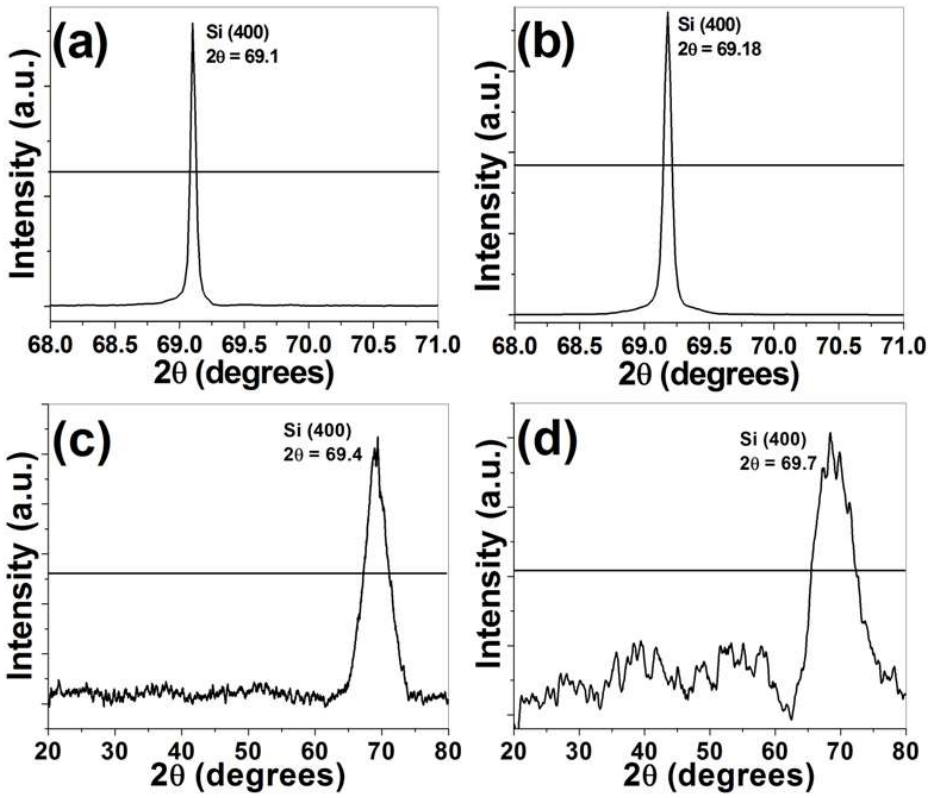

Fig.2.3: XRD pattern of (a) undiffused 180 μm monocrystalline p-type wafer (b) undiffused 30 μm wafer (c) n-diffused 180 μm wafer from n-side and (d) n-diffused 30 μm wafer from n-side.

wafers were estimated to be 1.77. This means, that after scaling down the wafer thickness to ~30 μm from 180 μm, the defect level increases by 1.77 times, which may not be a factor for all practical purposes. This, in turn, indicates that the defect level-related trapping/recombination of the photogenerated charge carriers in a thin wafer will be almost like that of a thick wafer. The value for microstrain (ε), which is another important parameter for device reliability, was calculated using the equation $\varepsilon = (\beta\text{Cos}\theta)/4$, and was found to be 8.62×10^{-4} and 1.14×10^{-3} for the thick and thin wafers,

respectively. This means, there was a 1.33 times increase in microstrain inside the material after thinning it, which is also not so significant. This once again makes the ~30 μm wafer a good competitor of the ~180 μm wafer from the crystallographic point of view. It is also understood that incorporation of dopants (either p or n) in material increases the defects levels and this is reflected in the broadening of the FWHM of the characteristics diffraction peak(s). In this case (Fig.2.3c and 2.3d), after n-diffusion in the p-wafer, a notable broadening in the FWHM of the characteristics <400> peak of both thick and thin wafers was noticed and the broadening in the thin wafer (FWHM = 6.84 in 2θ) was higher than that of the thick wafer (FWHM = 3.90 in 2θ). Thus, the enhancement in defect density in thin wafer after n-diffusion was 3.07 times higher than that of n-diffused thick p-wafer. Under the same condition of n-diffusion, the enhancement of defect density in the thick wafer was 4.225×10^3 times than the undoped condition, and the same after n-diffusion in the thin wafer was 7.310×10^3 times. This indicates facile diffusion in the ~30 μm wafer.

2.3.2. Optical properties of the thin wafers:

Reflectance measurements were carried out with the thick, thin, and n-diffused thin wafers to investigate any reflectance-related optical loss that wafers might undergo during the scaling down and diffusion process. The reflectance spectra for the thick (as cut) and thin monocrystalline p-type wafers along with the n-diffused thin wafer are shown in Fig.2.4. The reflectance pattern (within 400 – 1100 nm) obtained from all three substrates is typical, showing no significant change after scaling down of the thickness and/or after diffusion. As the scaling down, in this case, was achieved by alkali etching, there might be a chance of getting a polished surface and that might lead to reflectance enhancement and subsequent photon loss.

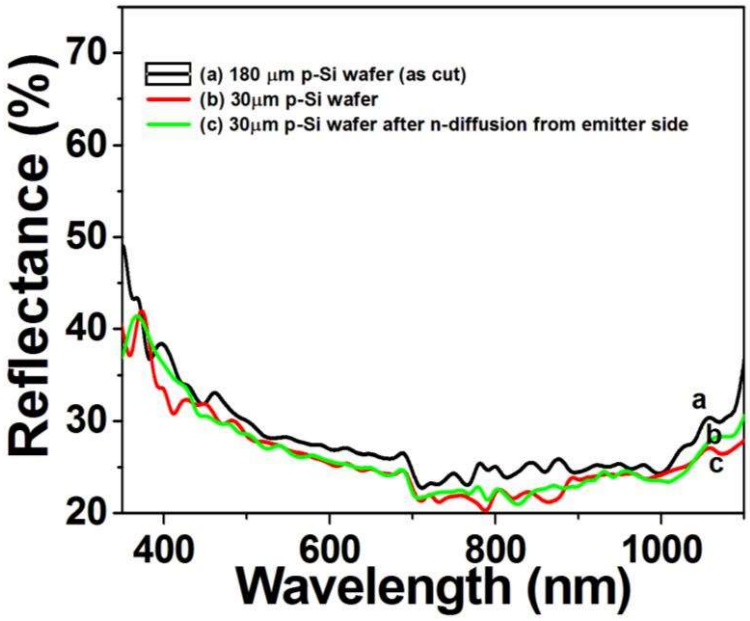

Fig.2.4: Reflectance spectrum of (a) as cut 180 μm wafer (b) 30 μm wafer and (c) n-diffused 30 μm wafer from n-side.

However, the observation, in this case, is encouraging, making the ~30 μm wafer competitive with ~180 μm from the point of view of reflectance from the surface. The structural, crystallographic, and optical analyses are providing enough points in favor of the ~30 μm wafer to make a single-junction solar photovoltaic device using it.

2.3.3. Current-voltage characteristics:

The work initiated with the formation of a primitive p-n junction cell by taking the ~30 μm wafer and n-diffusion within it with Ag top contact and 200 nm thick Al back contact, as mentioned in Section 2.1. This has been described as "Cell 1" and the related current density – voltage (J–V) curves are presented in Fig.2.5. The efficiency of this cell was extremely poor (0.29%) and the J–V curve is presented as curve 'a' in Fig.2.5. However, when the cell was annealed in air at 600°C for 10 minutes, an increase in efficiency to 0.91% was observed (curve 'b') with a notable rise in V_{oc} but a lowering in J_{sc}.

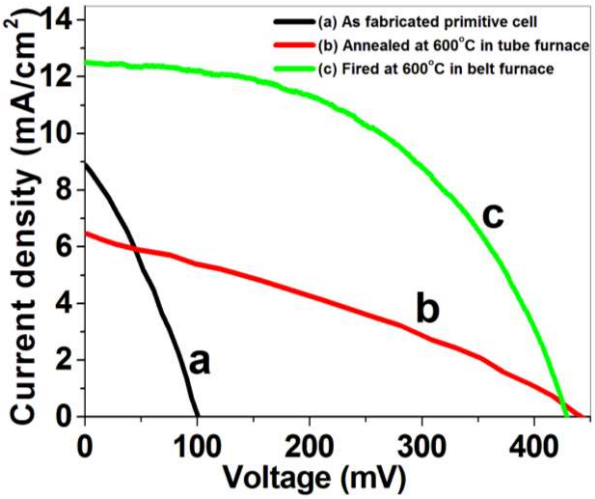

Fig.2.5: J – V characteristics of "Cell 1" and its variants: (a) primitive cell (b) after annealing in air at 600°C for 10 minutes and (c) primitive cell after firing in belt furnace at 600°C.

This means, by thermal treatment better junction formation took place owing to the formation of a back p^+ layer caused by the diffusion of Al^{3+} ions from Al back contact to p-Si. But there were some problems with the carrier collection from either end of the device. This might be attributed to the formation of insulating Al_2O_3 at the back due to prolonged annealing in air at elevated temperatures [151,152]. To avoid this, a newly fabricated primitive cell was fired in a firing furnace to give a thermal shock (rather than annealing) with the conditions as mentioned in Section 2.2.1. The outcome was promising in this case, which has been reflected in an increase in both V_{oc} and J_{sc} than the primitive cell leading to a conversion efficiency of 2.68% (curve 'c' in Fig.2.5). This indicates, good junction formation along with better carrier collection from both the contacts can be achieved by providing a thermal shock to this thin device and a 200 nm thick Al back contact is sufficient for that. Due to the short duration of the thermal shock, the chances of formation of insulating Al_2O_3 is minimized, as well as, a portion of the trivalent Al atoms are supposed to diffuse through the p-side of the wafer to produce a p^+ region that provides the back surface field (BSF) and minimizes carrier recombination in turn. In the next step, aiming to further increasing the current

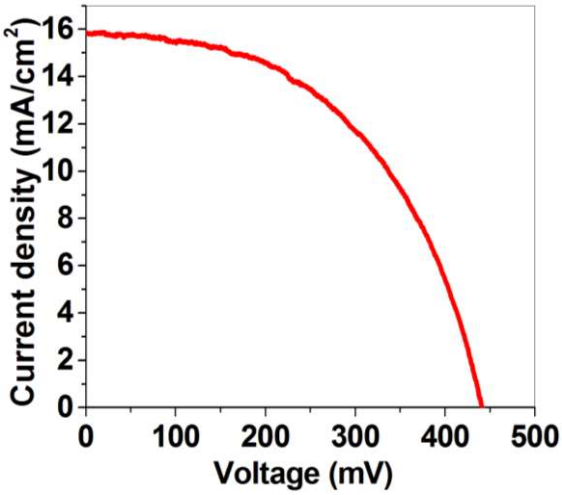

Fig.2.6: J – V characteristics of Cell 2.

collection from the front/top, a thin layer (~50 nm) of ITO was deposited on the complete cell using pulsed dc sputtering as mentioned in Section 2.2.1 and this cell is designated as "Cell 2" (Fig.2.1b). No notable change in V_{oc} was observed as expected, however, interestingly, an increase in J_{sc} was noticed by such front coating of ITO. This led to an uplift of conversion efficiency to 3.53% (Fig.2.6). This thin ITO layer is expected to have a positive impact to minimize the surface defects by blocking the dangling sites of thin silicon as it has been sputtered with slightly oxygen-rich argon plasma. Optically, a ~50 nm thin ITO layer is sufficiently transmissive [153-156] and so, it will not put any significant obstacle in light soaking by the cell. This ITO layer mainly acts as an anti-reflection coating, however, may also help to scatter the incident light more within the cell due to the formation of localized optically matched layers viz. air/ITO/Si whose refractive indices (RIs) fall in a graded manner, i.e. $RI_{air} \times RI_{Si} = (RI_{ITO})^2$. This practice increases the optical path length (OPL) of the light within the cell and hence, the carrier generation increases near the junction. Keeping in mind the improvement in the front current collection in "Cell 3", the concept of introducing a dangling bond blocking layer [154,157] has been adopted to minimize the surface defects and related loss in carriers. Previously, it has been reported that ITO

nanoparticles can act as a very good back grid contact layer for the performance enhancement of single-junction crystalline silicon solar cells [158]. To study in detail, the back of the cells were coated with ITO layers with three different thicknesses viz. 50, 100, and 150 nm before the Al coating. These cells are designated as "Cell 3a", "Cell 3b" and "Cell 3c". Improvement in J_{sc} was observed in Cell 3a (than Cell 2), which has a 50 nm thick back ITO layer; however, with increasing ITO thickness, there was a drop in both J_{sc} and V_{oc} as can be evident by Fig.2.7.

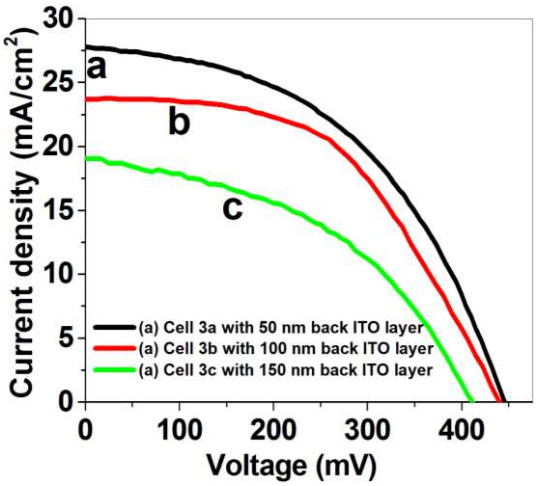

Fig.2.7: J–V characteristics of Cell 3a, 3a, and 3c.

With increasing ITO thickness, the chances of diffusion of trivalent Al ions from the back Al contact to the p-layer becomes difficult, leading to a less populated p^+ region. This in turn lowers the BSF and subsequent lowering in V_{oc} is observed. The lowering in J_{sc} with increasing thickness of ITO layer is attributed to the back reflection phenomenon. To investigate in detail, the actual reflection properties from the back Al/ITO layer, ITO and Al (200 nm) have been deposited on the thin Si wafer to produce the following four structures: (i) Si/Al, (ii) Si/ITO-50 nm/Al, (iii) Si/ITO-100 nm/Al and (iv) Si/ITO-150 nm/Al. Light impinged from the Si side within the wavelength range 400–1100 nm and the result is shown in Fig.2.8.

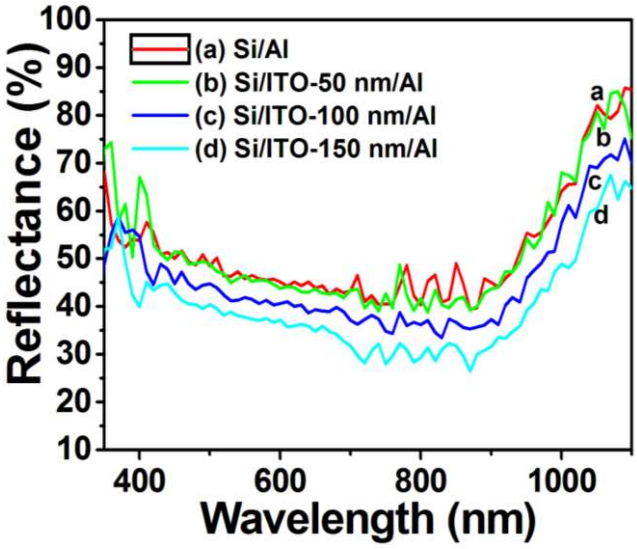

Fig.2.8: Reflectance from (a) Si/Al, (b) Si/ITO-50 nm/Al, (c) Si/ITO-100 nm/Al and (d) Si/ITO-150 nm/Al structures with light impinging on the Si surface. The thickness of Al layer in all cases is 200 nm.

Si/Al and Si/ITO-50 nm/Al structures showed almost similar reflectance from the back, however, with increasing thickness of the ITO layer, a notable lowering in the back reflection has been observed over the entire 400 – 1100 nm region. This might be attributed to more interplanar reflections [159] by the ITO layers with increasing thickness and planes that lead to greater parasitic absorption. Now, as the reflection from the back surface becomes poor, the active layer of the solar cell gets less amount of light leading to lesser carrier generation, and this is reflected in the lowering of J_{sc} of the respective cells. So, it can be concluded that the 50 nm thick ITO layer is optimum for Al diffusion and light reflection. However, this resulted in a maximum of 7.07% conversion efficiency with a 30 µm wafer with 50 nm front and back ITO coating. The contact resistance between the ITO/p-Si layer was found to be 1.26 ohm. This knowledge has been exploited to further enhance the cell efficiency by front texturing on a 30 µm wafer along with the incorporation of 50 nm front and back ITO coating as per Fig.2.1d and is referred to as “Cell 4”. The texturization has been carried out by placing a 30 µm wafer (one side blocked with nitride coating) vertically in a bath

containing a mixture of 2% aqueous KOH solution and 5% isopropyl alcohol preheated at 80°C. After 40 minutes the wafer was removed from the solution, washed thoroughly with isopropyl alcohol, dried using compressed nitrogen flow. A representative morphological view of such textured wafer without and with ITO coating is presented in Fig.2.9a. It is evident from Fig.2.9a, that the pyramids are well grown even on the thin wafer; they are compact and have a base edge length ranging between 5–7 µm.

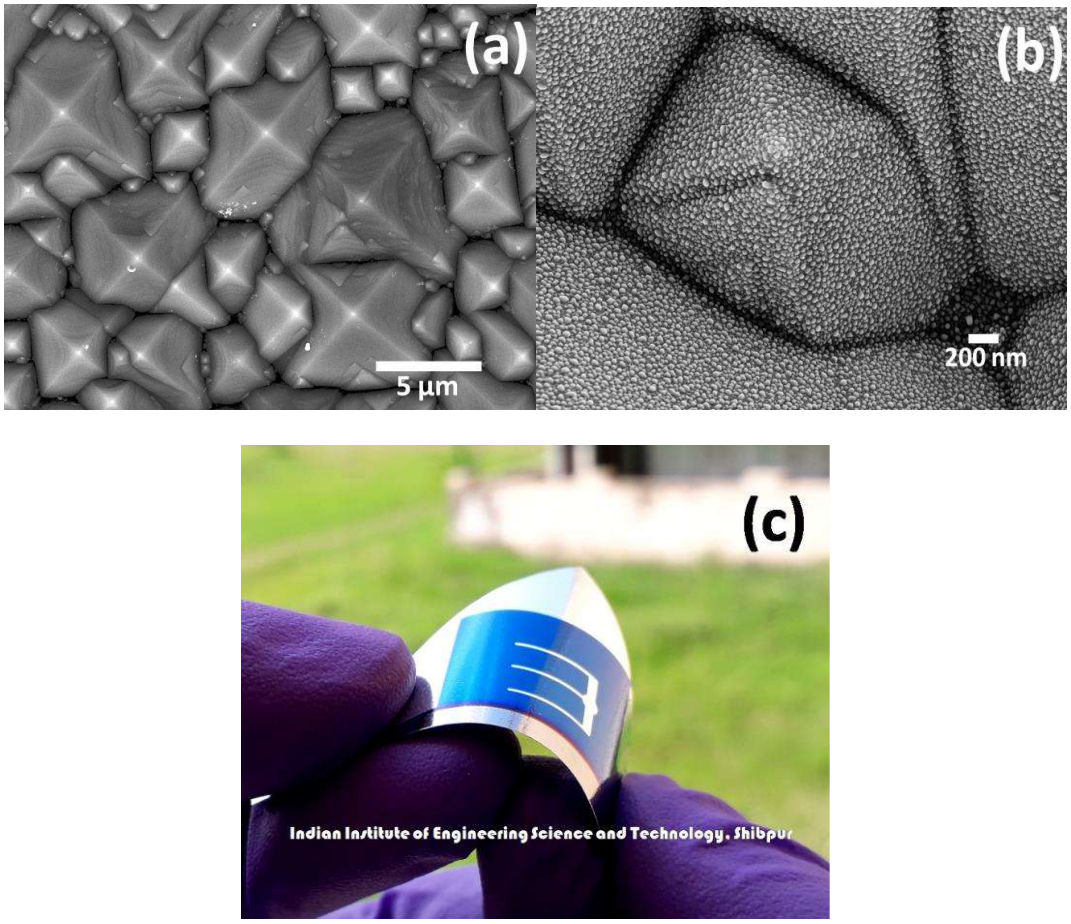

Fig.2.9: (a) FESEM image of the 30 µm textured wafer before ITO coating and (b) after ITO coating. (c) Photograph of a finished cell on a textured thin wafer.

The texturized sample was then taken for n-diffusion supported by a Quartz glass and after diffusion HF treatment was carried out. This removes the nitride layer from the back and phosphosilicate glass (formed during diffusion) from the top. The backside was then coated with 50 nm ITO by sputtering. Front Ag (‘E-mask’) and back

Al (entire surface) contacts were formed using evaporation to produce a final cell as (Cell 4) as shown in Fig.2.9c. Cell 4 had two subtypes, one without a top 50 nm ITO layer (Cell 4a) and the other with a 50 nm top ITO layer (Cell 4b). The image representing the morphology of the cell after coating with ITO is presented in Fig.2.9b and the photograph of a flexible cell is shown in Fig.2.9c. The J–V characteristics of Cell 4a and 4b are shown in Fig.2.10.

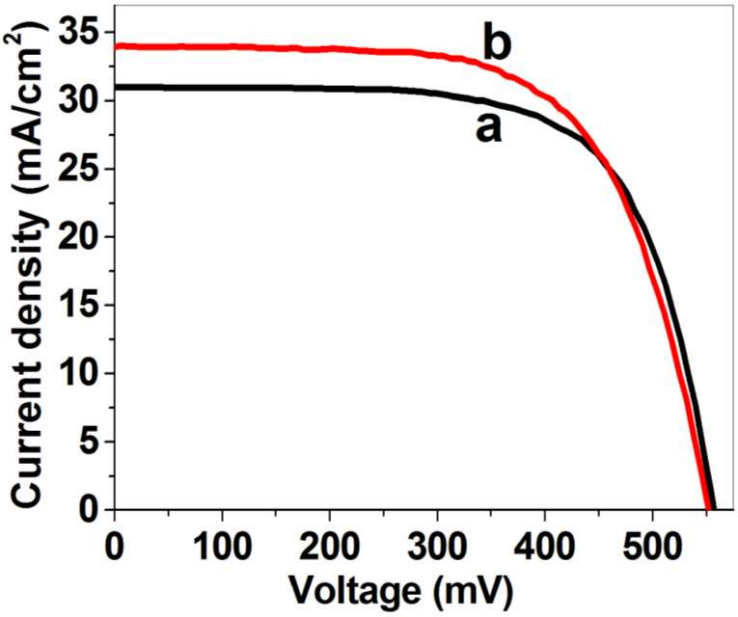

Fig.2.10: J–V characteristics of Cell 4a and Cell 4b.

Both Cell 4a and Cell 4b were given thermal shock using a firing belt furnace as mentioned here. Cell 4a yielded a photo-conversion efficiency of 11.73%, which showed a notable increase in J_{sc} and efficiency after top ITO coating. Again, this proves that the 50 nm thick top ITO layer is a good current collector which does not compromise with the light transmittance. This prototype showed 12.23% conversion efficiency which is the best so far in this thin and flexible wafer-based single-junction solar cell series. The observed cell parameters for all the cells fabricated in this work have been summarized in Table 2.1.

2.3.4. Experimental and theoretical validation:

The gradual improvement in efficiency and other cell parameters, as demonstrated in this work, for thin (30 μm) wafer-based monocrystalline single-junction solar cells has been achieved mainly due to the incorporation of thin ITO layers on the top and at the bottom and Al back contact followed by firing. Finally, the concept of introducing front texturization on a thin wafer has been adopted which resulted in markedly high efficiency of 12.23%.

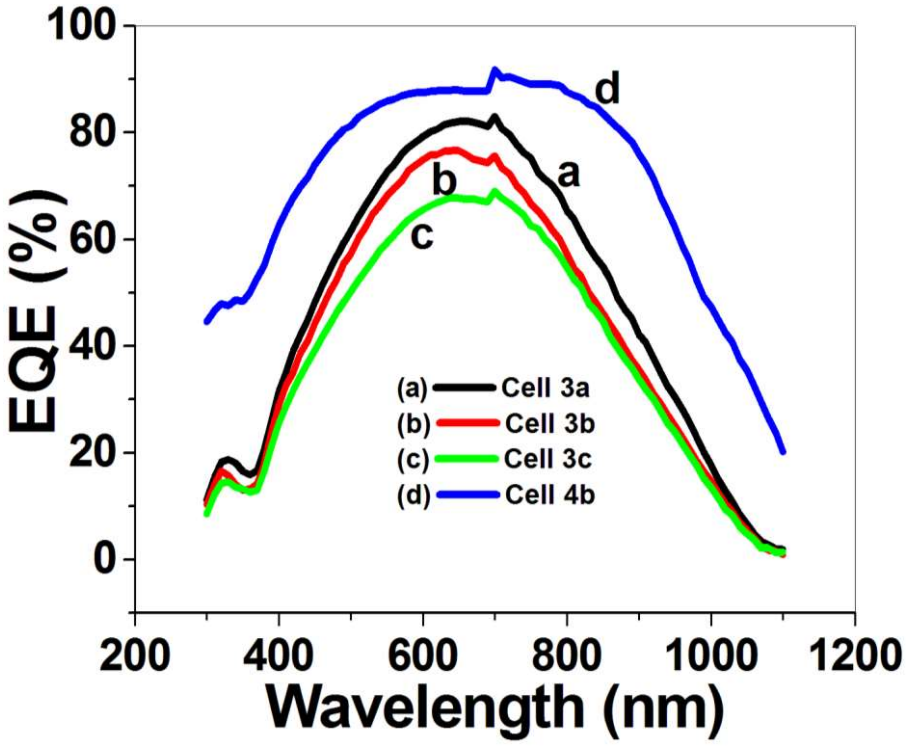

Fig.2.11: EQE curves for (a) Cell 3a (b) Cell 3b (c) Cell 3c and (d) Cell 4b.

These findings have been validated through external quantum efficiency (EQE) measurements and also by studying the simulated energy profiles within the cells. The variation in thickness of the back ITO layer (within Al and p-Si) brings the difference in Cell 3a, 3b, and 3c (fabricated following Fig.2.1c). As the thickness of the ITO layer in all cases was in several tens of nanometers, it is expected that their effect on blocking/passivating the dangling sites to minimizing the surface defects will be the

same. So, the other two things, i.e. the reflectance from Al/ITO surface and the capability of aluminum diffusion through the ITO layer play key roles. It has been seen from the reflectance profiles of various Al/ITO layers (Fig.2.8) that the 50 nm ITO layer on Al has an almost similar reflectance pattern as of bare Al layer with a small lowering within 500 to 900 nm. However, the reflectance within 400 to 500 nm and 900 to 1100 nm for Al/50 nm ITO layer was slightly higher than that of bare Al. Fig.2.8 also exhibited a notable lowering in reflectance from Al/100 nm ITO and Al/150 nm ITO layers over the entire 400 to 1100 nm wavelength zone, making them a poor reflector than either bare Al or Al/50 nm ITO layer. This has also been reflected by the EQE curves (Fig.2.11) of Cell 3a, Cell 3b, and Cell 3c consisting of 50 nm, 100 nm, and 150 nm ITO layers on Al at the back, respectively. In comparison to Cell 3a, the EQE response of Cell 3b within 500–1000 nm was poor. The same for Cell 3c was poor over the entire 400 – 1000 nm region than Cell 3a. Primarily, this can be attributed to the reflection loss from the Al/100 nm ITO and Al/150 nm ITO layers which leads to poor carrier generation near the junction. Among these three, Cell 3a has the best EQE profile within 400–1000 nm, which may be accounted for better light reflection by the Al/50 nm ITO layer leading to better carrier generation near the junction of the thin cell.

To validate this, energy profiles on the top of Cell 3a (near the junction) have been estimated using the COMSOL Multiphysics^{TM} tool at nine different wavelengths covering entire 300–1100 nm, and most interestingly, energy hotspots were found to generate and grow gradually up to 0.60 μm from the top of the cell, i.e., within the diffusion or junction zone, with

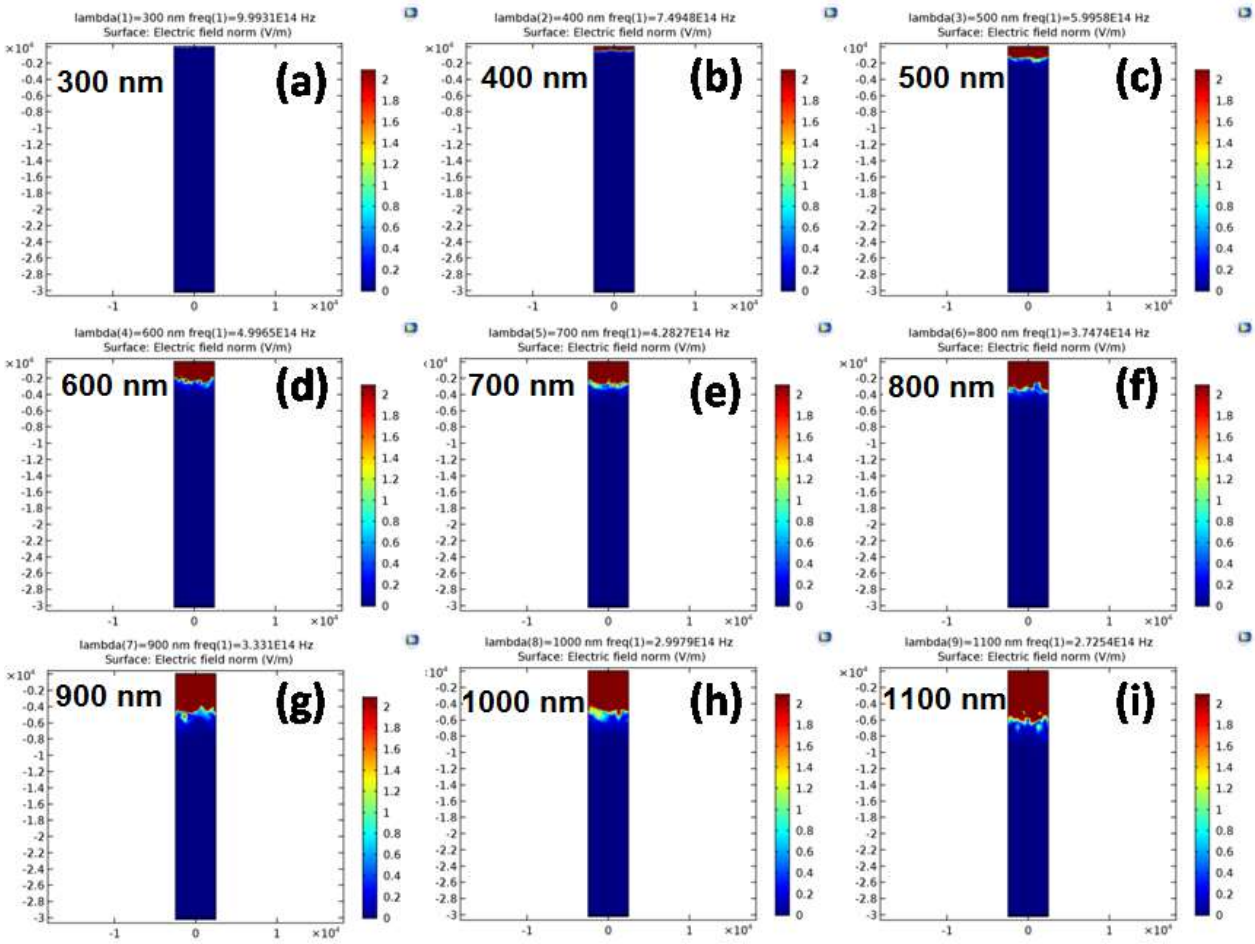

Fig 2.12: Wavelength-dependent energy profile diagram near the junction of the cell fabricated with 30 µm wafer and having Al/50 nm thick ITO layer as the back contact (Cell 3a). Chosen wavelengths: (a) 300 (b) 400 (c) 500 (d) 600 (e) 700 (f) 800 (g) 900 (h) 1000 and (i) 1100 nm.

the increasing wavelength of incident light. The energy hotspots were not so intense for 300 and 400 nm of incident light (denoted by bluish-green regions, Fig.2.12a and 2.12b), however, from 500 nm onwards, the intensity and depth of the energy hotspots were found to increase significantly (Fig.2.12c-i). The reflected light with a longer wavelength travels all through the p-type thin wafer from the back and is trapped near the junction and generates energy hotspots. No absorption of light either in the back or in the middle of the cell is revealed by the absence of high-energy spots (green/yellow/red). This in turn confirms the good light reflection behavior, especially in the longer wavelength region, by the Al/50 nm ITO back contact layer. As the

diffusion depth from the top of the cell is about 0.4 µm (as per the adopted condition), it is evident that the cell is getting more light from the longer wavelengths due to the introduction of 50 nm top and bottom ITO layers.

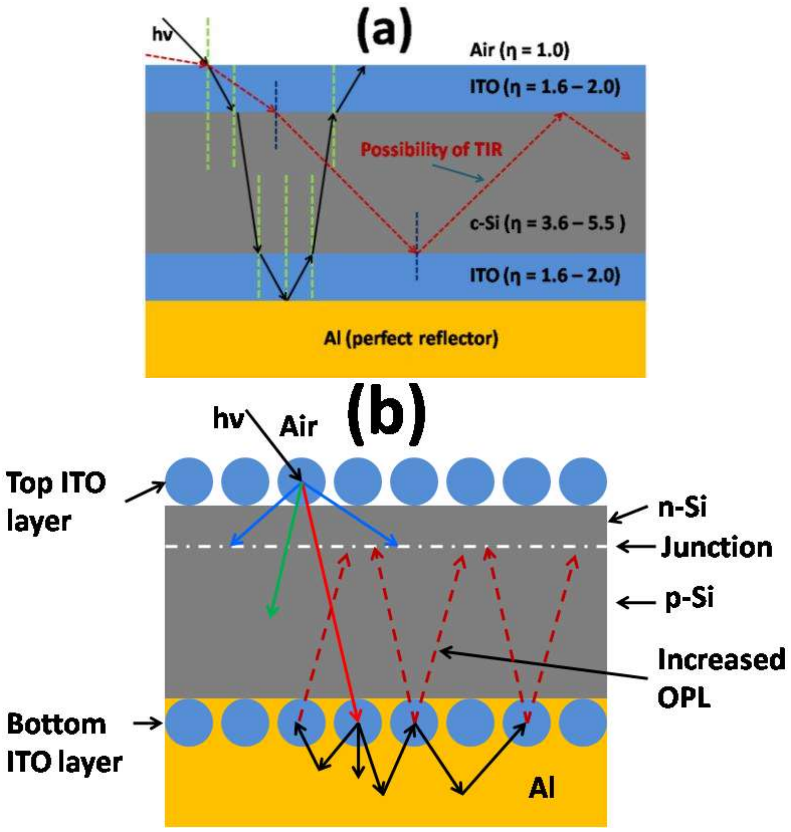

Fig.2.13: Schematics showing (a) the pathway of light through the finished cell depending upon "graded refractive index". The red dotted arrow is showing the possibility of total internal reflection. The refractive indices (RI) are for the 400 – 900 nm zone (b) scattering and multiple bounces of light with longer wavelength (red arrow) in the sandwiched BRL leading to increased OPL (red dotted arrow).

It is interesting to note that the presence of the ITO layer on both sides of the thin cell acts in different ways for trapping the photons. The top layer acts as an anti-reflection coating (ARC) as well as a front scatterer while the bottom layer acts as the back reflector layer. As the light enters from a rarer to a denser medium for the front ITO layer, it allows most of the light to pass through it with some angular bending. On the other hand, for the back ITO layer, the light comes from the denser Si to the lighter

ITO and hence, the back ITO layer shows its reflection property rather than transmission (Fig.2.13a).

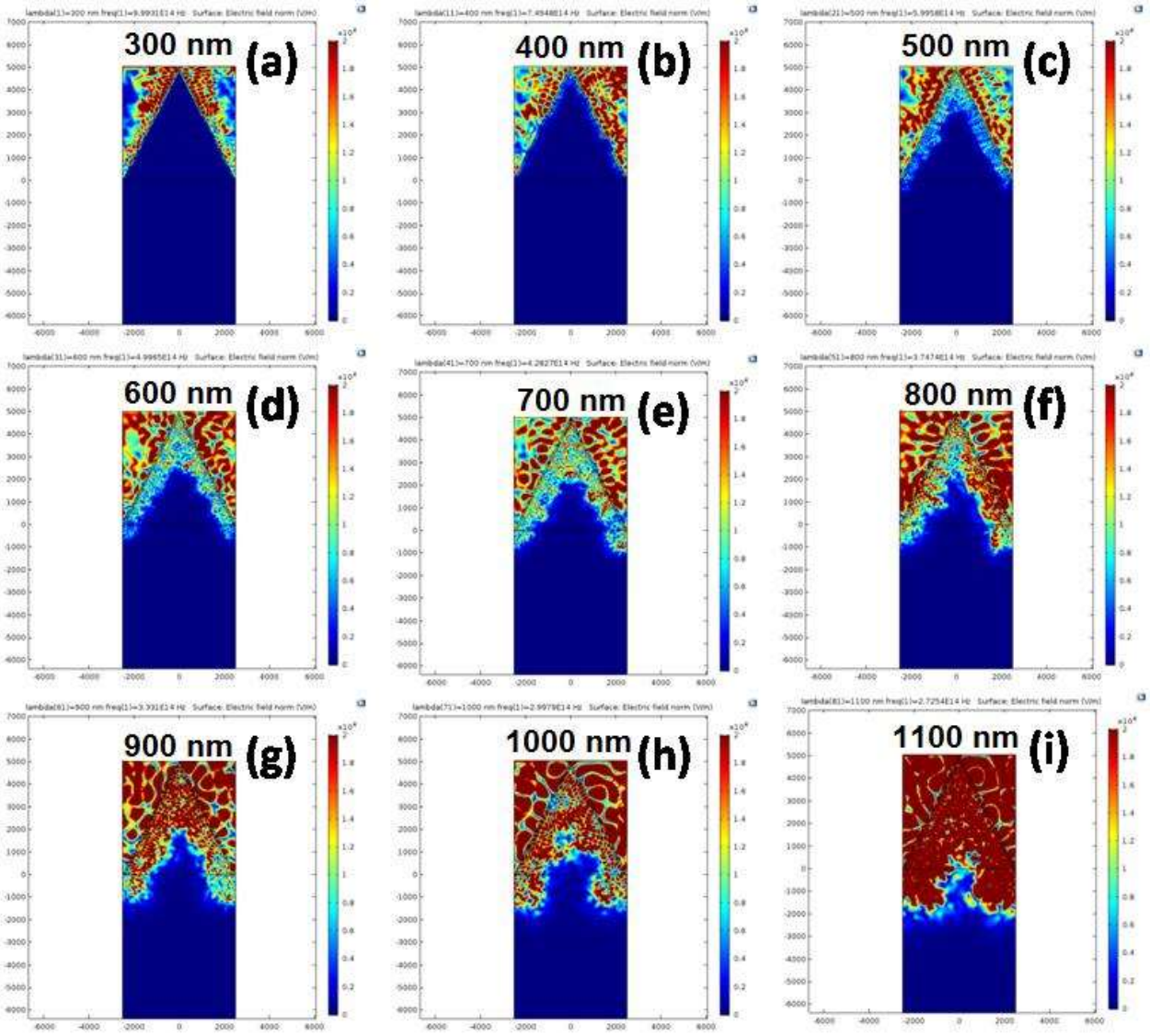

Fig.2.14: Wavelength-dependent energy profile diagram near the junction of the textured cell fabricated with a 30 µm wafer and having Al/50 nm thick ITO layer as the back contact. Chosen wavelengths: (a) 300 (b) 400 (c) 500 (d) 600 (e) 700 (f) 800 (g) 900 (h) 1000 and (i) 1100 nm.

The light rays which strike the Si and the bottom ITO interface at angles greater than the critical angle, get total internally reflected. On the other hand, the rays which strike the interface at angles smaller than the critical angle get transmitted into the bottom ITO layer and are finally reflected from the bottom Al contact. The bottom Al contact and

the sandwiched ITO layer together ensure complete trapping of the photons. As the 50 nm thick back ITO layer falls in the sub-wavelength region for the active solar spectrum, it facilitates the longer wavelength lights to bounce back and reach the junction as well as increases the OPL (Fig.2.13b). There is also a probability of multiple bounces of the scattered light between the ITO and Al layers and as a result of this, a part of the light with longer OPL gets transmitted through the ITO layer and reaches the junction. Thus, the introduction (in between Si and Al) of a rarer medium (to Si) like ITO with optimized thickness enhances the possibility of TIR through additional scattering from ITO nanoparticles providing better light management in the cell. Now, the case becomes more interesting when the top and bottom ITO layers (50 nm) were introduced with the textured thin wafer (Fig.2.14). At 300 and 400 nm, practically no energy hotspots were generated within the wafer/cell (Fig.2.14a and 2.14b). From 500 nm onwards (Fig.2.14c), the electric field started generating within the bulk but near the top of the Si. The intensity of the electric field increases as the wavelength becomes longer, indicating good light trapping behavior within the cell by the application of both top and bottom ITO layers. Like the non-textured cells, in this case, also, no absorption and hotspot generation was found to take place either at the bottom or in the middle of the cell. The fields were found to grow gradually within the bulk from the top by well penetrating the diffusion/junction depth, which is an indication of better light trapping followed by carrier generation. The generation and penetration of electric fields were better in this case than in the cell without front texturization. This, in turn, pushes up the efficiency to 12.23% with a notable value of Voc (552 mv) and Jsc (33.91 mA).

Table 2.1 Observed cell parameters of the cells fabricated in this work.

Cell name	Voc (mV)	Jsc (mA)	Fill Factor (%)	Efficiency (%)
Cell 1a	101	8.92	32.05	0.29
Cell 1b	439	6.46	31.94	0.91
Cell 1c	498	12.50	43.03	2.68
Cell 2	441	15.90	50.42	3.53
Cell 3a	445	27.95	56.82	7.07
Cell 3b	439	23.89	50.98	5.36
Cell 3c	411	19.06	44.70	3.50
Cell 4a	557	31.05	68.02	11.73
Cell 4b	552	33.91	65.25	12.23

2.4. Chapter Conclusion:

In an attempt to meet the sweet point of four primary criteria of modern photovoltaics, i.e. cost-effectiveness, reliability, efficiency, and flexibility, a new concept of single-junction mono-crystalline silicon solar cells based on 30 μm thick wafer has been demonstrated. The as-fabricated prototype showed a state-of-the-art efficiency of 12.23% under AM 1.5 simulated radiation. To manage the incident photons with longer wavelengths (>700 nm) that tends to pass through the thin wafer, an ITO layer was placed between the conventional thin Al back contact and p-type wafer, which not only helped in good back reflection with a probability of TIR but also acted as the blocking/passivating agent of the dangling bonds present on the silicon surface to restrict carrier recombination. The influence of the thickness of such a back ITO layer on the efficiency of the cell has been studied systematically. A systematic

approach of enhancing the efficiency from primitive p-n junction cell structure the final cell has been demonstrated incorporating front texturization, front, and back ITO layers, and thin metallic Al back contact. The experimental results corroborate further predictions based on fundamental principles. This work can open up the possibility of a new photovoltaic technology that utilizes only1/6th (~16%) of the thickness of standard Si wafer used in contemporary solar cells, thereby cutting down the material cost significantly. Further, it is envisaged that the thin Si wafer will make the solar cells suitable for flexible electronics.