SHJ Solar Cells on an Adequately Thin c-Si Wafer With Dome-Like Front and Double-Layer ITO Nanoparticles as Rear Light Trapping Arrangements

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***Abstract*— This present work describes the fabrication of silicon heterojunction (SHJ) solar cells as a proof-of-concept scheme on an adequately thin (~30 μm) n-type crystalline silicon (c-Si) wafer as the active layer. The thickness of the cell, in this case, is five to six times lower than any c-Si-based conventional solar cell technology. The work has been initiated to go in line with the recommendations of the International Technology Roadmap for Photovoltaics (ITRPV) in 2019 on the "thinning" of silicon-based solar cells to achieve cost-effectiveness of the modules. To address light-trapping-related issues in thin silicon substrate, dome-like front texturization and indium tin oxide (ITO) compact layer/nanoparticle (NP) array as the back reflecting configurations have been adopted. Dome-like front textured surface helped in conformal deposition of the front amorphous layers, improving the shunt resistance, open-circuit voltage, and fill factor of the cell. On the other hand, a properly placed array of single and double layers of ITO NPs notably increased the back reflection of light with wavelengths >700 nm, resulting in improved short-circuit current density and conversion efficiency. Comparative investigations have been carried out to explore the influence of different ITO-based back reflecting structures on the cell parameters with detailed optical and electrical characterization. We have reported ~15% conversion efficiency with an n-type as-cut c-Si wafer having a carrier lifetime of ~100 μs.**

***Index Terms*— Double back reflection layer, indium tin oxide (ITO) nanoparticle (NP), light trapping, proper positioning, silicon heterojunction (SHJ) solar cell, thin crystalline silicon (c-Si) wafer.**

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I. Introduction

EVEN though there are multiple thin and cost-effective solar cells developed worldwide [1]–[7] in the past few decades, crystalline silicon (c-Si)-based solar cells are still leading the solar photovoltaics (SPV) market due to their high conversion efficiency, robustness, reliability, and natural abundance of raw materials [8]. Since the invention of the silicon solar cells [9]; this technology has progressed a lot through the improvement of material quality, light-trapping structures, and overall cell architecture, facilitating the fabrication of very thin silicon-based solar cells [10]–[13]. In the present era, the only possibility by which we can achieve the Shockley limit [14], [15] is by incorporating the silicon heterojunction (SHJ) cell concept, in a conventional c-Si solar cell. Even after such advancements in solar PV technology, generally, the major cost of the c-Si solar modules is due to the cost of its bulk Si material. So, it is necessary to enhance the conversion efficiency of the cell, as well as to reduce the fabrication cost to make SPV more popular. One of the most effective ways for reducing the cost of a c-Si module is to cut down the material cost by lowering the thickness of the active c-Si layer. It has been forecast that a 50-μm-thick wafer has the potential to minimize the module cost without much compromising with the cell efficiency [16]. According to the recommendations made by the International Technology Roadmap for Photovoltaics (ITRPV) in 2019, "thinning" of silicon-based solar cells to 110 μm is crucial to achieving the cost-effectiveness of the modules within the year 2029.

As far as the SHJ solar cells are concerned, Hirayama *et al.* [17] reported 22.8% efficiency on 100-μm wafer, and Taguchi *et al.* [18] reported 24.7% efficiency on 98-μm wafer. Very recently, Sai and Matsui [19] have achieved 22% efficiency on less than 50-μm thin wafer using SHJ structure. It was stated that the parasitic absorption at a longer wavelength is a function of wafer thickness, and fill factor (FF) is also sensitive to surface recombination which varies with wafer thickness [20]. Later, Balaji *et al.* [21] reported a 22.48% efficiency for a 40-μm silicon wafer by optimizing the intrinsic hydrogenated amorphous silicon (i-a-Si:H) layer by varying the compositional ratio of silane to hydrogen gas. These works

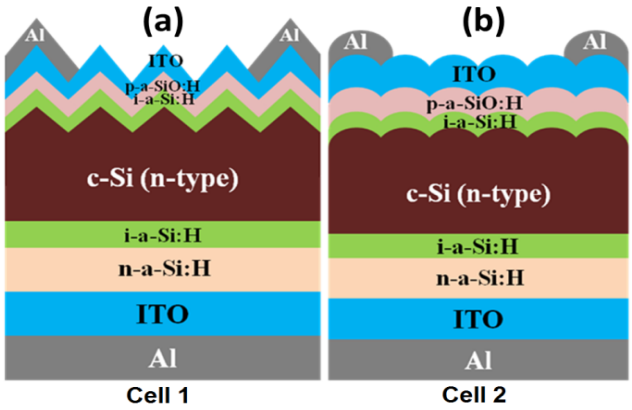

Fig. 1. Schematic of thin (~30 μm) SHJ cells (a) with pyramidal front texture (Cell 1) and (b) with dome-shaped front surface (Cell 2).

were performed on wafers with notably high carrier lifetime >2 ms. On the other hand, Dikshit *et al.* [22] have successfully fabricated 12.25% efficient single-junction solar cells on a 30-μm c-Si wafer with a lifetime of 100 μs. However, cutting down the absorber layer thickness up to a certain level results in less photocarrier generation and lowered short-circuit current density (J_{SC}) as the thinner c-Si substrate is quite transparent to the incident light having longer wavelengths, mainly in the near-infrared (NIR) region [21]. For this reason, well-suited front scattering and back reflection arrangements are essential to fabricate a solar cell (either with SHJ structure or single junction) with notably good cell parameters.

This work includes the fabrication of SHJ solar cells on ~30-μm-thick n-type c-Si wafers as a proof-of-concept scheme to go in line with ITRPV-2019 recommendations regarding the use of thinner active layer. As this 30-μm wafer is quite transparent to incident light with wavelengths >700 nm, proper light trapping tricks like the use of dome-shaped front scatterer and properly positioned indium tin oxide (ITO) nanoparticle (NP) array as back reflector layers (BRLs) were introduced.

II. Experimental Details

The conventional baseline fabrication procedure for SHJ solar cells has been modified and optimized to make thin SHJ cells in this work. Initially, 180-μm-thick 3" × 3" commercially available n-type monocrystalline <100> Czochralski grade (CZ) Si wafers having a carrier lifetime of 100 μs (as per specification) were taken and scaled down to ~30 μm following the procedure as mentioned elsewhere [22]. In brief, the wafers were mounted vertically in a borosilicate beaker containing 10% NaOH solution at 85 °C. After 55 min, the wafers were removed and washed thoroughly with deionized cold water. This yielded thin wafers with ~30-μm thickness. The thin substrates were used to investigate the optical (transmittance) properties in bare condition, as well as decorated with ITO layers/NPs. For the textured structures and cells, the starting thickness of the scaled-down substrate was taken as ~50 μm by lowering the thinning time to 48 min. The additional 20 μm thickness margin is necessary for texturization-related etching and back polishing so that the final substrate/cell thickness comes down to ~30 μm and the uniformity in thickness is maintained. These wafers were cut into 18 mm × 18 mm pieces using Nd:YAG laser (λ = 1064 nm, Argus, China) to fabricate the cells. Before texturization, one side of such wafers was blocked using silicon nitride (SiN_X) coated with plasma-enhanced chemical vapor deposition (PECVD) (make Hind High Vacuum, India) under 1 torr pressure, 400 °C process temperature, and 30 W RF power for 10 min with a gas flow (sccm) ratio of 45:45:65 for NH_3:H_2:SiH_4. This restricts the texturization of the wafer on the SiN_X-coated side. Texturization was done by placing such a wafer vertically in a bath containing a mixture of 2% aqueous KOH solution and 5% isopropyl alcohol (IPA) preheated at 80 °C. The wafer was removed from the solution after 40 min, washed thoroughly with normal IPA, and dried using compressed nitrogen flow. This yielded pyramidal shapes on the SiN_X-uncoated (front) surface and removal of the nitride coating followed by the generation of some undulations on the other (back) surface. These wafers were divided into two sets. Backside polishing of a set of such wafers was carried out using a custom-built single-side etcher with the help of a 20% KOH solution so that the front side remains pyramidal. The second set was treated with HNA (HF:HNO_3:CH_3COOH) solution with a concentration ratio of 5:1:1 at ambient temperature for 4 min to create dome shapes out of the pyramidal structures. HNA treatment in this case also performs backside polishing of the wafers. Cleaning of wafers was accomplished with the help of standard wet cleaning process of RCA-1 and RCA-2 followed by 1% HF dip and cleaning by running deionized water. The ITO layers and NPs were deposited using RF magnetron sputtering (Hind High Vacuum) from an ITO target with the composition In_2O_3:SnO_2 as 90:10 (wt%). The detailed ITO deposition procedure has been elaborated on in the respective section for easy reading. The amorphous and micro-c-Si-based layers like p-type hydrogenated amorphous silicon oxide (p-a-SiO:H) layer, i-a-Si:H layer, n-type hydrogenated amorphous silicon (n-a-Si:H) layer, and n-type microcrystalline hydrogenated amorphous silicon (n-μc-Si:H) layer required to fabricate the SHJ cells were deposited using a five-chamber PECVD cluster tool (Hind High Vacuum) following the recipe as mentioned in Table I. The thickness of the individual layers was monitored using an in-built dynamic thickness monitor. The PECVD system used in this case is a single-side deposition unit, and the deposition of amorphous silicon layers on both sides of the wafer is not possible without breaking the vacuum and taking out the sample from the chamber with this particular instrument. This may affect surface passivation and might be the reason for not getting state-of-the-art V_{OC}. The carrier lifetime of the wafer also influences the electrical properties of the fabricated cells. An ITO layer with a thickness of 50 nm was placed between the silicon substrate and back contact using RF magnetron sputtering. A front ITO layer with the same thickness was also sputtered on the finished cell before taking the front Al contacts. Finally, front and back metallic Al contacts were deposited on these ITO layers from the finished cells using thermal evaporation (Hind High Vacuum). The thickness of the back contact was 300 nm, whereas it was 250 nm for the front contact that was deposited through

TABLE I
DETAILED RECIPE FOR THE DEPOSITION OF AMORPHOUS AND MICROCRYSTALLINE LAYERS

Type of Layer	SiH_4:H_2	B_2H_4 (sccm)	PH_3 (sccm)	CO_2 (sccm)	P_d (mW/cm$^{2)}$	P_r(torr)	Thickness (nm)
p-a-SiO:H	1:25	3	NA	2.5	60	1	12
i-a-Si:H	1:6	NA	NA	NA	30	1	5
n-a-Si:H	1:5	NA	0.2	NA	40	1	25
n-μc-Si:H	1:50	NA	0.04	NA	35	1	20

an *E*-mask ("shadow mask" having the shape of the letter "*E*"). Morphological analyses of the textured surface and ITO NPs were carried out using a field emission scanning electron microscope (FESEM, Zeiss Sigma). Particle diameter measurement was carried out using ImageJ software. Optical reflectance and external quantum efficiency (EQE) were investigated using a Bentham PVE-300 Series spectral response unit. The current density–voltage (J–V) characteristic was measured with the help of a Cell Tester CT-50AAA from Photo Emission Tech., California, USA. Both reflectance and J–V characteristics were measured under AM1.5G simulated radiation.

III. RESULTS AND DISCUSSION

A. Fabrication of Thin SHJ Solar Cells

Thin SHJ cells with two different front surface morphologies have been fabricated as per the scheme shown in Fig. 1. The recipe as elaborated in Section II was followed to make the cells. During the deposition of front i-a-Si:H, p-a-SiO:H, and ITO layers on the thin wafer with the pyramidal front surface, it has been observed that due to the presence of sharp spikes on the textured front, punching of these ultrathin layers occurs leading to poor shunt of the cell. Hence, FF and V_{OC} of the cell are sacrificed. Technically, conformal covering of the pyramids (with height ~3 μm) by ultrathin amorphous layers is difficult. This could be resolved by partial etching of the pyramidal textured surface that leads to dome-shaped topography. The cross-sectional FESEM image (Fig. 2) of the textured thin c-Si wafer before and after HNA treatment clearly shows the formation of dome-shaped morphology after partial etching of pyramidal textures. The height of such domes was found to be within 1–1.5 μm. It can clearly be understood from Fig. 2(b) that rounding off of the surface will facilitate conformal deposition of ultrathin amorphous layers on the front of thin c-Si wafer which is essential to achieve good electrical property of the SHJ cell. However, it is worth mentioning that the rounding off of the pyramidal surface to dome-like morphology will put some detrimental effect on the optical property of the wafer. To study any such effect, reflectance from thin c-Si wafer with pyramidal and dome-shaped structures was measured within 300–1100 nm wavelength region and is presented in Fig. 3. A total loss of 2.7% in the weighted average reflectance was observed after rounding off the pyramidal textures, which is not quite significant as the gain in electrical properties predominates in the latter case. This has been established by measuring the performance of the two SHJ cells as per the schemes presented in Fig. 1. The advanced thin silicon solar cells of recent times involve the use of a flat rear surface rather than a textured surface. This is done to obtain better passivation as reported

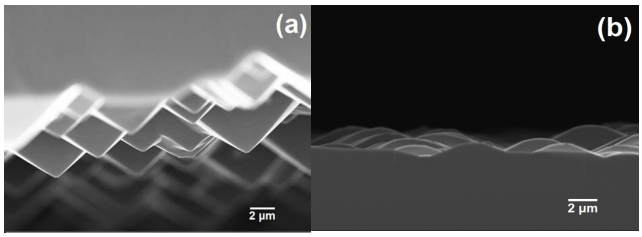

Fig. 2. Cross-sectional view of the textured thin c-Si wafer (a) before HNA treatment and (b) after HNA treatment. Partial etching of the pyramidal structure leading to dome-shaped topography is evident.

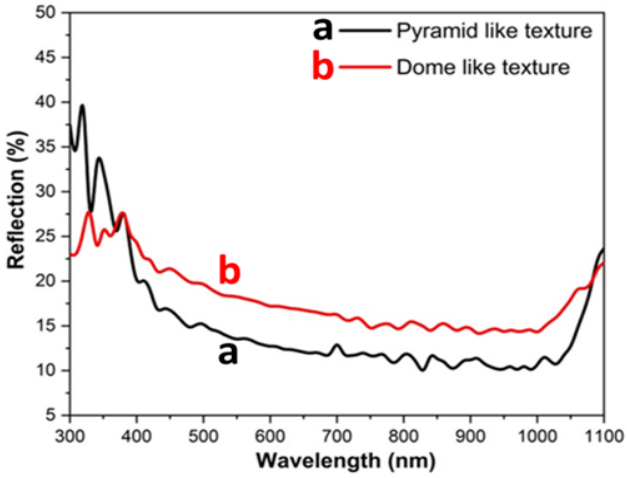

Fig. 3. Reflection characteristics of the surface of the c-Si wafer with (a) pyramidal and (b) dome-shaped textures.

by Kim *et al.* [23] and Kung *et al.* [24]. The same concept has been adopted here. The cell area was 1.0 cm^2 in all cases.

The J–V characteristics of Cell 1 and Cell 2 are presented in Fig. 4, and the cell parameters are summarized in Table II. It has been found that Cell 1 yielded V_{OC} and J_{SC} as 627 mV and 30.98 mA/cm^2, respectively; with an FF of 0.62. The conversion efficiency was 12.04%, whereas for Cell 2, the values for V_{OC}, J_{SC}, and FF were 638 mV, 30.36 mA/cm^2, and 0.69, respectively. This leads to a conversion efficiency of 13.37% for this case. Here, the obtained V_{OC} is somewhat lesser than the previous reports [20], [21]. This might be attributed to the use of as-cut CZ wafers having carrier lifetime ~100 μs, which is notably lower than the value (>2 ms) of the referred cases. Moreover, the fabrication limitations as mentioned earlier in depositing the amorphous layers on both sides without breaking the vacuum of the PECVD chamber could be the other reason. The effect of "doming" of the front textured surface on the optical and electrical properties is quite evident from the cell parameters of Cell 2. About 2% loss in J_{SC} is attributed to light loss due to enhanced reflection by the dome-like front structure. Whereas the gain in V_{OC} and FF is

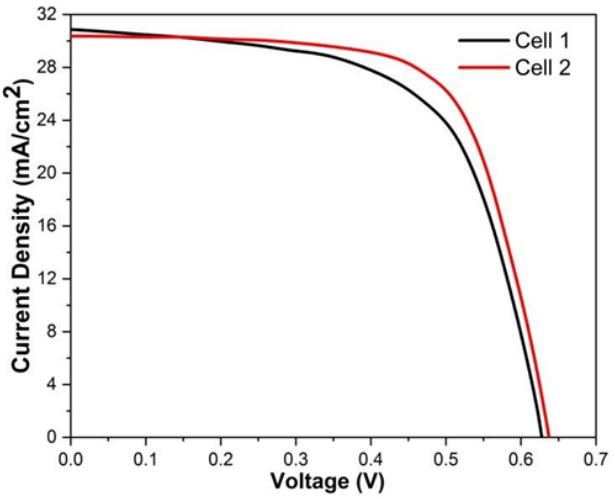

Fig. 4. *J–V* characteristics of the thin SHJ cell with pyramidal (Cell 1) and dome-shaped (Cell 2) front textures.

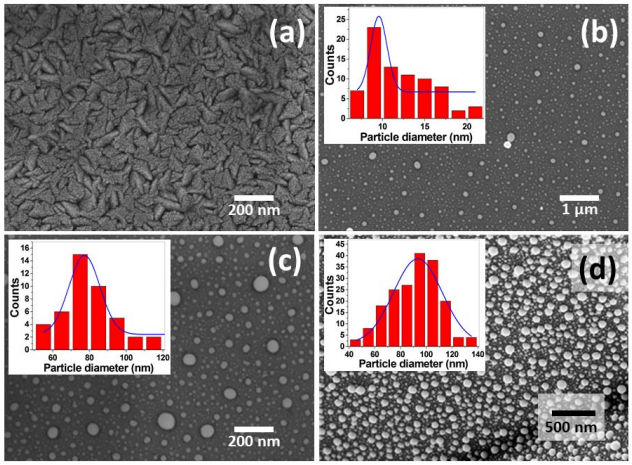

Fig. 5. Morphology of the ITO layers (a) 50-nm-thick flat sample and 20-nm-thick Ar plasma-treated samples for (b) 5 min, (c) 10 min, and (d) 15 min. Inset images show the particle size distribution curves for the respective samples.

due to better passivation and improved shunt attained after doming the front textures. This resulted in an overall 11.04% increase in photoconversion efficiency.

The photoconversion efficiency of Cell 2 is 13.37% and this could be further improved by applying proper back reflection architecture. Minimizing the transmission loss of the longer wavelengths through thin active materials is one of the crucial steps that need to be taken care of in this regard.

B. ITO NPs as the Back Reflectors

It is well-known that semiconductor NPs (like ITO NPs) have lower parasitic absorption than metal (Au, Ag) NPs. This means light loss due to Joule heating will be less in the case of ITO NPs than metal NPs. For this reason, the use of ITO NPs has been adopted in the back reflecting structure in this case. This will also help to compare the flat and NP array of ITO layers in terms of their light reflection capabilities. It can be seen from Fig. 1 that a flat ITO layer with 50 nm thickness was introduced between the n-a-Si:H and back Al contact for both Cell 1 and Cell 2. This ITO layer plays two roles, viz.: 1) helps in forming good ohmic contact between the n-a-Si:H and metallic Al layer and 2) increase the probability of light reflection from the back.

The flat ITO layers with 50-nm thickness were deposited using RF magnetron sputtering from an ITO (SnO_2:In = 90:10) target at a process pressure of 2×10^{-5} mbar and temperature 180 °C with a power density of 1.2 W/cm^2. Sputtered gas argon (Ar) has been used along with oxygen (O_2) with a flow (sccm) ratio of 99:1. The same sputtering chamber and sputtered gas Ar were used for realization of ITO NPs keeping the target closed by a stainless steel lid. However, to form ITO NPs, the initial thickness of the layer was kept at 20 nm. Process pressure and power density were kept fixed at 0.5 torr and 100 mW/cm^2, respectively. Ar plasma exposure time was varied from 5 to 15 min for realization of ITO NPs with various diameters. Fig. 5(a) represents the morphology of the as-deposited ITO layer, whereas Fig. 5(b)–(d) represents the morphology of the Ar plasma-treated ITO substrates. The tendency of forming almost spherical ITO NPs and their density was found to increase with an increase in Ar plasma treatment duration, which is also evident from the particle size distribution curves of the respective samples placed as the inset images. For the 10-min Ar plasma-treated sample [Fig. 5(c)], the main particle size distribution was found to be within 70–90 nm. Whereas a broad particle size distribution, mainly over 70–110 nm with increased distribution density, was observed for the 15-min Ar plasma-treated sample [Fig. 5(d)]. This particular sample was chosen as the back reflecting structure along with the flat one [Fig. 5(a)] to carry out a comparative investigation.

C. Transmission and Reflection Properties of BRLs

Transmission of light with longer wavelengths through a thin (c.a. 30 μm) silicon substrate is a typical problem. To explore the exact scenario in this case, five different back layer configurations with thin (~30 μm) c-Si wafer and ITO layer/NPs have been prepared as described in Fig. 6. In this case, the thickness of the ITO layers was 50 nm in all cases, whereas the ITO NPs bear the properties mentioned in Section III-B. Being significantly small in thickness, the other amorphous silicon-based layers on the front were not considered. The light transmission properties of the back layer configurations as presented in Fig. 6 were experimentally measured within the wavelength range of 500–1100 nm and the results are shown in Fig. 7. A sharp rise in transmittance of light through the 30-μm substrate has been observed after 750 nm for all five configurations. The thin and bare c-Si showed maximum transmittance, whereas the thin wafer decorated with n-a-Si:H layer and ITO NPs [Fig. 6(e)] showed minimum transmittance of light within 750–1100 nm. The weighted average transmittance was found to be 17.38, 16.99, 13.20, 14.14, and 11.16 for thin n-c-Si wafers with conditions (a) bare, (b) coated with 50-nm ITO layer, (c) decorated with ITO NPs, (d) coated with both n-a-Si:H (25 nm) and ITO layer (50 nm), and (e) coated with 25-nm n-a-Si:H layer and decorated with ITO NPs, respectively. It is

TABLE II
CELL PARAMETERS OF THE FABRICATED SHJ CELLS ON 30-μm WAFER WITH VARIOUS LIGHT MANAGEMENT SCHEMES

Sl No.	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF	E_{ff} (%)	Series resistance (Ω)	Shunt resistance (Ω)
Cell 1	30.98	627	0.62	12.04	5.13	149.80
Cell 2	30.36	638	0.69	13.37	5.17	344.33
Cell 3A	29.11	591	0.58	9.98	6.12	102.76
Cell 3B	29.84	602	0.60	10.78	5.84	132.54
Cell 3C	33.80	641	0.68	14.73	5.20	323.15
Cell 3D	**34.46**	**641**	**0.68**	**15.02**	**5.11**	**315.83**

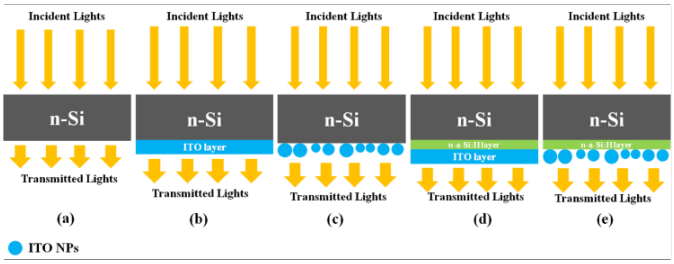

Fig. 6. Transmission analysis configurations of 30-μm c-Si. (a) Without any layers. (b) With ITO layer. (c) With ITO NPs. (d) With n-a-Si:H and ITO layers. (e) With n-a-Si:H layer and ITO NPs.

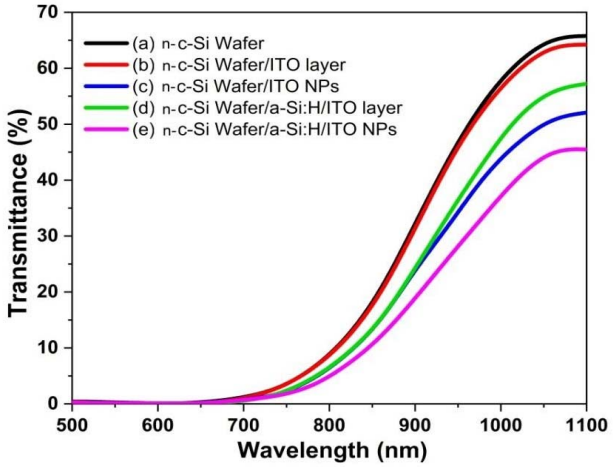

Fig. 7. Transmittance curves for 30-μm c-Si wafer decorated with ITO layer/NPs. (a) n-c-Si wafer. (b) n-c-Si wafer/ITO layer. (c) n-c-Si wafer/ITO NPs. (d) n-c-Si wafer/a-Si:H/ITO layer. (e) n-c-Si wafer/a-Si:H/ITO NPs.

evident from the curves presented in Fig. 7 and the weighted average transmittance values that ITO, specifically in the form of almost spherical NPs, plays a significant role in lowering the light transmission loss within 750–1100 nm through the 30-μm thin n-c-Si active layer. This might be attributed to the good light reflection behavior of ITO NPs that reflect a part of the incident light coming through the n-c-Si thin wafer.

This could be further validated by measuring reflectance from the proposed back layer configurations as mentioned in Fig. 6(a)–(e). To do so, initially, it has been tried to measure reflections from the front of the n-c-Si substrate after depositing the layers on it; however, no prominent signal was received and this might be due to the absorbance of small-intensity back-reflected lights within the active layer. To address this problem, inverted back reflection configurations were mimicked on properly cleaned glass substrates as elaborated in Fig. 8. As it has been seen from the transmittance measurements that the 30-μm thin c-Si wafer allows the light to pass through mainly after 700 nm in wavelength, light reflection from the front of these configurations has been measured within 700–1100 nm, and the curves are presented in Fig. 9.

It is evident from Fig. 9 that incorporation of ITO, either as a flat layer or in the form of NPs, enhances reflection in comparison to the blank Al layer coated on the glass within the longer wavelength region. Again, ITO, in the form of NPs, showed better reflectance than the flat ITO layers within the same environment. This might be attributed to the better light scattering phenomenon exerted by the almost sphere-like ITO NPs than the flat morphology. The presence of discrete spherical clusters in the ITO matrix with diameters less than the wavelengths of incident light promotes the probability of localized surface plasmon resonance than the flat ITO structure, hence scattering increases in the former case [25]. It has also been observed that the ITO NPs deposited on glass/Al substrate and embedded within n-a-Si:H layer [as shown in Fig. 8(e)] have better reflectance property than the bare ITO NPs deposited on glass/Al. The n-a-Si:H coating makes the ITO NPs more confined, and hence, the scope of localized surface plasmon resonance increases in this case. The weighted average reflectance was found to be 87.63, 89.34, 96.09, 89.16, and 97.94 for the curves as presented by Fig. 9(a)–(e), respectively. This means about 11.76% and 9.62% enhancement in back reflection can be achieved by incorporating ITO NPs in n-a-Si:H layer rather than choosing the conventional bank Al or Al/ITO (flat) back reflection configurations, respectively. Thus, the ITO NPs behave like nanomirrors and reflect a notable amount of light from the rear side of the cell, mainly with longer wavelengths. Hence, it would be worth implementing such ITO NPs as the back reflectors for performance enhancement of SHJ cells fabricated on a 30-μm thin c-Si wafer.

D. Thin Film of SHJ Solar Cell With ITO NP Embedded Back Reflection Architecture

It is quite obvious that to get the maximum effect of back reflection of the unabsorbed light of the first pass from the ITO NPs, proper positioning of them in the rear side of the cell along with the other layers is very crucial. This is essential so that maximum light can be collected by the silicon wafer without hampering the other attributes of the device. In this case, three different SHJ cells were fabricated on 30-μm n-c-Si wafer by placing ITO NPs at different positions (Fig. 10) in the rear side stacks of the cells in the following ways: 1) between n-c-Si and back i-a-Si:H layers (Cell 3A); 2) between back

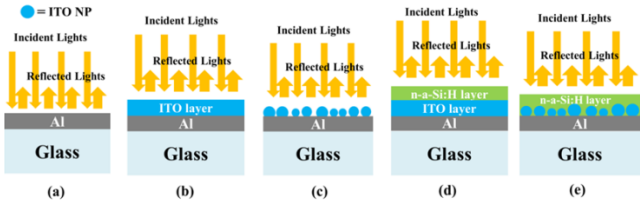

Fig. 8. Back reflection measurement configurations with five different structures. (a) Glass/Al. (b) Glass/Al/ITO layer. (c) Glass/Al/ITO NPs. (d) Glass/Al/ITO layer/n-a-Si:H layer. (e) Glass/Al/ITO NPs/n-a-Si:H layer.

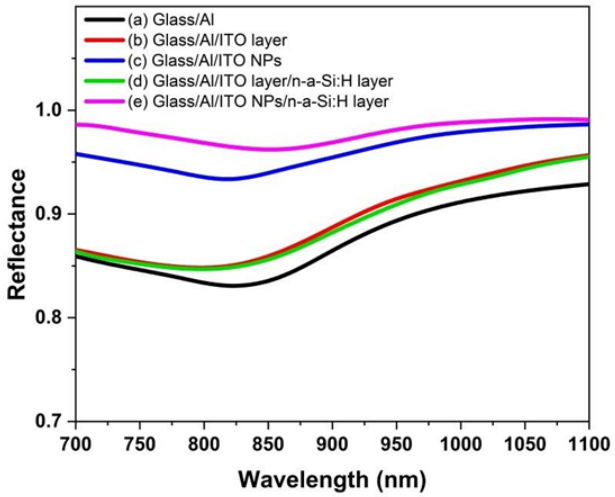

Fig. 9. Reflectance curves as obtained from the back layer configurations prepared on glass. (a) Glass/Al. (b) Glass/Al/ITO layer. (c) Glass/Al/ITO NPs. (d) Glass/Al/ITO layer/n-a-Si:H layer. (e) Glass/Al/ITO NPs/n-a-Si:H layer.

i-a-Si:H and n-a-Si:H layers (Cell 3B); and 3) embedded within n-a-Si:H layer (Cell 3C). In all cases, the ITO NPs were synthesized using the recipe as mentioned in Section III-B. A systematic investigation on the performance of these three cells (Cell 3A, Cell 3B, and Cell 3C) has been carried out and the values have been compared with Cell 2, i.e., the thin SHJ cell with no ITO NPs at the back but with all other structures as the same. The J–V curves of these four cells are presented in Fig. 11.

1) Case-I (Cell 3A): According to the back layer architecture adopted here, the light of the first pass from the n-c-Si wafer will first interact with this array of ITO NPs. In addition, these ITO NPs are at the farthermost position from the back Al/ITO layer.

Hence, the maximum reflection of the unabsorbed first pass lights will be obtained from these NPs. But placing the ITO NPs at the interface of n-c-Si and back i-a-Si:H layers will affect the surface passivation of the wafer immensely which has an adverse effect on the cell parameters as shown in Fig. 11. For this cell, the open-circuit voltage (V_{OC}) and FF were found to be 591 mV and 0.58, respectively. It can be seen (Table II) that V_{OC} and FF were affected majorly due to inferior back surface passivation occurred by the incorporation of ITO NPs at this interface, than the cell without ITO NPs, i.e., Cell 2. There is a drop in V_{OC} from 638 mV (Cell 2) to 591 mV (Cell 3A). Even the short-circuit current density (J_{SC}) was found to be reduced (29.11 mA/cm^2) compared with Cell 2

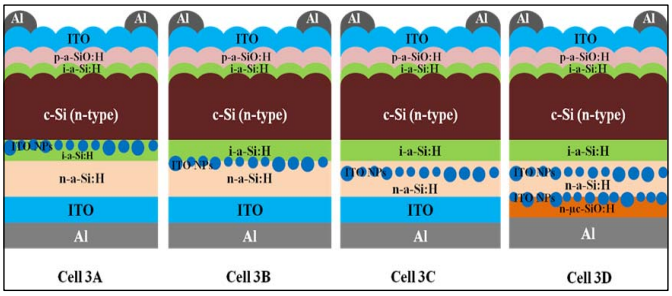

Fig. 10. Schematic showing the relative positions of ITO NPs at the rear side of the SHJ cells fabricated on a thin n-c-Si wafer.

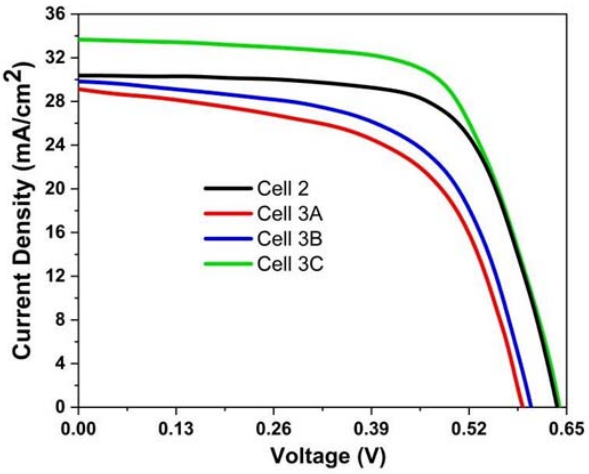

Fig. 11. J–V curves for Cell 2, Cell 3A, Cell 3B, and Cell 3C.

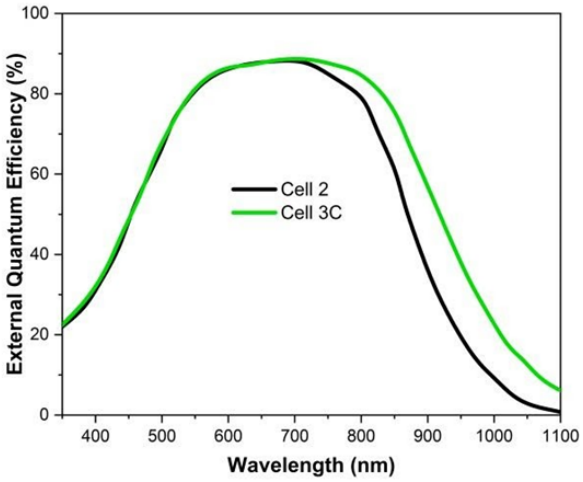

Fig. 12. EQE curves for Cell 2 and Cell 3C.

(30.36 mA/cm^2) owing to high carrier recombination caused by poor passivation at the immediate back surface of thin n-c-Si wafer. Cell 3A yielded high series resistance (R_S) with lower shunt resistance (R_{SH}) of 6.12 and 102.76 Ω, respectively. The photoconversion efficiency was 9.98% in this case.

2) Case II (Cell 3B): Due to the adverse effect of positioning the ITO NPs at the interface of n-c-Si and back i-a-Si:H layers as observed in the case of Cell 3A, now in Cell 3B, the ITO layer was placed after depositing the back i-a-Si:H layer (at the interface of back i-a-Si:H and n-a-Si:H layers) aiming at minimization of surface passivation of the crystalline wafer

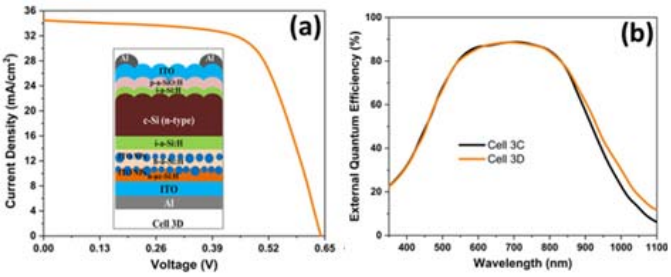

Fig. 13. (a) *J–V* characteristics (inset: schematic of Cell 3D) and (b) EQE curve for Cell 3D.

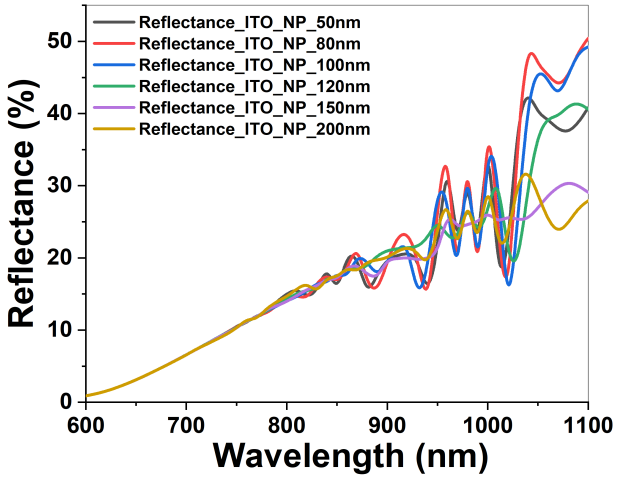

Fig. 14. Reflectance plot obtained from ITO NPs with different particle diameters adopting the architecture of Cell 3D.

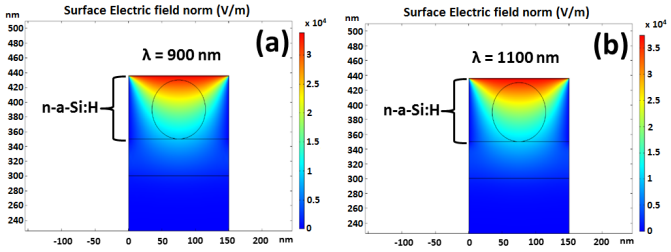

Fig. 15. Electric field profiles obtained from a single ITO NP with 80-nm diameter at two representative wavelengths of (a) 900 and (b) 1100 nm and as adopted in Case–III.

by detaching it from the ITO NPs. Eventually, it did not help much in improving the PV parameters as can be seen from Table II. This might be attributed to two factors as follows: 1) deposition of ITO layer through sputtering ruptures the very thin (5 nm) i-a-Si:H layer due to high-energy bombardment which in turn, again, results in poor surface passivation. The extent of surface passivation is somewhat better in this case that has been reflected by a nominal increase in V_{OC} and J_{SC} and 2) Ar plasma treatment to make ITO NPs from the ITO layer might cause partial crystallization of the i-a-Si:H layer which could have been the reason behind poor FF. The series and shunt resistance (5.84 and 132.54 Ω, respectively) also got some improvements than Cell 3A. Somewhat better performance of Cell 3B in comparison to Cell 3A indicates that separating the ITO layer from the n-c-Si layer has some positive influence in enhancing the cell parameters by improving

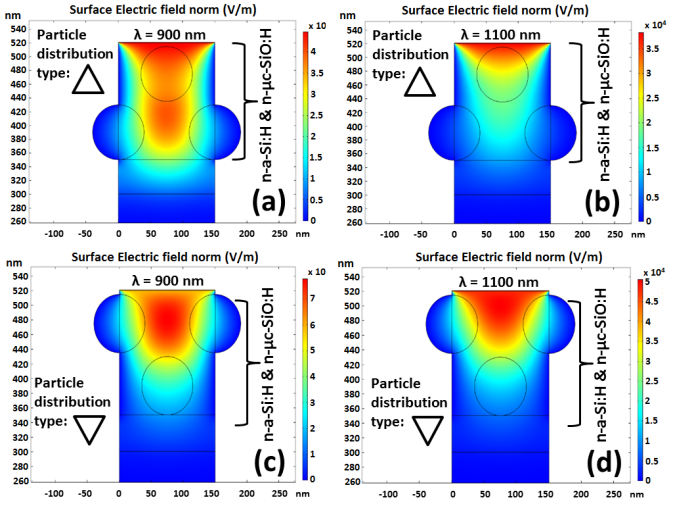

Fig. 16. Electric filed profiles at two representative wavelengths of 900 and 1100 nm obtained from the bilayer of ITO NPs with 80-nm diameter and 30-nm periodicity as adopted in Case–IV. Two types of particle distribution have been adopted for both the wavelengths. (a) and (b) Triangular. (c) and (d) Inverted triangular.

surface passivation. The photoconversion efficiency achieved for this cell architecture was 10.78%.

3) Case III (Cell 3C): In this case, the ITO NPs were embedded within the n-a-Si:H layer as shown in Fig. 10. To do so, first a 10-nm-thick n-a-Si:H layer was deposited on the i-a-Si:H layer followed by deposition of ITO NPs using the recipe as mentioned in Section III-B. Then another 15-nm layer of n-a-Si:H was deposited on it followed by complete cell fabrication. It has been found that there was a notable increase in cell parameters (Table II) that yielded a significantly high conversion efficiency of 14.73%. The result clearly shows that a balance between the optical and electrical properties of the BRL configuration has been achieved by placing the ITO NPs within the n-a-Si:H layer. According to the reflectance measurements (Fig. 9), the BRL architecture adopted in Cell 3C has a maximum back reflectance attribute than the other adopted configurations. On the other hand, sufficient separation of the ITO NPs from thin n-c-Si wafer exerts a positive impact on surface passivation and the electrical properties of the active layer. Hence, a balance between the optical and electrical properties has been established in this cell structure. The EQE curves (Fig. 12) clearly show that there is a notable increase in EQE mainly within 700–1100 nm in Cell 3C in comparison to Cell 2, which does not have any ITO NPs at the back. This might be attributed to a good amount of reflection back of transmitted light with longer wavelengths in Cell 3C, and the result is well-corroborated with the reflectance studies. It is worth mentioning here that the light reflected or scattered back by the ITO NPs will face multiple bounces within the active layer of the cell, and hence, the prospect of photocarrier generation will be increased [26].

4) Case IV (Cell 3D): The results obtained so far indicate that ITO NPs are excellent candidates in the back reflection of transmitted lights without compromising the electrical properties of the SHJ cells fabricated on 30-μm thin c-Si wafer if placed properly in the back-reflector structure. With this

improvisation, another SHJ cell, designated as Cell 3D, was fabricated on a thin n-c-Si substrate with a double array of ITO NPs as depicted in the inset of Fig. 13(a). In this case, two layers of ITO NPs separated by n-a-Si:H layer were embedded at the rear surface. The first layer of ITO NPs was embedded within the n-a-Si:H layer in a similar process as described in Case III. To embed the second layer of ITO NPs, a 20-nm ITO layer was deposited followed by Ar plasma treatment in the same chamber, and finally, those ITO NPs were covered by a 15-nm-thick n-μc-Si:H layer. The other structural attributes of the cell remained unchanged. The performance of Cell 3D was the best among the lot. It can be seen from the J–V curve [Fig. 13(a)] and Table II that inserting two layers of ITO NPs at the back did not hamper V_{OC} and FF of the cell. The shunt resistance was compromised slightly, which was countered by lowered series resistance in comparison to Cell 3C. Most importantly, there was an increment in J_{SC} from 33.80 to 34.46 mA/cm^2 (than Cell 3C) that might be attributed to better light back reflection by the double layer of ITO NPs in Cell 3D. The NPs in each layer in this case work as nanomirrors and aid multiple scattering/bounces of light within the cell. This increment in J_{SC} was further supported by the marginal enhancement in EQE in the NIR region in comparison to Cell 3C as depicted in Fig. 13(b). Eventually, Cell 3D yielded a 13.50% enhancement in J_{SC} and 12.34% increment in photoconversion efficiency than those of Cell 2, which has the same dome-like front surface but does not have ITO NPs as the back reflecting structure. From the above discussions, it is clear that SHJ solar cells on adequately thin ($\sim$30 μm) c-Si wafers can be prepared with notable photoconversion efficiency by adopting suitable front and backlight trapping architectures. Proper placing of ITO NPs at the back of the cell plays an important role in balancing between the optical and electrical properties of the fabricated cells.

E. Theoretical Analysis on Back Reflection

It has been observed from Fig. 7 that c-Si wafer with a thickness of $\sim$30 μm transmits a good amount of light in the longer wavelength region, mainly within 900–1100 nm. The entire experimental optical engineering in this work has been aimed to address this problem, which is further supported by the theoretical analysis on generation of electric field in the presence of ITO NPs, with the help of COMSOL[1] Multiphysics (Figs. 14 and 15). The finite element method (FEM)-based numerical solver has been used to study the back reflection from ITO NPs. The electromagnetic wave frequency domain (EWFD) module has been used to analyze the proposed model. Here, it is considered that the device has material homogeneity along two Cartesian axes in 3-D Euclidean space. The model is defined in 2-D ("xy" plane). The material stack is defined along the y-axis, while the model is assumed to be periodic along the x-axis. For measuring light absorption, two ports have been defined on the front and rear sides of the device within the active region of c-Si. The front port is used for excitation and the rear side port is used for measuring the back reflection of the light. This solver considers a continuous homogeneous out of the plane in the z-dimension to describe the 3-D wave. The electric field "E" in the wave equation is a constant vector defined along the z-axis to comply with the continuous boundary condition considering linear polarization. The wave vector $\boldsymbol{k}$ is calculated from frequency or wavelength, elevation angle (α_1), and azimuthal angle (α_2). To simulate the structure as mentioned in Section III-D (Fig. 10; Cell D) at the top, a $\sim$30-μm layer of c-Si layer has defined in COMSOL[1] Multiphysics. Next, a thin layer of i-a-Si:H ($\sim$5 nm) has been added at the rear of the thin c-Si layer. Subsequently, a layer of ITO NPs was added as an embedded layer within n-a-Si:H. Finally, another layer of ITO NPs was added within n-μc-SiO:H. Initially, a reflectance scan was performed within 600–1100 nm considering the bilayer of ITO NP at the rear side (Cell 3D). A wide range of ITO particle size, viz., 50, 80, 100, 120, 150, and 200 nm, was chosen for this purpose, and the plot is presented in Fig. 14. The reflectance was measured at the junction of n-c-Si and i-a-Si:H layer. The best reflection property was found to be delivered by the ITO NPs with 80- and 100-nm diameter, specifically within the longer wavelength (900–1100) region. The weighted average reflectance was calculated to be 25.27%, 27.33%, 27.06%, 24.74%, 22.26%, and 22.34% for 50, 80, 100, 120, 150, and 200 nm ITO NPs, respectively. This result clearly indicates that ITO NPs with diameter within 80–100 nm are best suitable for back reflection purpose in this case. Hence, investigations on electric field generations will be focused taking 80-nm ITO NP as the reference case in the coming section.

Fig. 15 shows the electric field profiles at two representatives longer wavelengths, viz., 900 and 1100 nm were obtained from a single ITO NP with 80-nm diameter (as adopted in Case–III). The results indicate that such ITO NPs embedded within n-a-Si:H layer can substantially reflect the light with longer wavelengths (denoted by red regions) near the junction of i-a-Si:H and n-c-Si. The structure becomes complex when the bilayer of ITO NPs is adopted as per Case–IV. In this case, the ITO NPs can be arranged in two most possible ways, viz., triangular [Fig. 16(a) and (b)] and inverted triangular [Fig. 16(c) and (d)] arrangements keeping one ITO NP on the top and the other two at the bottom and two ITO NPs on the top and one at their bottom, respectively. The diameter of the ITO NPs and periodicity of them were taken as 80 and 30 nm, respectively. For the triangular distribution, the electric field intensity was found to be generated within the NP array, which also covers the top of this particular host zone for the incident light with a wavelength of 900 nm [Fig. 16(a)]. Prominent shifting of this electric field intensity toward the top of this host-zone, i.e., near to the junction, was observed for the light with wavelength 1100 nm [Fig. 16(b)]. For the inverted triangular arrangement of ITO NPs, the generation of electric field intensity was within the NP array but slightly shifted near to the top of this host zone at 900 nm [Fig. 16(c)]. However, at 1100 nm, the shifting of electric field intensity toward the top of this host-zone was prominent [Fig. 16(d)]. With the help of this theoretical analysis, it has further been proved that the synthesized ITO NPs, both as a discrete unit and also in a bilayer structure, can prominently reflect the photons with longer wavelengths closer to the junction of this

[1]Trademark.

SHJ architecture as denoted by the generation and shifting of the electric field intensity. It is evident from the results obtained from simulated structures (Figs. 15 and 16) that the back reflection capability of bilayer NP is more than that of a single layer, leading to an enhancement of light from the back of the cell and yielding a significant increase in J_{SC} from 33.80 to 34.46 mA/cm^2.

Using COMSOL[1] Multiphysics, weighted average absorbance (over 300–1100 nm wavelength region) was also calculated in the active region considering the following three cases: 1) without any NP layer at the rear (Cell 2); 2) single ITO NP layer (Cell 3C); and 3) bilayer of ITO NP at the rear side (Cell 3D); and the values were found to be 0.5742, 0.6253, and 0.6399, respectively. Therefore, it may be concluded that incorporation of bilayer ITO NPs at the rear side of such cell can produce a better back reflection of light which is again supported by the highest weighted average absorbance observed within the active region of the cell.

IV. Conclusion

SHJ solar cells on adequately thin (∼30 μm) n-c-Si wafer were fabricated as a proof-of-concept scheme. To address the light-trapping-related issues in thin c-Si substrates without compromising the electrical properties of the device, proper measures such as "doming" of the pyramidal front textures and the use of ITO NPs as the back reflector material have been adopted. In comparison to only Al or Al/ITO back reflector structure, the ITO NPs showed a better back reflection of transmitted light in longer wavelengths, resulting in a notable enhancement in photoconversion efficiency.

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