Chapter 2

Electrolytic Capacitor-Less Isolated DC-DC Resonant Converters

2.1 Introduction

This chapter discusses the design and operation of two electrolytic capacitor-less isolated DC-DC resonant converters. The circuital operation and mathematical modeling of the proposed converter are explained. Based on the mathematical analysis presented, proposed converters are optimally designed to operate with soft-switching for the full load of range. The conditions for the soft-switching operations are formulated. Later in the chapter, a 500 W laboratory prototype of the proposed converter is developed. To verify the efficacy of the mathematical modeling and soft-switching operation, the theoretically formulated data is compared with the simulation and experimental results for 100% and 20% of load at steady-state conditions.

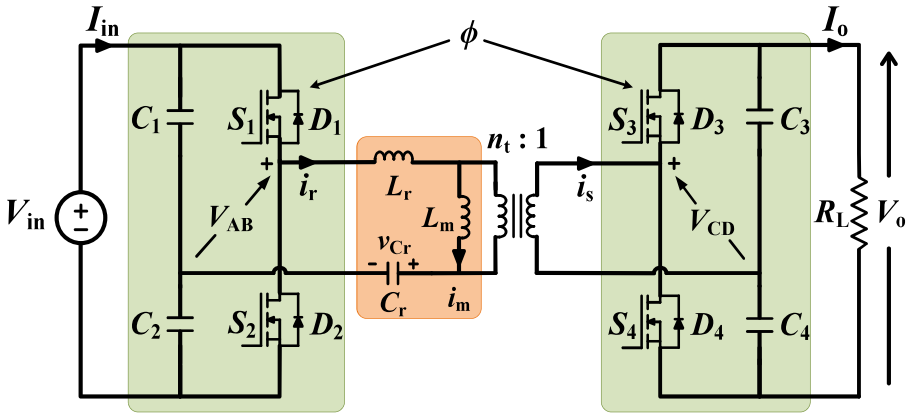


Fig. 2.1 Circuit diagram of the dual half active bridge resonant converter.

2.2 Proposed Converter -1 (Dual-Half Active Bridge Resonant Converter)

The circuit diagram for the proposed dual half-active bridge resonant converter (DHABRC) is shown in Fig. 2.1. The proposed converter consists of two half-active bridges isolated from a high-frequency transformer (HFT). The leakage and mutual inductance of the HFT are utilized as tank components of the *LLC*.

2.3 Operation of the Proposed DHABRC

The steady-state waveform for the proposed converter is shown in Fig. 2.2. From the waveform, it can be observed that all switches operate with a duty cycle of 50%, but there is a phase shift ϕ between the primary and secondary bridge switches. This causes the primary and secondary bridge voltages V_{AB} and V_{CD} to fluctuate with a magnitude of half of the input voltage V_{in} and output voltage $V_{o,}$ respectively. The resonant tank comprises resonant inductance L_r, parallel inductance L_m, and resonant capacitance C_r. The resonance causes the resonant current i_r and the secondary current i_s to be approximately sinusoidal. The parallel inductor current i_m is triangular in shape because of the square waveform of V_{CD} appearing across it. The switching frequency f_s is kept greater than the resonant frequency f_r so the resonant current i_r operates in continuous current mode. The operating waveforms for the operation of the DHABRC can be explained in 8 different intervals.

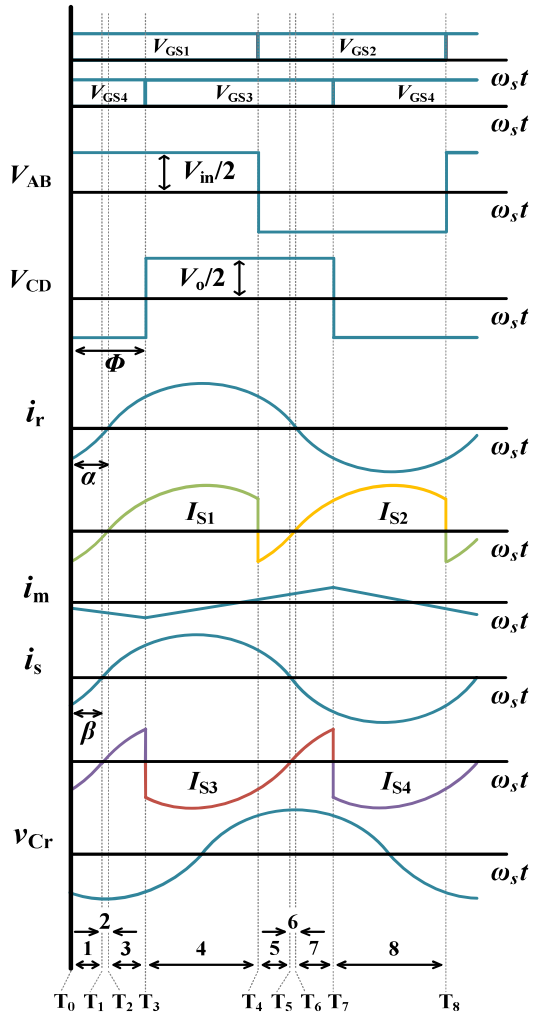


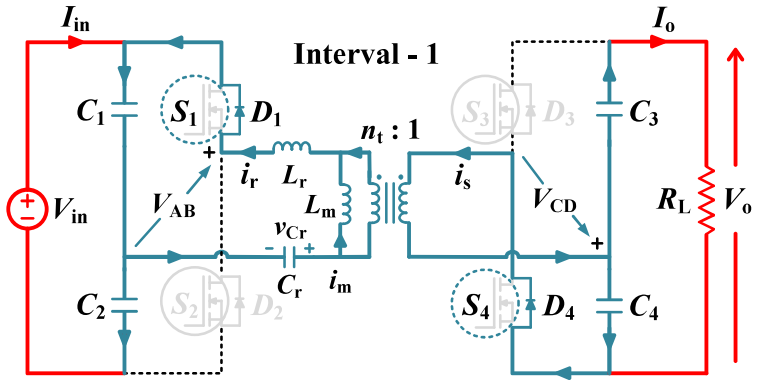
Fig. 2.2 Key operating waveform for the DHABRC.

2.3.1 Interval 1: ($T_0 - T_1$) Fig. 2.3 (a)

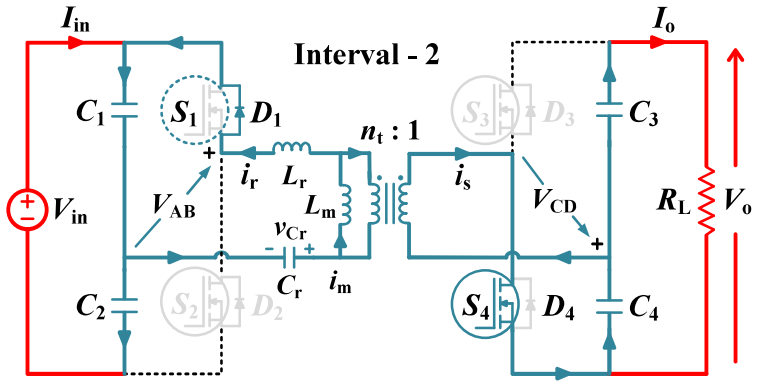
This interval starts when the gate signal is given to switch S_1 and switch S_4 is already in on state. The primary bridge voltage V_{AB} is positive, and the secondary bridge voltage V_{CD} is negative. In this interval, the tank circuit releases its energy, making the resonant current i_r negative. The parallel inductor current i_m will continue to decrease because of voltage $-V'_{CD}$ across it. The secondary current ($i_s = i_r - i_m$) can be obtained using the KCL. Since the currents i_r and i_s are flowing in the negative direction, the body diodes D_1 and D_4 of switches S_1 and S_4 will conduct the current. The resonant capacitor voltage V_{Cr} will also increase in sinusoidal nature, lagging behind i_r by 90°. This interval ends when the i_s reduced to zero.

2.3.2 Interval 2: ($T_1 - T_2$) Fig. 2.3 (b)

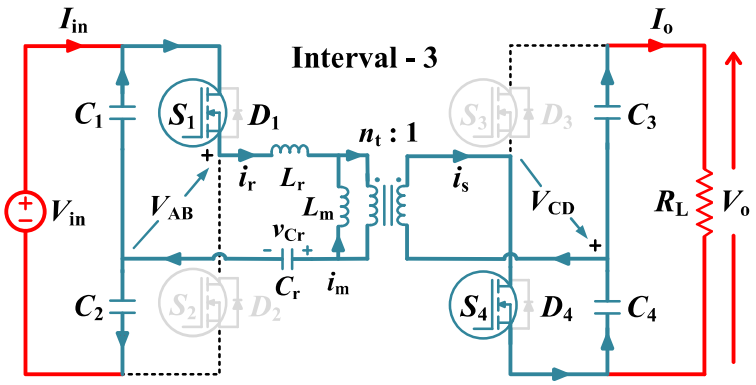
The switching status in this interval will be similar to the previous interval. Now, the current i_m becomes greater than i_r and i_s starts to build in the positive direction. Since the body diode D_4 conducts the current before the switch S_4, it will be turned on with ZVS. It can be seen from Fig. 2.2 that the current i_s is lagging behind the voltage V_{AB} by an angle of β. Finally, the resonant current i_r will be zero.



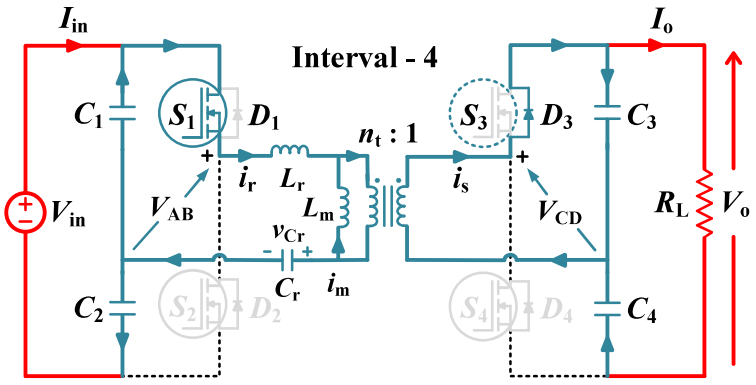
(a)



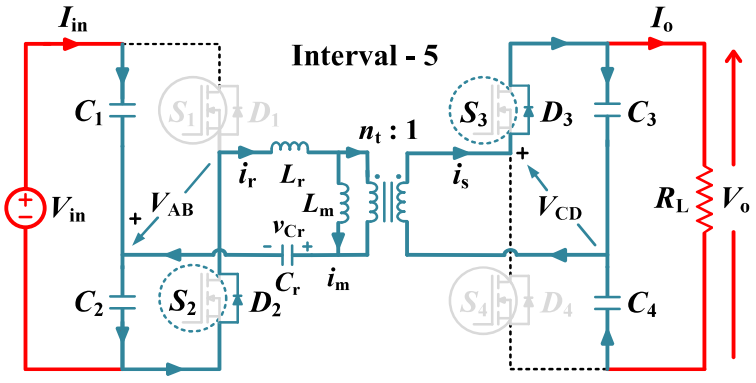
(b)


Interval - 3
I_{in}
I_o
C_1
S_1
D_1
$n_t : 1$
S_3
D_3
C_3
V_{in}
V_{AB}
i_r
L_r
L_m
i_s
V_{CD}
R_L
V_o
v_{Cr}
C_r
i_m
C_2
S_2
D_2
S_4
D_4
C_4

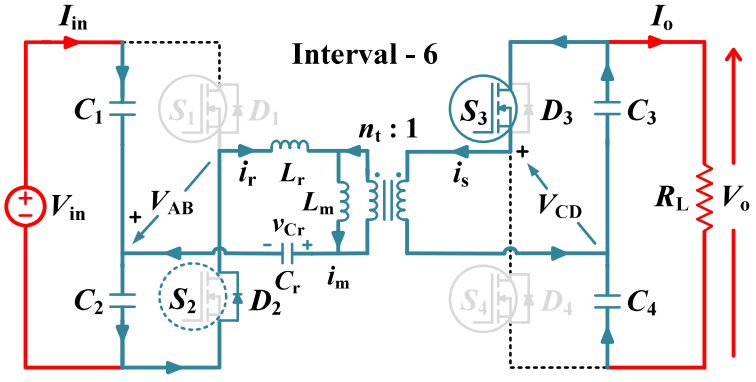
(c)


Interval - 4
I_{in}
I_o
C_1
S_1
D_1
$n_t : 1$
S_3
D_3
C_3
V_{in}
V_{AB}
i_r
L_r
L_m
i_s
V_{CD}
R_L
V_o
v_{Cr}
C_r
i_m
C_2
S_2
D_2
S_4
D_4
C_4

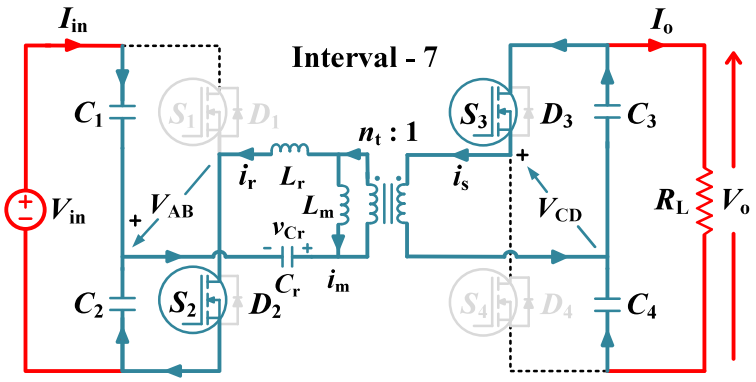
(d)


Interval - 5
I_{in}
I_o
C_1
S_1
D_1
$n_t : 1$
S_3
D_3
C_3
V_{in}
V_{AB}
i_r
L_r
L_m
i_s
V_{CD}
R_L
V_o
v_{Cr}
C_r
i_m
C_2
S_2
D_2
S_4
D_4
C_4

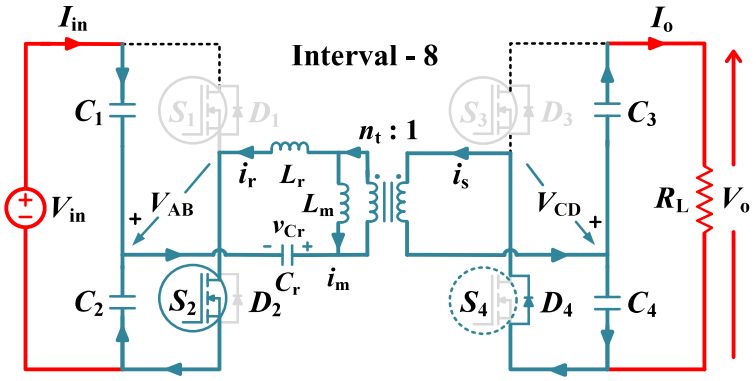
(e)


Interval - 6
I_{in}
I_o
C_1
S_1
D_1
$n_t : 1$
S_3
D_3
C_3
V_{in}
V_{AB}
i_r
L_r
L_m
i_s
V_{CD}
R_L
V_o
v_{Cr}
C_r
i_m
C_2
S_2
D_2
S_4
D_4
C_4

(f)



(g)



(h)

Fig. 2.3 Operation of the circuit in different operating intervals.

2.3.3 Interval 3: ($T_2 - T_3$) Fig. 2.3 (c)

Now, the resonant current i_r will become positive in this interval, and the tank circuit will start storing the energy. The current i_r will lag behind the voltage V_{AB} by an angle of α. The switch S_1 will conduct the current. Since the body diode D_1 of switch S_1 conducts the current before the switch, it will be turned on with ZVS. At the end, the gate signal is removed from S_4.

2.3.4 Interval 4: ($T_3 - T_4$) Fig. 2.3 (d)

In this interval, the gate signal has now been given to S_3. The secondary bridge voltage V_{CD} will become positive. Since the secondary current i_s is positive, the body diode of switch S_3 will conduct the current. At the end, the gate signal is removed from switch S_1. Since the waveforms are symmetrical, the rest of the intervals can be explained similarly.

2.3.5 Interval 5: ($T_4 - T_5$) Fig. 2.3 (e)

Now, in this interval, the gate signal is given to S_2, and the primary bridge voltage will become negative. Since the current i_r is positive the current will flow through the body diode D_2 of the switch S_2. The parallel inductor current i_m will continue to increase because of the positive voltage + V_{CD}' appearing across it. At the end of this interval, the secondary current i_s will become zero as the resonant current i_r will become equal to i_m.

2.3.6 Interval 6: ($T_5 - T_6$) Fig. 2.3 (f)

In this interval, the switching status will remain the same. Now, as the secondary current i_s changes its direction, the switch S_3 will start to conduct the current. Since the body diode of S_3, conducts the current before the switch, it will turn on with ZVS. At the end of this interval, the resonant current will be reduced to zero.

2.3.7 Interval 7: ($T_6 - T_7$) Fig. 2.3 (g)

Now, as the direction of the resonant current i_r is changed, the switch S_2 will start to conduct the current and turn it on with ZVS. At the end of this interval, the gate signal is removed from switch S_3.

2.3.8 Interval 8: ($T_7 - T_8$) Fig. 2.3 (h)

In this interval, the gate signal is given to S_4, and the secondary bridge voltage will become negative. Since the current i_s is flowing in the negative direction, the body diode of D_4 will conduct the current. The parallel inductor current i_m will start to reduce since the negative voltage is appearing across it.

2.4 Proposed Converter -2 (Asymmetrical Dual Active Bridge Resonant Converter)

The circuit diagram for the asymmetrical dual active bridge resonant converter (ADABRC) is shown in Fig. 2.4. The ADABRC consists of one full active bridge at the input side and one half-active bridge at the output side, isolated from a high-frequency transformer (HFT) and an *LLC* resonant tank. The leakage and mutual inductance of the HFT are utilized

as resonant tank components, and a series film capacitance (C_r) is added that acts like a DC blocking component, avoiding the saturation of the HFT.

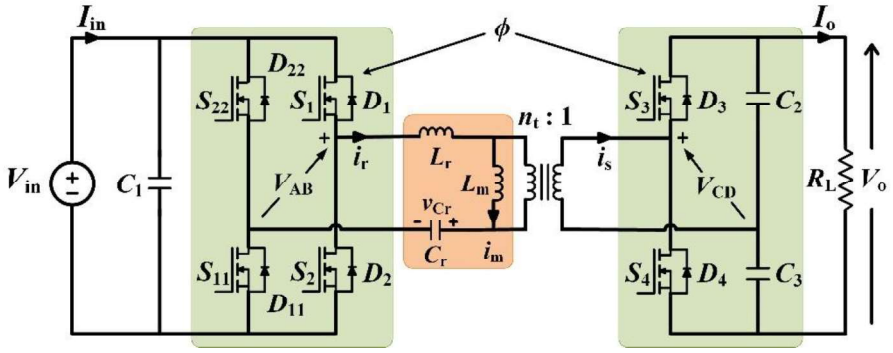


Fig. 2.4 Circuit diagram of the proposed converter ADABRC.

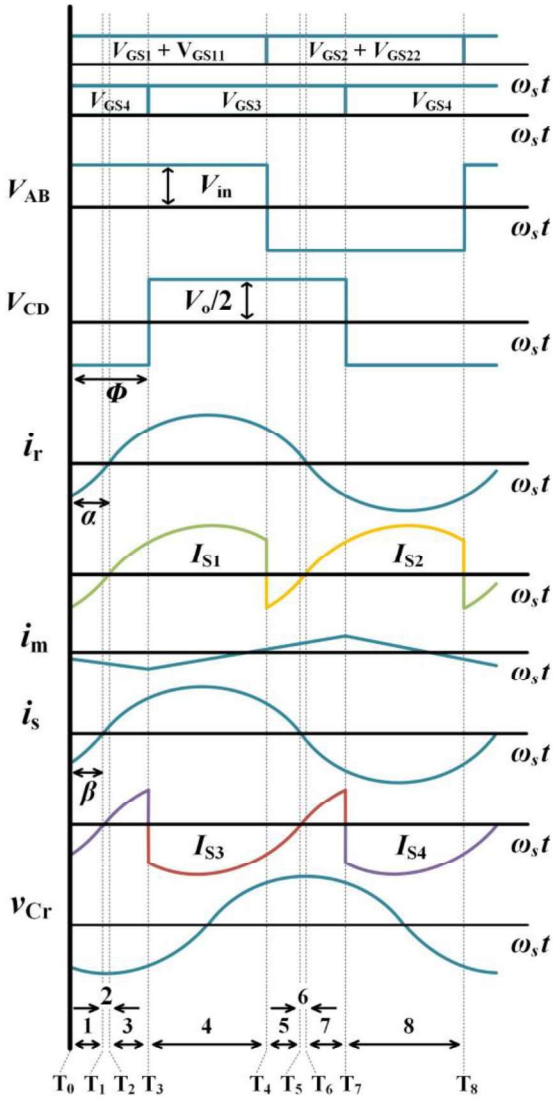


Fig. 2.5 Key operating waveform for the ADABRC.

2.5 Operation of the Proposed ADABRC

All the active switches in the ADABRC operate with a 50% duty cycle, but a phase shift exists between the primary and secondary bridge switches, as shown in Fig. 2.5. This causes the primary and secondary bridge voltages V_{AB} and V_{CD} to fluctuate with a magnitude of the input voltage ± V_{in} and half of the output voltage ± V_o/2, respectively. Resonance within the ADABRC results in approximately sinusoidal waveforms for the resonant current i_r and the secondary current i_s. The parallel inductor current i_m, however, exhibits a triangular shape due to the square-wave nature of the voltage V_{CD} across it. The operating waveforms of the ADABRC can be explained in eight different intervals, similar to the DHABRC.

2.6 Steady-State Analysis of Proposed Resonant Converters Using FHA

The resonant converters can be analyzed using two different approaches: the state space approach and fundamental harmonics approximation (FHA) or the complex AC circuit analysis approach. Although the state space approach is more accurate, it becomes cumbersome when the number of reactive components is high. The FHA approach involves the Fourier series and considers only the fundamental component of different variables. So, it will provide a compromised solution for resonant converters. The FHA equivalent circuit for the DHABRC is shown in Fig. 2.6.

2.6.1 Mathematical Model

For the designing purpose, calculations have been done in per unit values, and the base values are chosen to normalize the different parameters with respect to the angular resonant frequency $\omega_r = 2\pi f_r$ are the following.

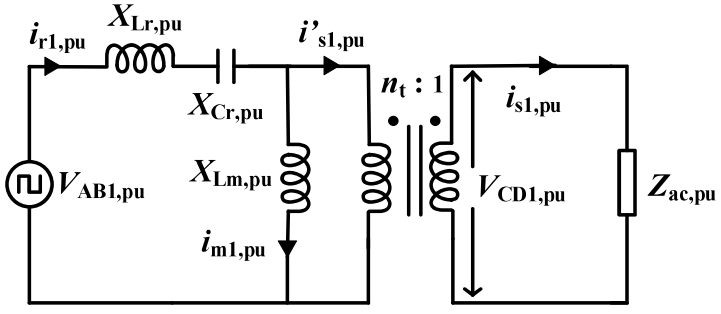


Fig. 2.6 FHA equivalent diagram of the DHABRC.

$$V_B = V_{in},\ Z_B = \sqrt{\frac{L_r}{C_r}},\ I_B = \frac{V_B}{Z_B} \text{ and } \omega_B = \omega_r \tag{2.1}$$

In equations, the subscript (‘) denotes that the parameter is referred to the primary side. The gain of the converter is given by:

$$M = \frac{V_o^{'}}{V_{in}} \tag{2.2}$$

Similarly, different tank reactance can be normalized as:

$$X_{Lr,pu} = F\ , X_{Cr,pu} = \frac{1}{F}\text{, and } X_{Lm,pu} = \frac{F}{K} \tag{2.3}$$

where $K = \frac{L_r}{L_m}$ and F is the normalized switching frequency given as (2.4).

$$F = \frac{\omega_s}{\omega_r} \tag{2.4}$$

where $\omega_s = 2\pi f_s$ is the switching angular frequency.

Using the Fourier series, the primary and secondary bridge voltages can be given as:

$$V_{AB}(t) = \sum_{n=1.3...}^{\infty} \frac{2V_{in}}{n\pi} \sin\left(n\omega_s t\right) \tag{2.5}$$

$$V_{CD}(t) = \sum_{n=1.3...}^{\infty} \frac{2V_o}{n\pi} \sin\left(n\omega_s t - n\phi\right) \tag{2.6}$$

2.6.2 Bridge Currents and Voltages

The tank currents can be calculated using the superposition principle. From Fig. 2.6. the resonant current can be given by (2.7).

$$i_{r,pu}(t) = \frac{V_{AB1,pu}(t) - V_{CD1,pu}^{'}(t)}{(F - 1/F)} \tag{2.7}$$

The resonant current can further be simplified as

$$i_{r,pu}(t) = i_{rp} \sin\left(\omega_s t - \alpha\right) \tag{2.8}$$

where $i_{rp} = \left(\frac{2\sqrt{1 + M^2 - 2M\cos\phi}}{\pi\left(F - 1/F\right)} \right)$ (2.9)

and $\alpha = \tan^{-1}\left(\left(\frac{\csc\phi}{M}\right) - \cot\phi\right)$ (2.10)

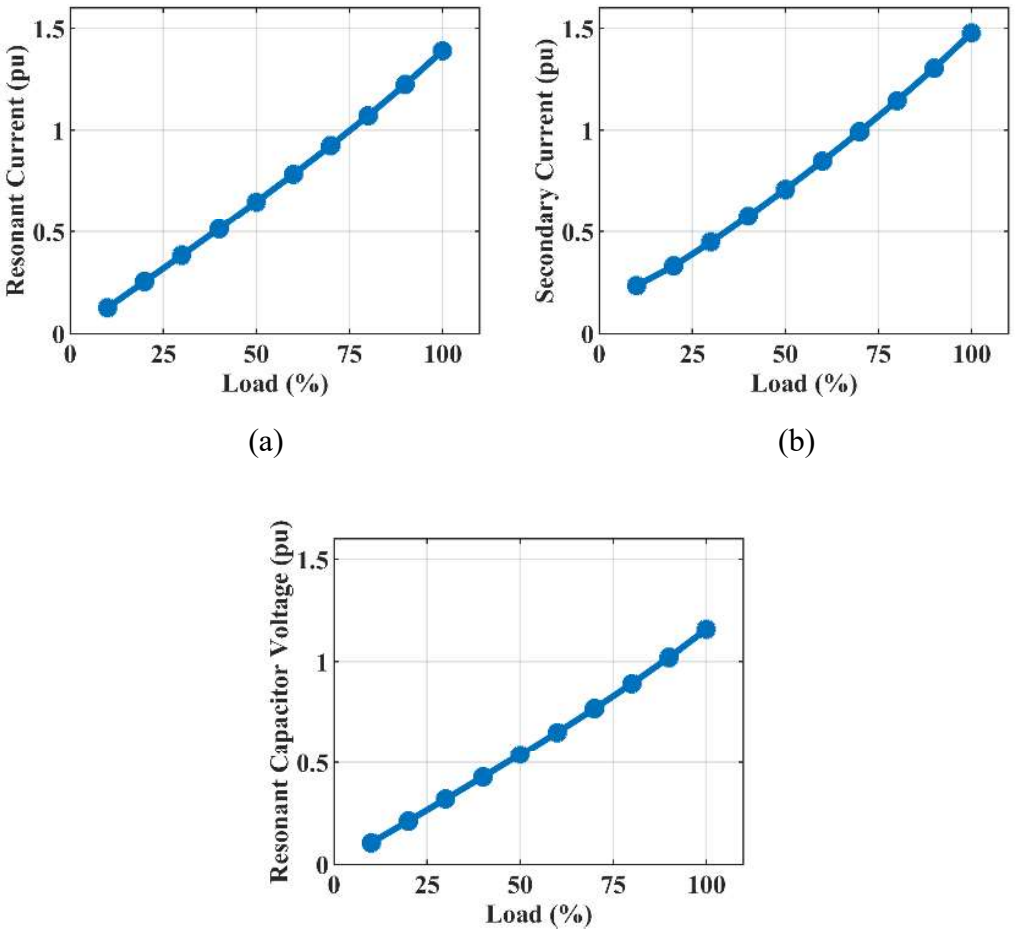
Here the angle α also represents the input impedance angle. Similarly, the secondary current can be written as:

$$i'_{s,pu}(t) = \frac{V_{AB1,pu}(t)}{(F - 1/F)} - \frac{V'_{CD1,pu}(t)}{(F - 1/F) \| (F/K)} \tag{2.11}$$

The secondary current can further be simplified as follows:

$$i'_{s,pu}(t) = i_{sp} \sin(\omega_s t - \beta) \tag{2.12}$$

where $i_{sp} = 2\frac{\sqrt{1 + (MX)^2 - 2MX\cos\phi}}{\pi(F - 1/F)}$ (2.13)



(a) (b)

(c)

Fig. 2.7 Variation of resonant parameters (a) Peak resonant current. (b) Peak secondary current. (c) Peak resonant capacitor voltage (all in per unit) with load.

$$X = \left(\frac{F - 1/F}{(F - 1/F) \,\|\, (F/K)} \right)$$

$$\beta = \tan^{-1}\left(\frac{(F/K)\csc\phi}{M\left(F - 1/F + F/K\right)} - \cot\phi \right) \tag{2.14}$$

The variation of the resonant current i_r and secondary current i_s with load is shown in Fig. 2.7 (a) and (b). The voltage across the resonant capacitor will also be sinusoidal, and its peak value can be given as

$$V_{Crp} = 2\frac{\sqrt{1 + M^2 - 2M\cos\phi}}{\pi(F^2 - 1)} \tag{2.15}$$

The variation of the resonant capacitor voltage V_{Cr} with load is shown in Fig. 2.7 (c). The relationship between the per-unit power transfer and the phase-shift angle can be given as

$$P_{pu} = \frac{1}{2\pi}\int_0^{2\pi} (V_{CD1} i_s)_{pu} d(\omega_s t) = \frac{2M}{\pi^2 (F - (1/F))}\sin(\phi) \tag{2.16}$$

2.6.3 Equivalent AC Impedance

For analyzing the resonant converter, the secondary side circuit (including half active bridge, capacitive filter, and resistive load) must be represented as an equivalent resistance. In conventional resonant converters, for diode full bridge configuration, it was described as $R_{ac} = \frac{8R_L}{\pi^2}$. Similarly, for half active bridge configuration, it will be given as:

$$Z_{ac} = \frac{2R_L\cos\theta}{\pi^2} \tag{2.17}$$

Here, $\theta = \phi - \beta$ is the phase angle of the equivalent impedance. This modification will be used for the calculation in this topology. It has been found that in previous literature, this modification works fairly for steady-state analysis of all types of tank circuits [19], [22]. Using (2.17), the relationship between the impedance angle θ and the controllable phase-shift angle ϕ can be given as:

$$\theta = \tan^{-1}\left(M\left(1 + \frac{F - 1/F}{F/K}\right)\csc\phi - \cot\phi \right) \tag{2.18}$$

2.6.4 Gain of the Converter

Using (2.2) and Fig. 2.6, the converter gain M can be given as:

$$M = \frac{Z'_{ac,pu} \,\|\, (F/K)}{(F - 1/F) + Z'_{ac,pu} \,\|\, (F/K)} = f(\theta) \tag{2.19}$$

Since the angle θ is not a directly controllable parameter. So, using (2.2), (2.17), and (2.18), it can be further normalized as:

$$M = \frac{\sin\phi}{Q(F - 1/F)} \tag{2.20}$$

From (2.20), it can be seen that the converter gain M is independent of the inductance ratio K. It is the function of quality factor Q and phase shift angle. So, by changing the phase shift angle, the converter gain can be kept constant for a change in load level.

2.6.5 Necessary Condition for ZVS

The efficiency of a converter can be improved by reducing the switching losses. Soft-switching can be obtained by controlling the gain and the angles of different currents. On the primary side, ZVS can be observed only if the tank resonant current i_r is inductive. Using (2.10), it can be given as $\alpha > 0$.

$$M < \sec\phi \tag{2.21}$$

Since the minimum value of $\sec\phi$ is 1, the ZVS in the primary bridge can be obtained for any phase shift if $M \leq 1$. Similarly, ZVS can be obtained on the secondary side if the secondary current is leading ahead of the secondary bridge voltage V_{CD}. Using (2.18), it gives the condition:

$$M > \frac{\cos\phi}{1 + K - K/F^2} \tag{2.22}$$

From (2.22), it can be observed that the ZVS condition at the secondary side is the function of normalized switching frequency, converter gain M, and inductance ratio K. Here, (2.21) and (2.22) provide only the necessary conditions for operating the converter within the safe limits of ZVS and don't consider the effect of the dead time under different magnetizing inductances value. To operate the active switches with complete ZVS, the sufficient condition implies that the value of inductive current should be high enough to charge and discharge the voltage of the junction capacitors (parasitic capacitances) [29]. Also, the minimum time required to reduce the junction voltage to zero will give the minimum dead time required for the active switches.

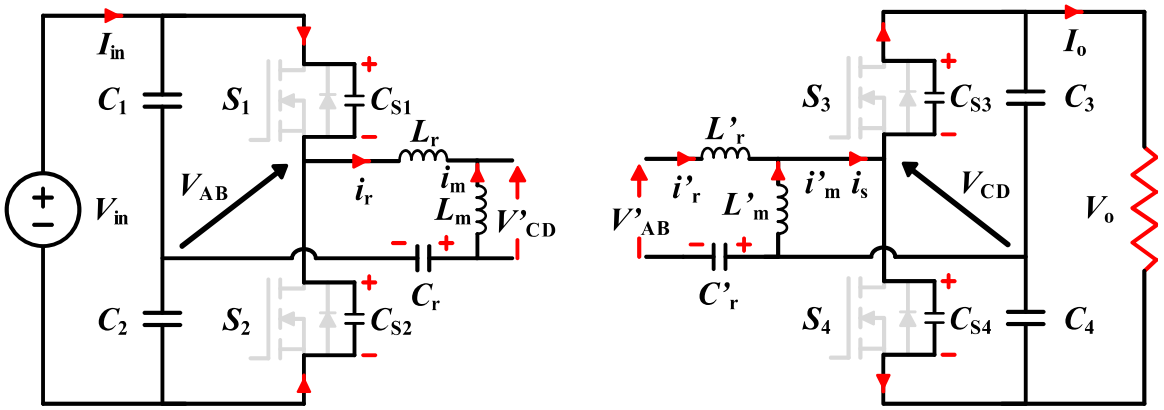


Fig. 2.8 Equivalent circuit diagram for an intermediate switching transition state (a) Just before turning switch S_2 on. (b) Just before turning S_3 on.

2.6.6 Sufficient Condition for ZVS and Effect of Dead Time

An intermediate switching transition instant happening between interval 4 and interval 5 (Fig. 2.2) is chosen to analyze the junction voltage on the primary side. In between these intervals, the gating signal of switch S_1 is removed and given to switch S_2. In Fig. 2.8 (a), an equivalent circuit of the proposed converter is shown that represents an intermediate transition state just before turning on the switch S_2. It can be seen from Fig. 2.8 (a) that the resonant current i_r charges C_{S1} and discharges C_{S2} of switches S_1 and S_2, respectively. The voltage across the film capacitors C_1 and C_2 is fixed and equal to V_{in} /2. The dynamic equation for the intermediate transition state can be given as follows.

$$\frac{V_{in}}{2} - V_{C_{S2}}(t) + L_r \frac{di_r(t)}{dt} + n_t V_{CD} + \frac{1}{C_r}\int i_r(t)\,dt = 0 \tag{2.23}$$

$$i_r(t) = -(C_{S1} + C_{S2})\frac{dV_{C_{S2}}(t)}{dt} \tag{2.24}$$

After solving (2.23) and (2.24), the expression of junction voltage is obtained as (29).

$$V_{C_{S2}}(t) = A + B(1 - \cos(\omega_{zp} t)) + C\sin(\omega_{zp} t) \tag{2.25}$$

The constants are defined in the below. The minimum time required to reduce the voltage to zero can be given as follows.

$$t_P = \frac{1}{\omega_{zp}}\left(\tan^{-1}\left(\frac{B}{C}\right) - \sin^{-1}\left(\frac{A+B}{\sqrt{B^2+C^2}}\right)\right) \tag{2.26}$$

Here $A = V_{in}$, $B = \frac{C_r V_{Cr}(t_4)}{(C_r + 2C_{S1})}$, $C = -\frac{i_r(t_4)}{2C_{S1}\omega_{zp}}$, $V_{Cr}(t_4) = V_{Crp}\cos(\alpha)$, $i_r(t_4) = i_{rp}\sin(\alpha)$

and $\omega_{zp} = \sqrt{\frac{C_r + 2C_{S1}}{2L_r C_r C_{S1}}}$.

By adding (2.26) with the turn-off delay time, the minimum dead time for the primary switches can be calculated as –

$$T_{Dp} = t_P + t_{Doff\_S1/S2} \tag{2.27}$$

Similarly, the junction voltage on the secondary side is calculated for an intermediate switching transition instant happening between interval 3 and interval 4. In between these intervals, the gating signal of switch S_4 is removed and given to switch S_3. In Fig. 2.8 (b), an equivalent circuit of the proposed converter is shown that represents an intermediate transition state just before turning on the switch S_3. It can be seen from Fig. 2.8 (b) that the secondary current i_s charges and discharges the capacitances C_{S4} and C_{S3} of switches S_4 and S_3, respectively. The voltage across the film capacitors C_3 and C_4 are fixed and equal to $V_o/2$. For the transition state, the dynamic equation can be given as follows.

$$\frac{V_{AB}}{n_t} - \frac{L_r}{n_t}\frac{d\,i_r(t)}{dt} + V_{C_{S3}}(t) - \frac{V_o}{2} - \frac{1}{n_t C_r}\int i_r(t)\,dt = 0 \tag{2.28}$$

$$n_t\left(i_r(t) - \left(i_{m\phi} - \frac{n_t V_o}{2L_m}t\right)\right) = -(C_{S3} + C_{S4})\frac{dV_{C_{S3}}(t)}{dt} \tag{2.29}$$

To simplify the equation, the Taylor series expansion is used, and after solving it, we get the junction voltage expression as

$$V_{C_{S3}}(t) = (A' - C')\cos(\omega_{zs}t) + B'\sin(\omega_{zs}t) + C' \tag{2.30}$$

The constants are defined below. The minimum time required to reduce (2.30) to zero can be given as

$$t_S = \frac{1}{\omega_{zs}}\left(\tan^{-1}\left(\frac{C' - A'}{B'}\right) + \sin^{-1}\left(\frac{-C'}{\sqrt{B'^2 + (A' - C')^2}}\right)\right) \tag{2.31}$$

Here $A' = V_o$, $B' = \frac{n_t\left(i_{m\phi} - i_r(\phi)\right)}{2\,\omega_{zs} C_{S3}}$, $C' = \frac{1}{\omega_{zs}^2}\left(\frac{n_t V_{Cr}(\phi)}{2L_r C_r} + \frac{A'}{L_r C_r} - \frac{n_t^2 A'}{4L_m C_{S3}}\right)$, $i_r(\phi) = i_{rp}\sin(\phi - \alpha)$

$V_{Cr}(\phi) = -V_{Crp}\cos(\phi - \alpha)$, and $\omega_{zs} = \sqrt{\frac{n_t^2 C_r + 2C_{S3}}{2L_r C_r C_{S3}}}$.

By adding (2.31) with the turn-off delay time, the minimum dead time for the secondary switches can be calculated as -

$$T_{D\_S} = t_S + t_{Doff\_S3/S4} \tag{2.32}$$

The analysis presented above shows that the dead time and ZVS range of the primary bridge switches are independent of the magnetizing current or mutual inductance. However, the magnetizing current discharges the junction capacitance faster for the secondary side, increasing the ZVS region to improve the converter's efficiency.

2.7 Design Optimization for the Proposed Converter DHABRC

To illustrate the efficacy of the analysis presented, a 500 W prototype of the proposed DHABRC is designed for 50 kHz operation with an input voltage of V_{in} = 140 V to provide an output voltage of V_o = 115-125 V. The details of optimally designed parameters are given as follows:

2.7.1 Selection of Normalized Switching Frequency (F)

The normalized switching frequency (F) is a crucial parameter as it appears in the ZVS condition of active bridges. Also, the values of resonant inductance and resonant current value can be reduced by selecting its small value. Common practice shows that a fixed frequency resonant converter should be in the range of 1.05 – 1.2 to keep the input impedance inductive. From (2.10) and (2.20), a 3D plot for the input impedance angle varying with F and gain is drawn and shown in Fig. 2.9 (a). For the design purpose, F = 1.2 is chosen with a safe limit to keep the input impedance angle lagging for ZVS operation.

2.7.2 Selection of the Quality Factor (Q)

The quality factor of a resonant converter is a crucial parameter as it decides the size of the reactive components and the magnitude of the different resonant currents. The quality factor

for the proposed converter DHABRC can be given as (2.33). After multiple iterations, the value of the quality factor is selected as 2 for the proposed converter.

$$Q = \frac{\pi^2 Z_B}{2n_t^2 R_L} \tag{2.33}$$

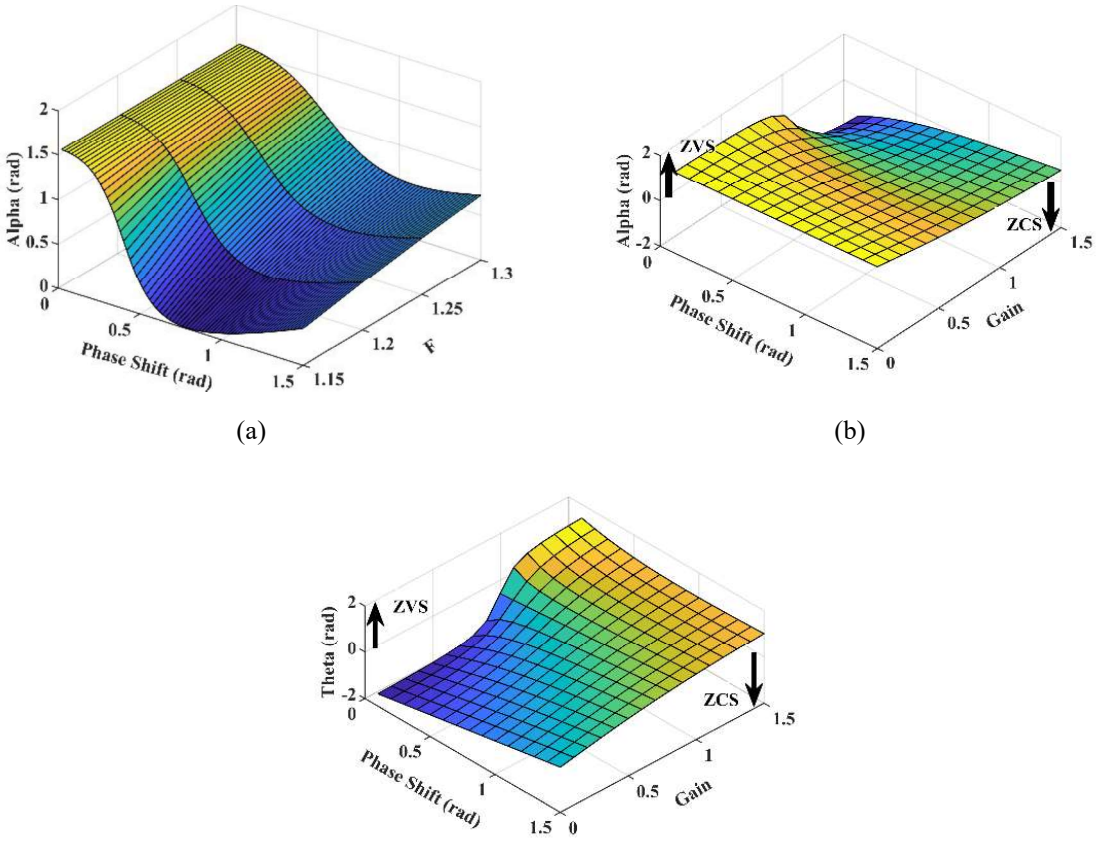


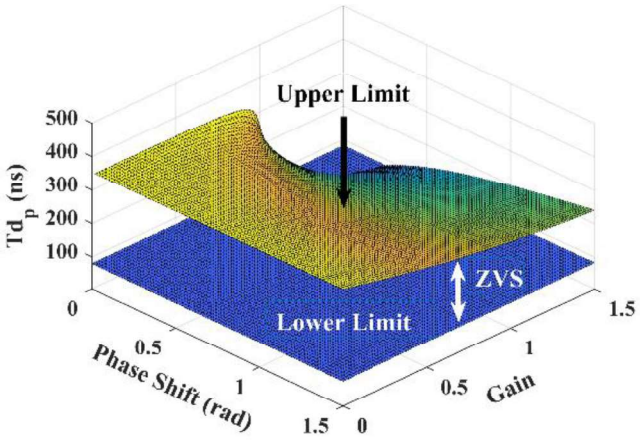
Fig. 2.9 Plot for ZVS operating Region showing the variation of (a) Input impedance angle (α) with phase-shift angle and normalized switching frequency. (b) ZVS conduction region on the primary side. (c) ZVS conduction region on the secondary side.

2.7.3 Selection of Converter Gain (M)

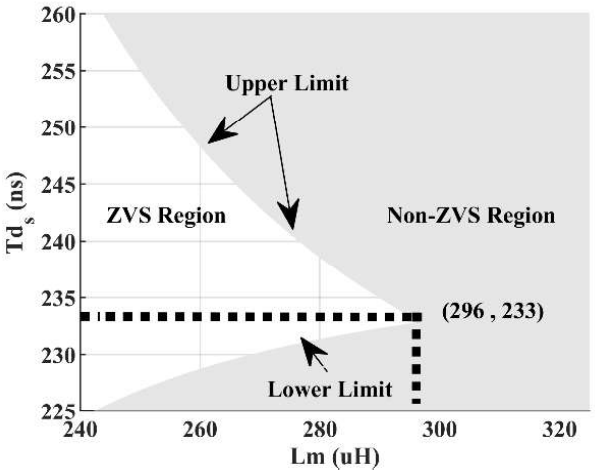
The soft-switching condition shows that ZVS could be attained for all loads and output voltage of the working range by selecting a proper value of converter gain *M*. From (2.10) and (2.18), it can be observed that when the M >1, ZVS will be lost. So, with $M_{\max}$ = 1, the turns ratio can be calculated as

$$n_t = \frac{V_{in} M_{\max}}{V_{o\max}} \tag{2.34}$$

In Fig. 2.9 (b)-(c), the range of the ZVS conduction region for different values of the converter gain and controllable phase-shift angle are shown for the primary side and the secondary side switches.



(a)



(b)

Fig. 2.10 Variation of dead time with (a) ZVS on the primary side. (b) Magnetizing inductance (L_m) for the ZVS region on the secondary side.

2.7.4 Inductance Ratio (K), Tank Components and Dead Time

With the known value of the normalized switching frequency, the values of resonant inductance and resonant capacitances can be calculated as

$$L_r = \frac{FZ_b}{2\pi F_s} \text{ and } C_r = \frac{F}{2\pi Z_b F_s} \tag{2.35}$$

From the soft-switching analysis, it can be observed that the magnetizing inductance can enhance the ZVS region at the secondary side. Using (2.23) - (2.27), the relationship between the dead time, control parameters ϕ, and converter gain for the ZVS operating region is plotted and shown in Fig. 2.10 (a) for the primary side. The upper limits of the plot can be obtained from the respective switch current using (2.23). With a safe operating limit, the dead time for the primary bridge switches is 290 ns. Similarly, for the secondary side, the variation of the dead time with magnetizing inductance can be observed for the ZVS region in Fig. 2.10 (b). From Fig. 2.10 (b), it can be observed that as the value of the magnetizing inductance increases, the secondary switches move toward the non-ZVS region. So, to operate all the switches with ZVS, the magnetizing inductance is selected to be 292 μH for a dead time of value 235 ns. The value of the inductance ratio K can be given as

$$K = \frac{L_r}{L_m} = 0.2078 \tag{2.36}$$

2.7.5 Voltage Stress

The peak voltage stress across the primary and secondary bridge switches under steady-state and different loading conditions can be given as

$$(V_{S1})_{peak} = (V_{S2})_{peak} = V_{in} \tag{2.37}$$

$$(V_{S3})_{peak} = (V_{S4})_{peak} = V_o \tag{2.38}$$

2.7.6 Design of the Film Capacitors

The current flowing into the film capacitor C_1 can be given as

$$i_{C_1} = I_{in} - i_r(t)$$

Assuming the input current (I_{in}) is ripple-free, and the average film capacitor current is zero. The capacitor voltage ripple through the film capacitors (C_1 and C_2) can be calculated as,

$$\Delta V_{C_1} = \Delta V_{C_2} \approx \frac{1}{C_1} \int_{\phi T_s/2\pi}^{T_s/2} (I_{in} - i_r(t))dt$$

$$C_1 = C_2 = \frac{1}{\omega_s \Delta V_{C_1}} \left[I_{in}(\pi - \phi) - i_{rp}\left(\cos\alpha + \cos(\phi - \alpha)\right) \right] \tag{2.39}$$

The input film capacitors are responsible for generating a square voltage across the primary bridge and they also participate in the resonance phenomenon with the resonant tank. An

improper design of the film capacitor may lead to ripples in primary bridge voltage and resonant current, and ripple in input current leading to a loss in power harnessed. So, to avoid these issues, film capacitors (C_1 and C_2) must be equal and larger than the series resonance capacitance C_r to avoid resonating interference for high-frequency ripples. For this, the film capacitors C_1 and C_2 are designed using (2.40).

$$C_1 = C_2 \approx 100 \cdot C_r \tag{2.40}$$

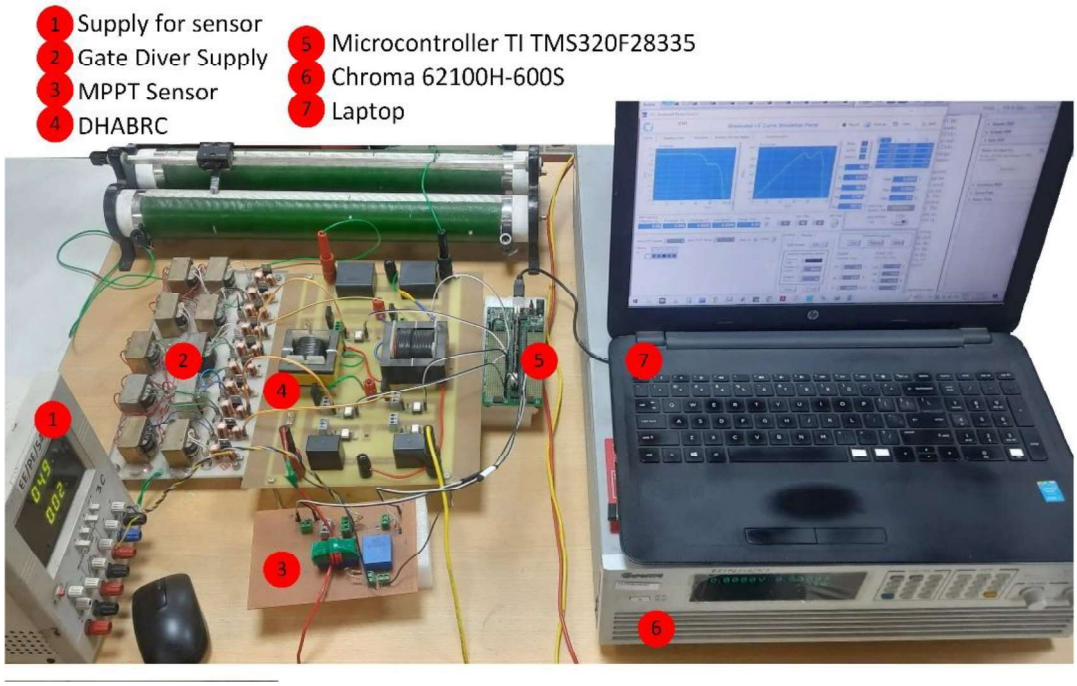


Fig. 2.11 The photograph of the experimental setup.

To design the input film capacitor value (2.39) and (2.40) must be satisfied. For the proposed converter, values of the C_1 and C_2 are chosen to be approximately 20 μF. Similarly, for the secondary side assuming that output current I_o is ripple-free, the current through the output film capacitor when the switch S_3 is turned off will be equal to the output current for a duration of half the switching cycle. The capacitor voltage ripple through the film capacitors C_3 and C_4 can be calculated as,

$$\Delta V_{C_3} = \Delta V_{C_4} \approx \frac{1}{C_3}\int_0^{T_s/2} I_o dt$$

$$C_3 = C_4 = \frac{I_o}{2\omega_s \Delta V_{C_3}} \tag{2.41}$$

From (2.41), the C_3 and C_4 are chosen to be approximately 20 μF. The design parameters of the DHABRC are given in Table 2.1 and the experimental photograph is shown in Fig. 2.11.

Table 2.1 Design parameters of DHABRC

Parameters	Value
Input Voltage (V_{in})	140 V
Output Voltage (V_o)	125-115
Output Power (P_o)	500 W
Switching Frequency (F_s)	50 kHz
Resonant Inductor (L_r)	60.68 μH
Parallel Inductor (L_m)	292 μH
Resonant Capacitor (C_r)	240.43 nF
Turns Ratio (n_t)	28:25
Film Capacitance (C_1 - C_4)	20 μF
Gate Driver IC	FOD 3184

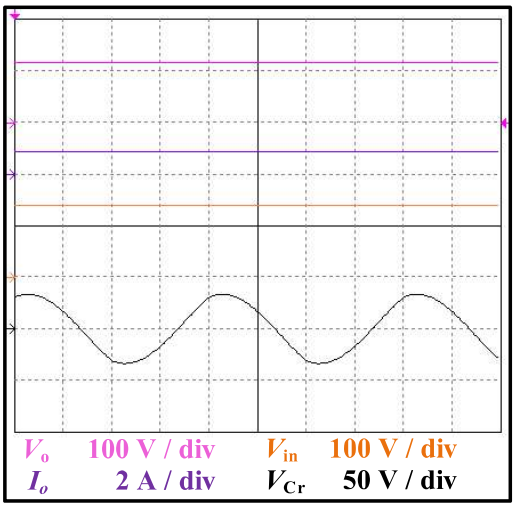
2.8 Results for DHABRC

The proposed DHABRC is tested using simulation software and experimental setup. The different results as follows.

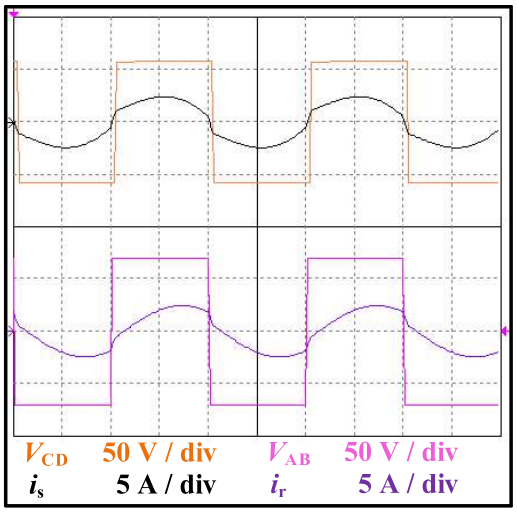
2.8.1 Simulation Results

The proposed converter is tested in steady-state conditions using simulation software PSIM 9.1 and results are shown in Fig. 2.12. To operate primary bridge switches (S_1 and S_2), with ZVS, the working current (i_r) must lag behind the primary bridge voltage V_{AB}. For secondary bridge switches (S_3 and S_4), the working current (i_s) must lead ahead of the secondary bridge voltage V_{CD}. It must be noted that the secondary current (i_s) flows opposite to the direction of the switch (S_3 and S_4) currents, so at the secondary side i_s must lead the V_{CD}.

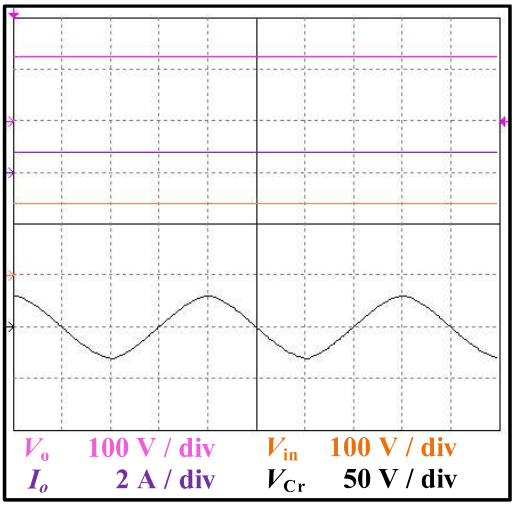
In Fig. 2.12 (a)-(b) and Fig. 2.12 (c)-(d), the steady-state simulation results for 20% load (100 W) at 115 V and 125 V output are shown. Similarly, the steady-state results for 100% (500 W) load at 115 V and 125 V output are shown in Fig. 2.12 (e)-(f) and Fig. 2.12 (g)-(h), respectively. It can be observed from the results that the analysis given for the proposed converter works fairly, and all the switches operate with ZVS for all the loading conditions.


V_o 100 V / div
V_{in} 100 V / div
I_o 2 A / div
V_{Cr} 50 V / div

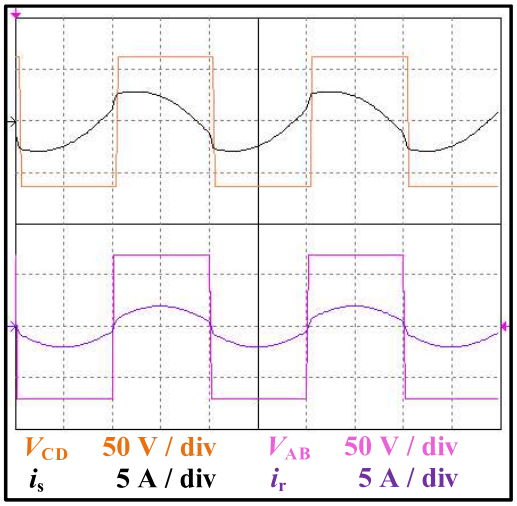
(a)


V_{CD} 50 V / div
V_{AB} 50 V / div
i_s 5 A / div
i_r 5 A / div

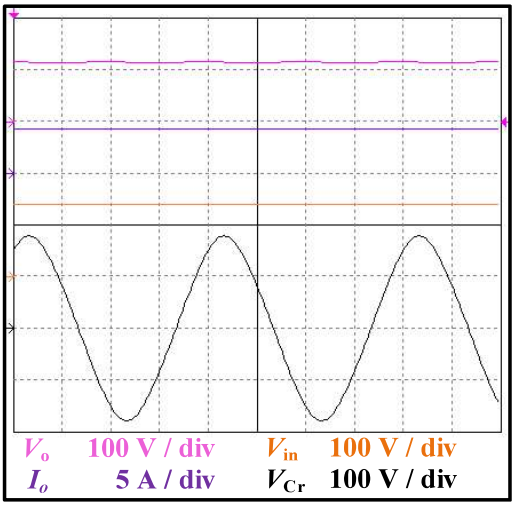
(b)


V_o 100 V / div
V_{in} 100 V / div
I_o 2 A / div
V_{Cr} 50 V / div

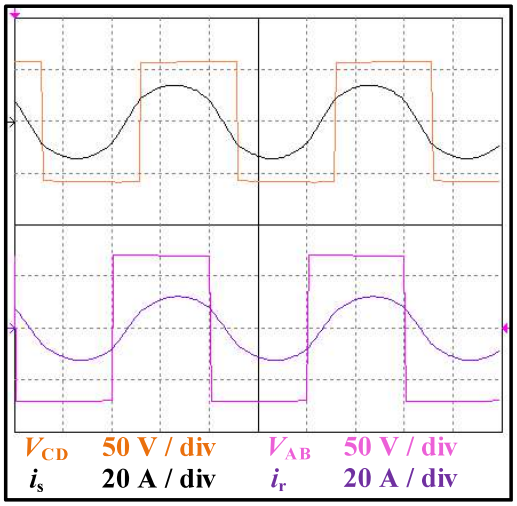
(c)


V_{CD} 50 V / div
V_{AB} 50 V / div
i_s 5 A / div
i_r 5 A / div

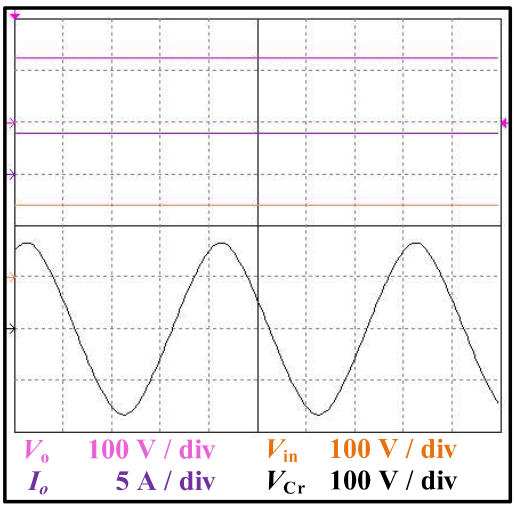
(d)


V_o 100 V / div
V_{in} 100 V / div
I_o 5 A / div
V_{Cr} 100 V / div

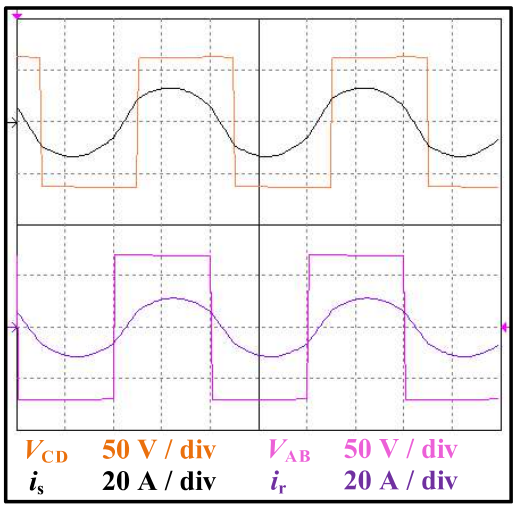
(e)


V_{CD} 50 V / div
V_{AB} 50 V / div
i_s 20 A / div
i_r 20 A / div

(f)



(g)

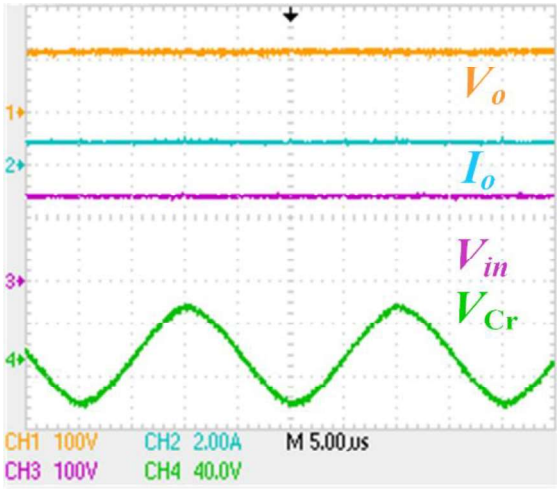


(h)

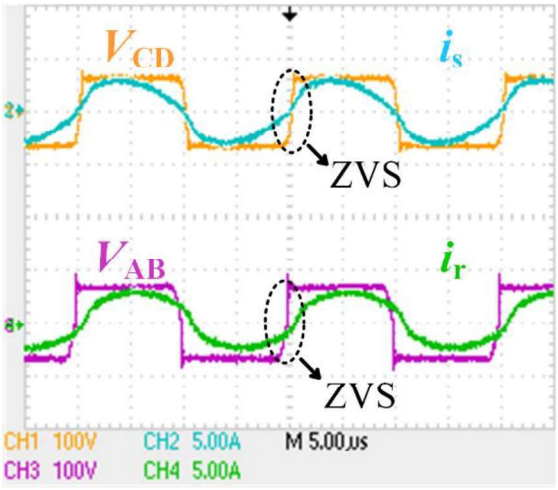
Fig. 2.12 Steady-state simulation results of DHABRC showing output voltage V_o and output current I_o, input Voltage V_{in}, capacitor voltage V_{Cr} and bridge voltages V_{AB} and V_{CD} and their corresponding bridge currents i_r and i_s for 20% load at (a) - (b) 115 V output and (c) - (d) 125 V output, 100% load at (e) - (f) 115 V output and (g) - (h) 125 V output.

2.8.2 Experimental Results

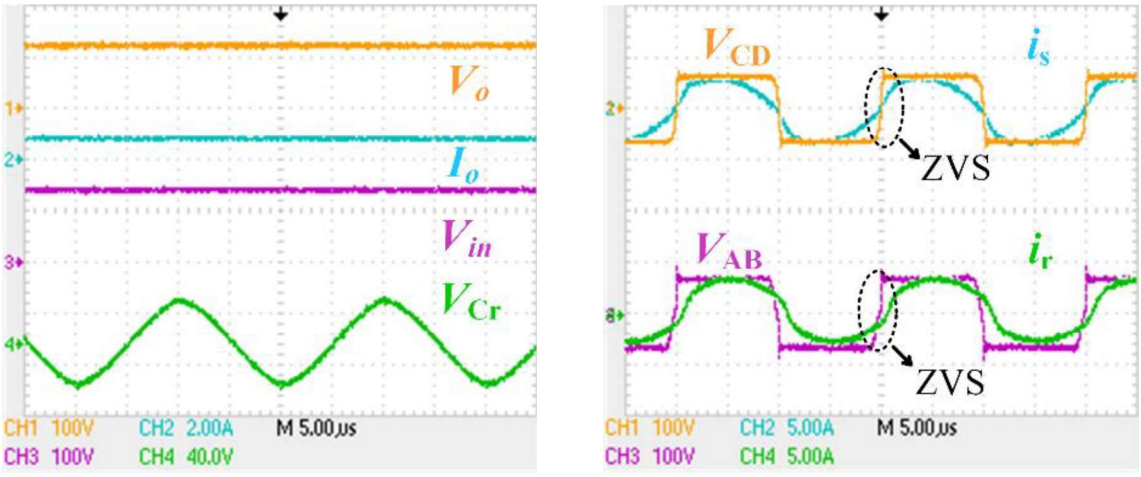
The steady-state experimental results of the DHABRC are shown in Fig 2.13. In Fig. 2.13 (a)-(b) and Fig. 2.13 (c)-(d) the steady-state results for 20% load at 115 V and 125 V output are shown. Similarly, the steady-state results for 100% load at 115 V and 125 V output are shown in Fig. 2.13 (e)-(f) and Fig. 2.13 (g)-(h) respectively. It can be observed from the experimental results that all the switches operate with ZVS for all the loading conditions.



(a)

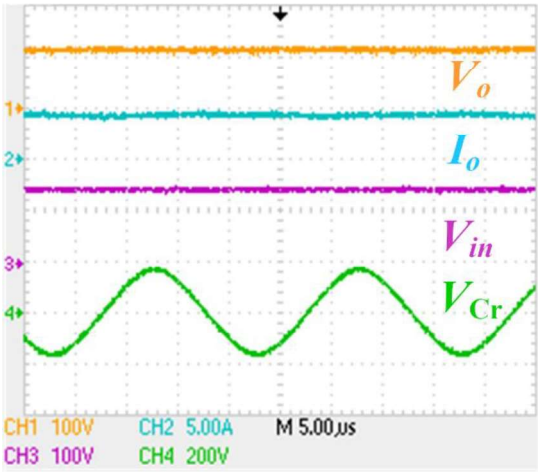


(b)

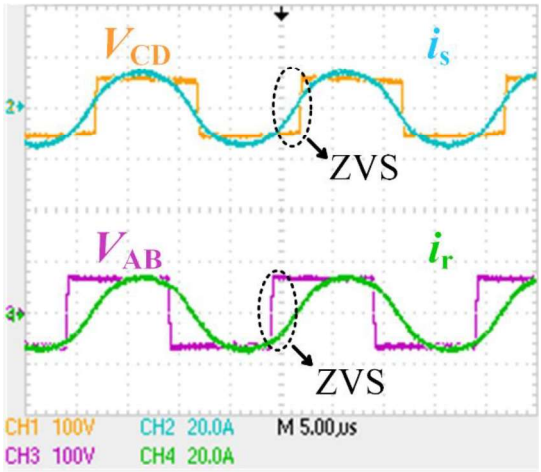


(c)

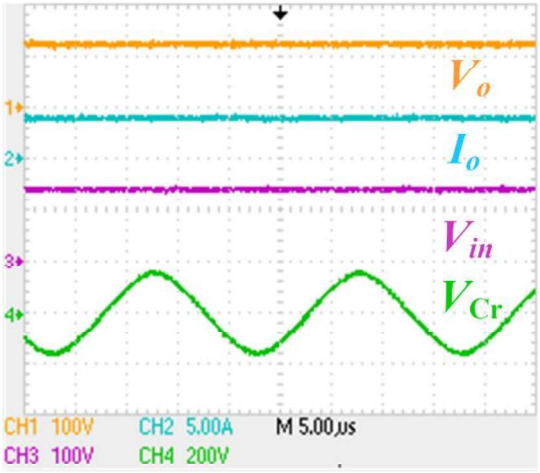
(d)



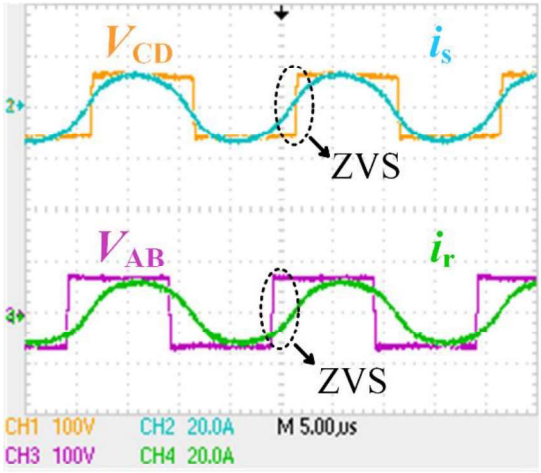
(e)



(f)



(g)



(h)

Fig. 2.13 Steady-state experimental results of DHABRC showing output voltage V_o and output current I_o, input Voltage V_{in}, capacitor voltage V_{Cr} and bridge voltages V_{AB} and V_{CD} and their corresponding bridge currents i_r and i_s for 20% load at (a) - (b) 115 V output and (c) - (d) 125 V output, 100% load at (e) - (f) 115 V output and (g) - (h) 125 V output.

2.8.3 Verification of the Efficacy of Analysis

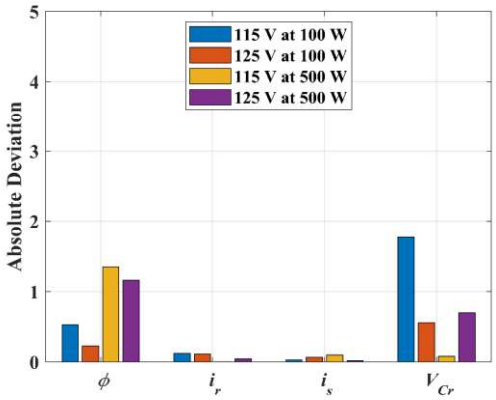
A comparison table (Table 2.2) is given to compare the value of the key parameters for 20% load and 100% load. The table shows that the theoretical results obtained from the modified FHA analysis are very similar (with some small variation due to the dead-band effect) to the simulation and experimental results. In Fig. 2.14 (a)-(b), the absolute deviation of the experimental results is shown using bar graphs with respect to key analytical equations and simulation results.

Table 2.2 Comparison table for the key parameters at steady-state condition

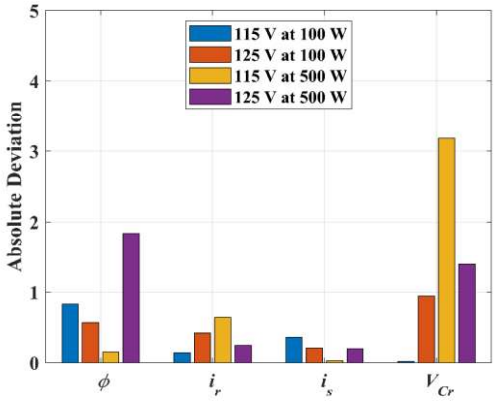
Parameter	**115 V at 100 Watt**			**125 V at 100 Watt**		
	Theo.	**Sim.**	**Exp.**	**Theo.**	**Sim.**	**Exp.**
ϕ	9.17	9.7	10	8.43	8.2	9
i_r	1.87	1.75	2.01	1.59	1.48	2.01
i_s	1.94	1.91	2.3	1.99	1.92	2.2
V_{Cr}	24.78	23	24.8	21.06	20.5	22
Parameter	**115 V at 500 Watt**			**125 V at 500 Watt**		
	Theo.	**Sim.**	**Exp.**	**Theo.**	**Sim.**	**Exp.**
ϕ	52.85	51.5	53	47.16	46	49
i_r	9.277	9.274	9.92	8.656	8.7	8.9
i_s	10.78	10.68	10.75	10.16	10	9.82
V_{Cr}	122.82	122.9	126	114.6	115.3	116

2.8.4 Verification of using Film Capacitor

Film capacitors outperform electrolytic capacitors in many areas, like reliability, life span, size, and power density. To prove the feasibility of using film capacitors further, a measurement of voltage across the film capacitors is taken under various conditions like startup transient, load dynamics, and steady-state conditions as shown in Fig. 2.15 (a)-(b). In Fig. 2.15 (c), the experimental results for the voltage holding capability of the film capacitors (C_3 and C_4) are shown for a constant voltage operation under a 50% change in load. It can be seen from Fig. 2.15 (c) that voltage across the capacitor remains constant for the change in the load current.

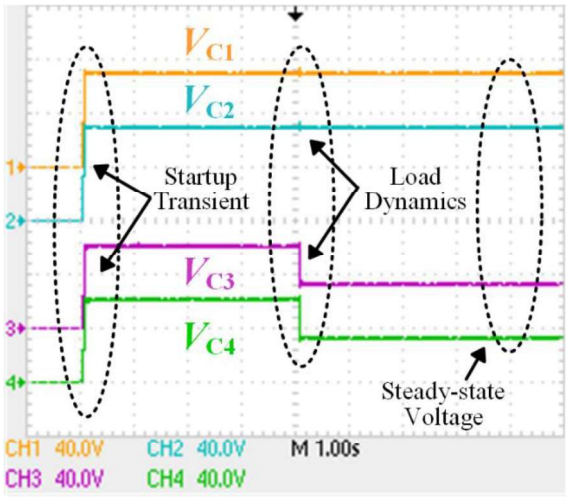


(a)

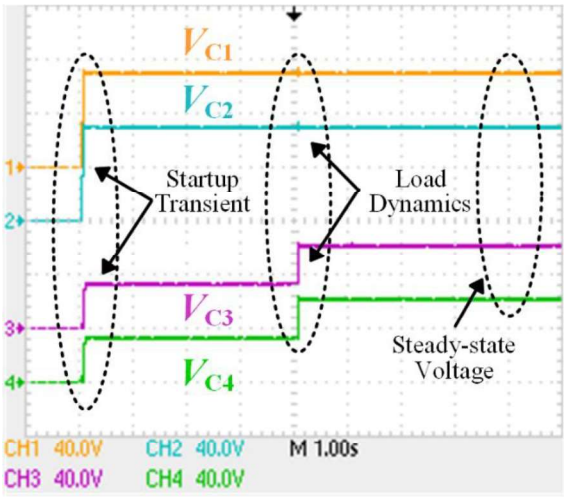


(b)

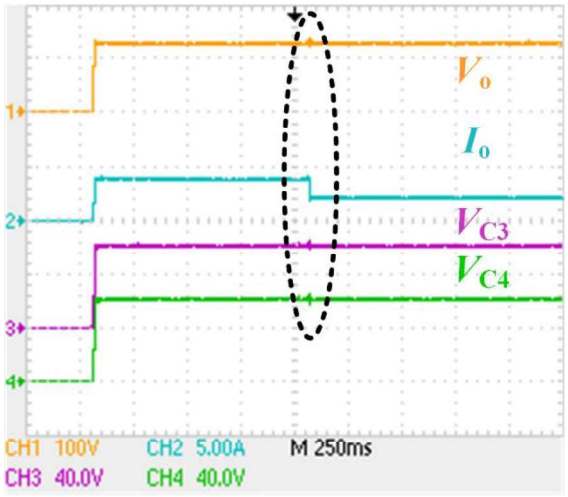
Fig. 2.14 Absolute variations of theoretical data from (a) Simulation results and (b) Experimental results.



(a)



(b)



(c)

Fig. 2.15 Measurement of film capacitor voltages V_{C1}–V_{C4} under startup transient, load dynamics, and steady-state conditions for (a) step increase in load (50%) and (b) step decrease in load (50%). (c) Voltage waveform of output voltage and film capacitors (V_{C3} and V_{C4}) for a load decrease of 50% under constant voltage operation.

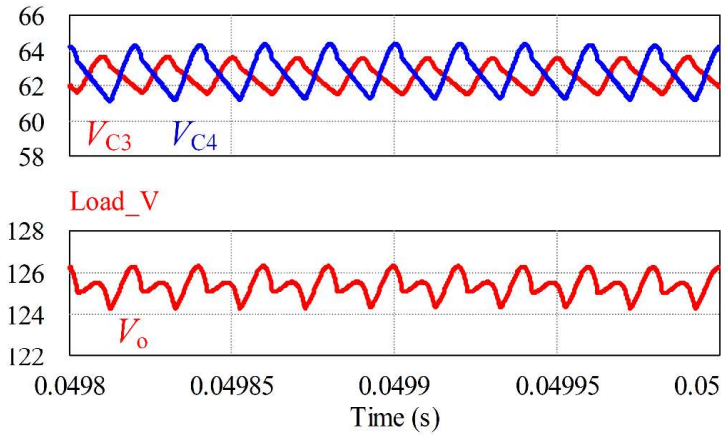


Fig. 2.16 Measurement of film capacitor voltages V_{C3}–V_{C4} and output voltage V_o for 125 V under 20% capacitance variation of C_3–C_4 due to tolerance.

From Fig. 2.15, it can be seen that the film capacitor voltages are steady and oscillation-free in all the above-mentioned tests and conditions. To verify the tolerance effect of the FCs on the converter output voltage V_o, a simulation result using PSIM 9.1 is shown in Fig. 2.16. For this, the capacitance C_3 is increased by 20% of its designed value, and the capacitance C_4 is decreased by 20% of its designed value. It can be seen that the output voltage V_o is not much affected by such variation in capacitance. For the DHABRC, FCs having a tolerance limit of

5% are used. The different tests and experimental results justify that the FCs are feasible to use for the DHABRC. While designing the isolated resonant converter, voltage balancing across the capacitors must be taken care of. So, to the best of effort, all the capacitors of the same value are selected to avoid any mismatch in the voltage and, therefore, maloperation of the proposed converter.

Table 2.3 Design parameters of ADABRC

Parameters	Value
Input Voltage (V_{in})	60 V
Output Voltage (V_o)	108-120 V
Output Power (P_o)	500 W
Switching Frequency (F_s)	50 kHz
Resonant Inductor (L_r)	44.6 μH
Parallel Inductor (L_m)	122.6 μH
Resonant Capacitor (C_r)	227.25 nF
Turns Ratio (n_t)	1:1
Film Capacitance (C_1 - C_3)	20 μF
Gate Driver IC	FOD 3184

2.9 Results for ADABRC

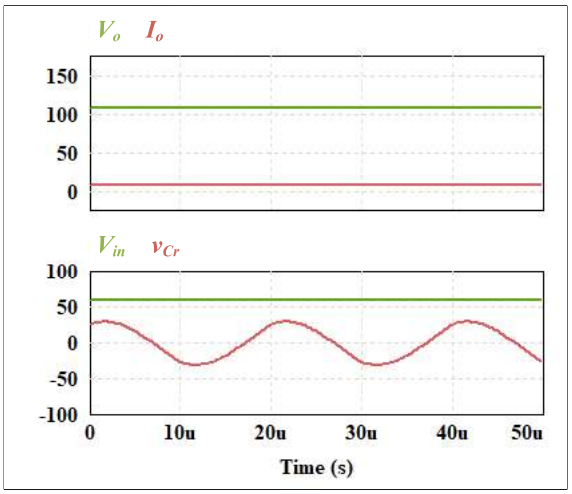
The design parameters of the ADABRC are given in Table 2.3. The proposed DHABRC is tested using simulation software and experimental setup. The different results are as follows.

2.9.1 Simulation Results

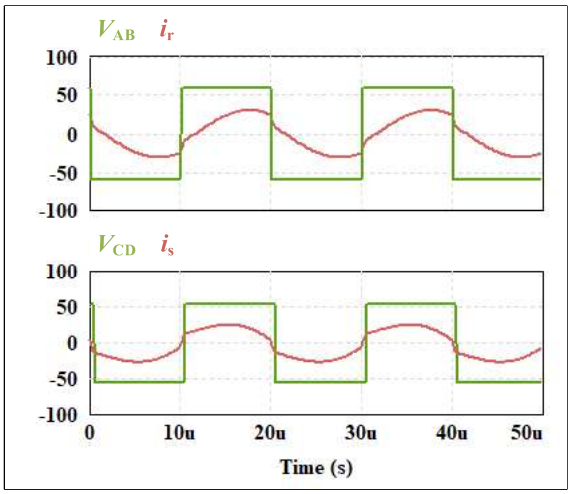
The proposed converter ADABRC is tested in steady-state conditions using simulation software PSIM 9.1, and results are shown in Fig. 2.17. To operate primary bridge switches with ZVS, the working current (i_r) must lag behind the primary bridge voltage V_{AB}. For secondary bridge switches (S_3 and S_4), the working current (i_s) must lead ahead of the secondary bridge voltage V_{CD}. It must be noted that the secondary current (i_s) flows opposite to the direction of the switch (S_3 and S_4) currents, so at the secondary side i_s must lead the V_{CD}.

In Fig. 2.17 (a)-(b) and Fig. 2.17 (c)-(d), the steady-state simulation results for 20% load (100 W) at 108 V and 120 V output are shown. Similarly, the steady-state results for 100% (500 W) load at 108 V and 120 V output are shown in Fig. 2.17 (e)-(f) and Fig. 2.17 (g)-(h)

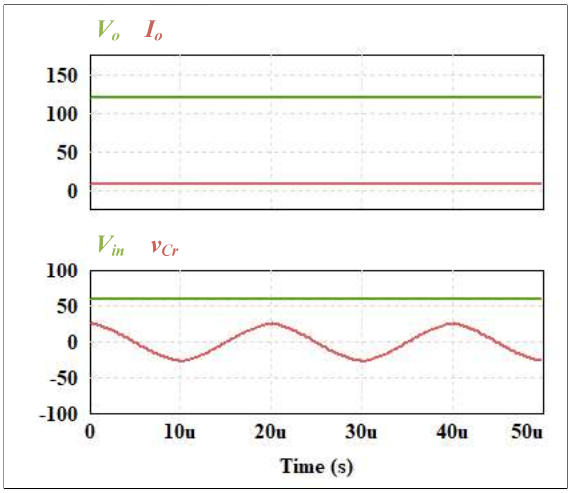
respectively. It can be observed from the results that the analysis given for the proposed converter works fairly, and all the switches operate with ZVS for all the loading conditions.



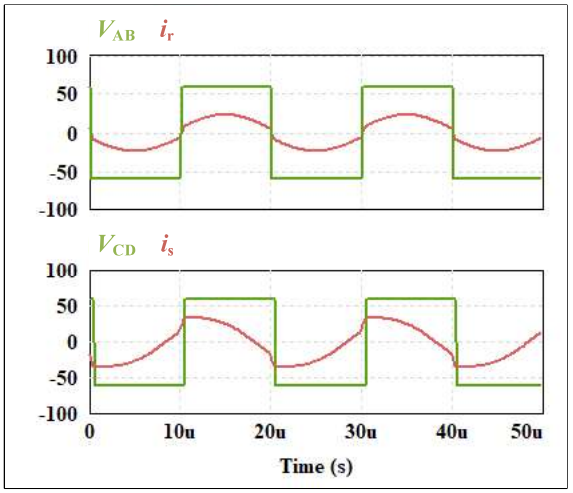
(a)



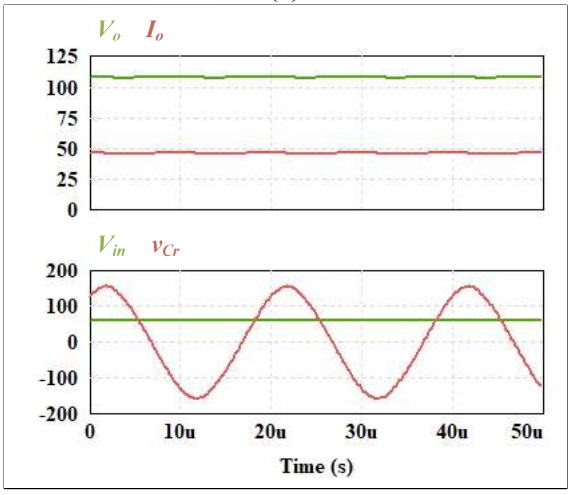
(b)



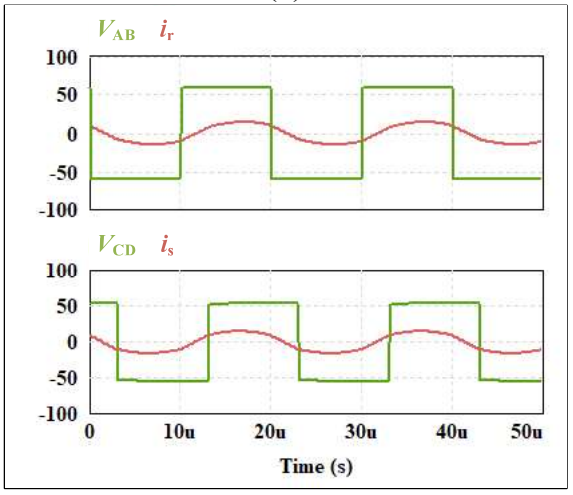
(c)



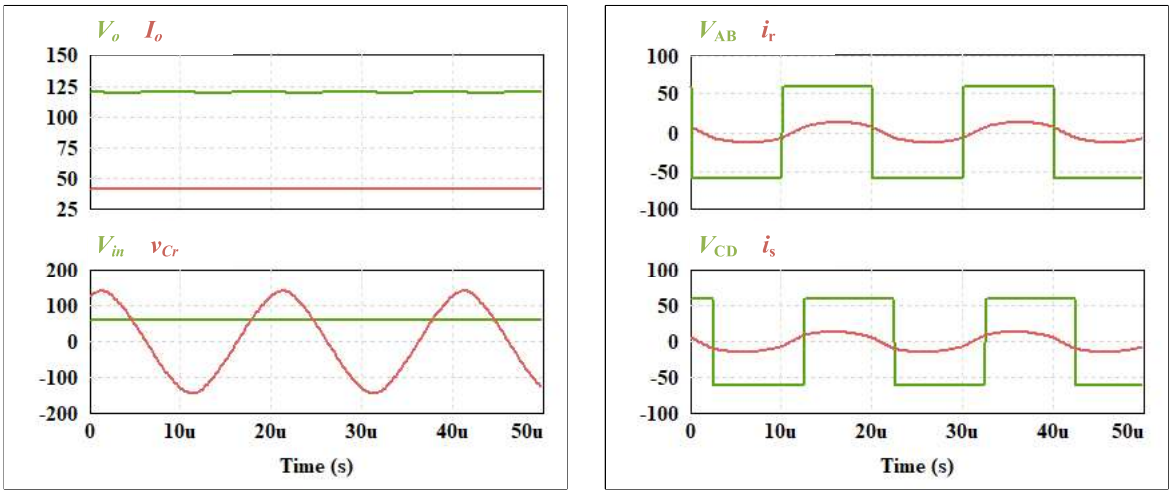
(d)



(e)

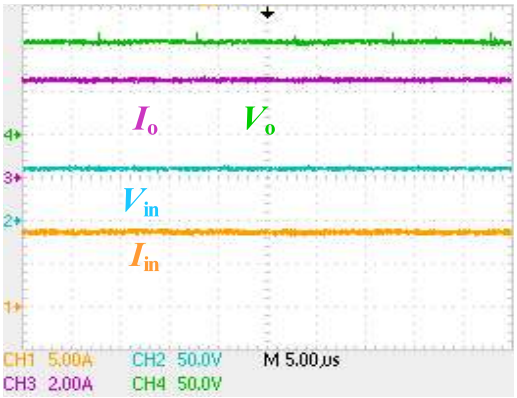


(f)

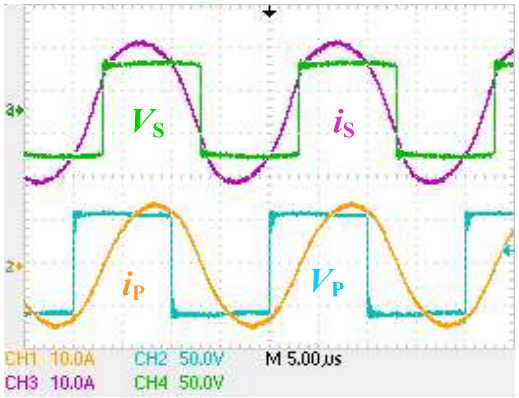


(g) (h)

Fig. 2.17 Steady-state simulation results of ADABRC showing output voltage V_o and output current I_o, input Voltage V_{in}, capacitor voltage V_{Cr} and bridge voltages V_{AB} and V_{CD} and their corresponding bridge currents i_r and i_s for 20% load at (a) - (b) 108 V output and (c) - (d) 120 V output, 100% load at (e) - (f) 108 V output and (g) - (h) 120 V output.



(a)



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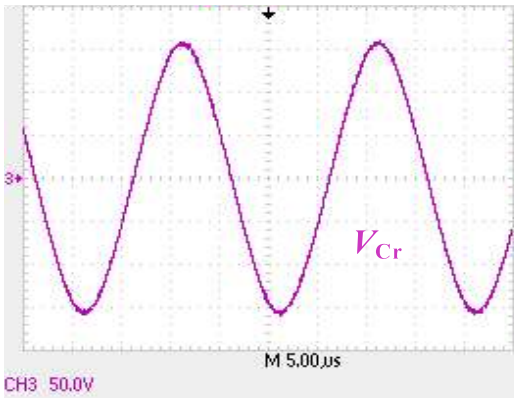
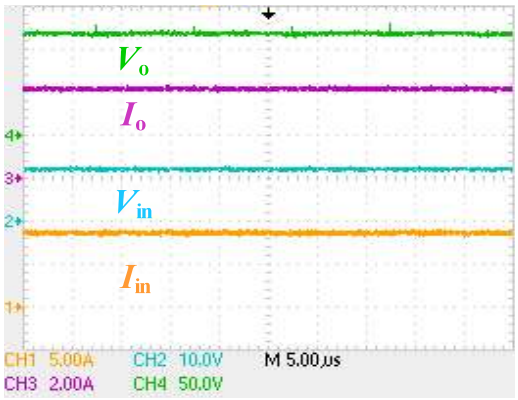
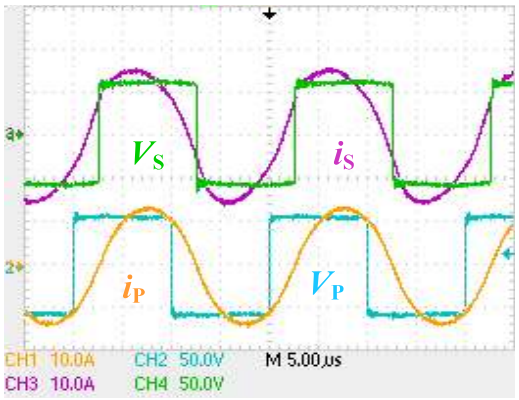


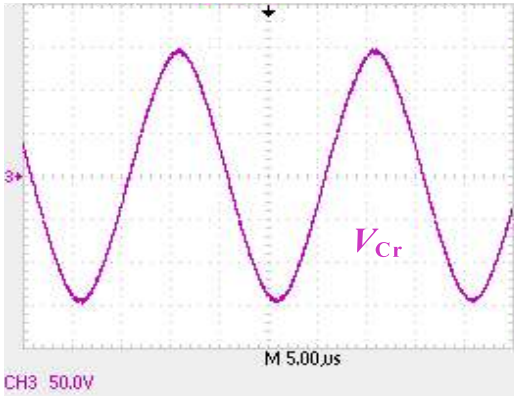
(c)



(d)



(e)



(f)

Fig. 2.18 Steady-state experimental results of ADABRC showing output voltage V_o and output current I_o, input Voltage V_{in} input current I_{in}, bridge voltages V_{AB} and V_{CD} and their corresponding bridge currents ir and is and capacitor voltage V_{Cr} for 500 W load at (a) - (c) 108 V output and (d) - (f) 120 V output.

2.9.2 Experimental Results

The steady-state experimental results of the ADABRC are shown in Fig 2.18. Fig 2.18 (a) shows the output voltage V_o, output current I_o, input voltage V_{in}, and input current I_{in} for 500 W and 120 V output. The bridge voltages (V_{AB} and V_{CD}) and their corresponding currents (i_r and i_s) have been given in Fig 2.18 (b). The resonant capacitor voltage V_{Cr} has been shown in Fig 2.18 (c). Fig 2.18 (d) shows the output voltage V_o, output current I_o, input voltage V_{in}, and input current I_{in} for 500 W and 108 V output in forward mode. The bridge voltages (V_{AB} and V_{CD}) and their corresponding currents (i_r and i_s) have been given in Fig 2.18 (e). The resonant capacitor voltage V_{Cr} for this case has been shown in Fig 2.18 (f). It can be observed from the experimental results that all the switches operate with ZVS.

2.10 Efficiency Analysis

The efficiency curve for the DHABRC is shown in Fig. 2.19. In Fig. 2.20, the loss breakdown for a 500 W proposed converter is presented for 125 V and 115 V voltage levels. The primary sources of the losses are the conduction losses of the active switches and copper loss of the resonant inductor and high-frequency transformer. Other losses are due to gate drivers and auxiliary supplies. The efficiency of the resonant converter can be further improved by optimizing the components and reducing the parasitic values. The peak efficiency for the DHABRC is approximately 96.4% for 125 V output and 95.9% for 115 V output.

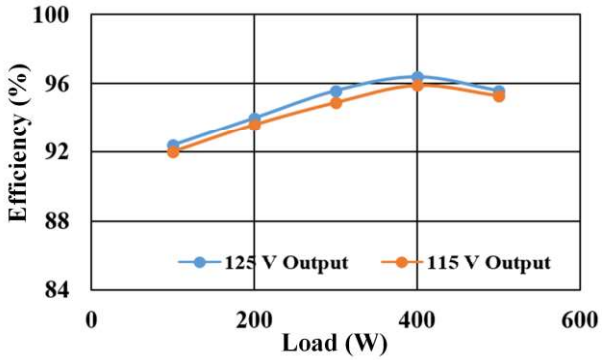


Fig. 2.19 Efficiency curve for the DHABRC.

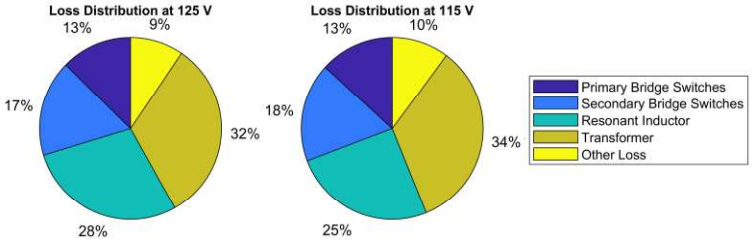


Fig. 2.20 The loss distribution map for the proposed converter.

2.11 Comparison with the Similar Topologies

To demonstrate the advantages and features of the DHABRC, a table (Table 2.4) is presented where it is compared with the existing topologies. The proposed converter outperforms the existing converters on the basis of component utilisation, component optimization using sufficient condition for soft-switching, dead-time optimization, etc. For solar PV applications, the input current should be ripple-free and hence the input capacitors are required to carry high ripple current with low ESR. For film capacitors, besides having very low of ESR (equivalent series resistance), its ripple current carrying capacity per unit capacitance is many times higher

than of the electrolytic capacitor, making it more suitable for solar PV applications. Similarly, at the output, the use of film capacitors reduces losses and hence more efficient power converter than the converter based on electrolytic capacitor.

Table 2.4 Comparison of proposed DHABRC with existing topologies

Parameters	[115]	[116]	[117]	[118]	[119]	[82]	[120]	Proposed
Active switches	4	6	4	4	2	2	8	4
Diodes	2	2	4	0	2	2	0	0
Resonance	Yes	Yes	Yes	Yes	Yes	Partial	Yes	Yes
Filter capacitor	EC+FC	EC	EC	EC	EC	EC+FC	EC	FC
Soft-switching	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
Sufficient Condition for Soft-switching	No	No	No	No	No	No	No	Yes
Dead-Time Optimization	No	No	No	No	No	No	No	Yes
Component Value Optimization	No	No	No	No	No	No	No	Yes

2.12 Conclusion

This chapter presents the design and operation of two electrolytic capacitor-less isolated DC-DC resonant converters, i.e., DHABRC and ADABRC. The soft-switching conditions of the proposed converters are derived using the fundamental harmonics approximation. Based on the mathematical analysis presented, the resonant tank components are optimized. Later in the chapter, the necessary conditions for the soft-switching are also derived, and its effect on the dead band time and mutual inductance is observed. A 500 W scaled-down laboratory prototype of the proposed converter is developed to verify the proposed concept. For DHABRC, the efficacy of the mathematical modeling and soft-switching operation is verified, and the theoretically formulated data is compared with the simulation and experimental results in steady-state conditions. The film capacitor's feasibility is also verified by observing the voltage across them during the startup transient, load dynamics, and steady-state voltage.

Now, to exemplify the application of the proposed converter, it is integrated with solar PV in Chapter 3. In solar PV integration, the traditional maximum power point tracking algorithms fail to harness the maximum power from solar PV under partial shading or non-uniform irradiance conditions. So, optimization-based maximum power point tracking algorithms like particle swarm optimization and grey wolf optimization are utilized and the challenges associated with the partial shading conditions are addressed.