Chapter 5

SPE GaSb/Si VTFET Versus SPE Ge/Si VTFET: Performance Comparison at Device and Circuit Levels

5.1 Introduction

It is discussed in Chapter-1 that the use of source/channel heterojunction based TFETs formed by using a narrow band gap material such as Ge, InAs, InSb, InGaAs in the source region and Si for both the channel and drain regions of the device can improve the performance over the conventional all-Si TFETs [80], [111], [113], [129]. In Chapter-2, we have combined the source pocket engineering with the heterojunction engineering to demonstrate the superior performance parameters of the source pocket engineered (SPE) GaSb/Si heterojunction (HJ) VTFETs over the all-Si based VTFETs. The application of the proposed SPE GaSb/Si HJ VTFETs in the 8T SRAM circuit has been discussed in Chapter-4. It may be mentioned that Ge is more widely used as the source material than III-V materials in the TFET due to their better lattice matching with Si. In view of the above, the present chapter is devoted to compare the device and circuit level performance analysis of the SPE GaSb/Si HJ VTFET with that of the SPE Ge/Si HJ VTFET. Various device-level performance parameters such as the drive current (ON-current), OFF-state current, SS, I_{ON}/I_{OFF} ratio, transconductance (g_m), intrinsic gate to drain capacitance (C_{gd}), intrinsic gate to source capacitance (C_{gs}), cut-off frequency (f_T), and transconductance generation factor (TGF) of the two devices have been compared. On the other hand, the two devices have been explored for designing the inverter and 8T SRAM cell to investigate the circuit level performances of

the two devices. The device level studies have been performed by using the commercially available SILVACO ATLAS^{TM} TCAD simulation tool [123] whereas the circuit-level performance has been studied by using the Cadence Virtuoso tool by exporting the I-V and C-V data from the device simulation tool. The layout of the present chapter can be given as follows.

In Section 5.2, we have shown simulation methodology for device and circuit-level simulations in the similar manner as considered in the previous chapters. Section 5.3 includes some important results and discussions related to the device and circuit-level performance parameters of both the source pocket engineered heterojunction vertical TFETs under study. Finally, Sec. 5.4 describes the conclusion of the present chapter.

5.2 Device and Circuit Level Simulation Methodology with Device Design Parameters

Fig 5.1(a) shows source pocket engineered Ge/Si heterojunction vertical TFET (SPE Ge/Si HJ VTFET) and Fig 5.1(b) shows source pocket engineered GaSb/Si heterojunction vertical TFET (SPE GaSb/Si HJ VTFET) presented for the device and circuit-level simulation in this study.The cross-sectional view of the presented VTFETs are depicted in Fig. 5.1(c), and (d) respectively. The models used to analyse the device level performance for the presented VTFETs are considered the same as discussed in Chapter-2 and Chapter-3. Uniform doping concentrations in various regions of the device is assumed. To include the effects of the traps created at the interface of the Si/Ge or Si/GaSb heterojunction (due to lattice mismatching of the two materials) on the device performance, the non-local trap models TAT.NLDEPTH and TAT.RELEI have been used in the TCAD simulation tool as discussed in Sec 2.2. Here the trap energy

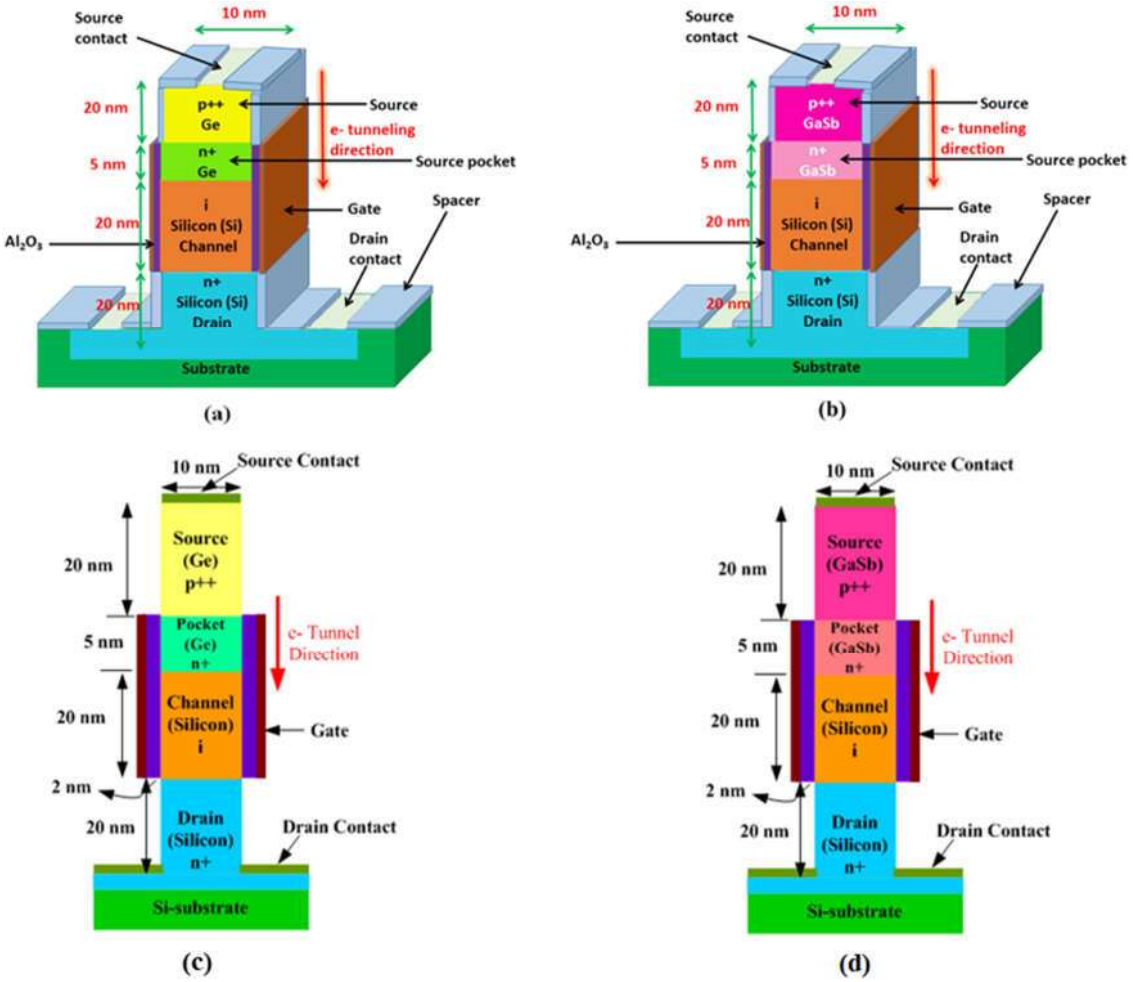

Fig. 5.1: Schematic representation of (a) SPE Ge/Si HJ VTFET, and (b) SPE GaSb/Si HJ VTFET respectively; cross-sectional view of (c) SPE Ge/Si HJ VTFET, and (d) SPE GaSb/Si HJ VTFET respectively.

levels in Gasb and Ge are assumed 0.16 eV and 0.15 eV above the valence bands of the source materials, respectively. The trap energy levels are assumed close to the valence band to consider the adverse effects of the traps on the tunnelling of electrons from the valence band of source to conduction band of the channel region in the TFETs. A bulk trap of density of 1×10^{18} cm^{-3} is assumed for the SPE GaSb/Si HJ VTFET whereas 5×10^{17} cm^{-3} has been considered for the SPE Ge/Si HJ VTFET under study. Optimized device design parameters along with optimized doping concentrations of

TABLE 5.1

DEVICE DESIGN PARAMETERS OF THE SPE GaSb/Si HJ VTFET AND SPE Ge/Si HJ VTFET

Parameters	**SPE GaSb/Si HJ VTFET**	**SPE Ge/Si HJ VTFET**
Source doping concentration (N_A)	2×10^{19} cm^{-3}	2×10^{19} cm^{-3}
Pocket doping concentration (N_D)	$7\times10^{18}cm^{-3}$	$7\times10^{18}cm^{-3}$
Channel doping concentration (N_A)	5×10^{16} cm^{-3}	5×10^{16} cm^{-3}
Drain doping concentration (N_D)	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
Thickness of channel (t_{Si})	10 nm	10 nm
Thickness of gate oxide (t_{ox})	2 nm	2 nm
Gate electrode work function (Φ_m)	4.2 eV	4.2 eV
Gate dielectric constant of Al_2O_3 (ε)	9.3	9.3
Gate length (L_G)	25 nm	25 nm
Source length (L_S)	20 nm	20 nm
Drain length (L_D)	20 nm	20 nm
Bandgap of Ge at room temperature	-	0.67 eV
Bandgap of GaSb at room temperature	0.7 eV	-
Bandgap of Silicon at room tempearture	1.12 eV	1.12 eV
Electron affinity of Ge	-	4.01 eV
Electron affinity of GaSb	4.05 eV	-
Electron affinity of Si	4.06 eV	4.06 eV
Lattice constant of Ge	-	5.65 ^{0}A
Lattice constant of GaSb	6.09 ^{0}A	-
Lattice constant of Si	5.43 ^{0}A	5.43 ^{0}A
Tunnel mass of hole in Ge (m_{htGe})	-	$0.084m_o$
Tunnel mass of electron in Ge (m_{etGe})	-	$0.092m_o$
Tunnel mass of hole in GaSb (m_{htGaSb})	$0.4m_o$	-
Tunnel mass of electron in GaSb (m_{etGaSb})	$0.0410m_o$	-
Tunnel mass of hole in silicon (m_{htSi})	$0.24m_o$	$0.24m_o$
Tunnel mass of electron in silicon (m_{etSi})	$0.20m_o$	$0.20m_o$
Pocket length	5 nm	5 nm
Trap energy above valence band for GaSb	0.16 eV	-
Trap energy above valence band for Ge	-	0.15 eV
Bulk trap density	1×10^{18} cm^{-3}	5×10^{17} cm^{-3}

different regions for the presented VTFETs are listed in Table-5.1. The tunnel mass for electrons and holes, electron affinity, band gap, lattice constant of silicon, germanium and GaSb are also listed in the Table-5.1. Consideration of both the VTFETs with homogeneous gate dielectric has been taken where the gate dielectric is adopted as Al_2O_3 with dielectric constant as 9.3 as discussed earlier in Chapter-2.

In order to test the feasibility of the presented VTFETs in circuit applications, two sets of lookup tables of current and capacitances are constructed using the data exported from SILVACO ATLAS^{TM} TCAD tool as discussed in Chapter-4. The look up tables are then implemented in CADENCE tool with the help of Verilog-A model [106] for implementing a basic digital logic inverter and 8T SRAM cell. The schematic of both the circuits are given in Fig. 5.2. The platform used for the device-circuit simulation remains the same as ilustrated in Chapter-4. The p-type vertical TFETs are assumed to have symmetric I_D-V_G characteristics corresponding to their n-channel counterparts

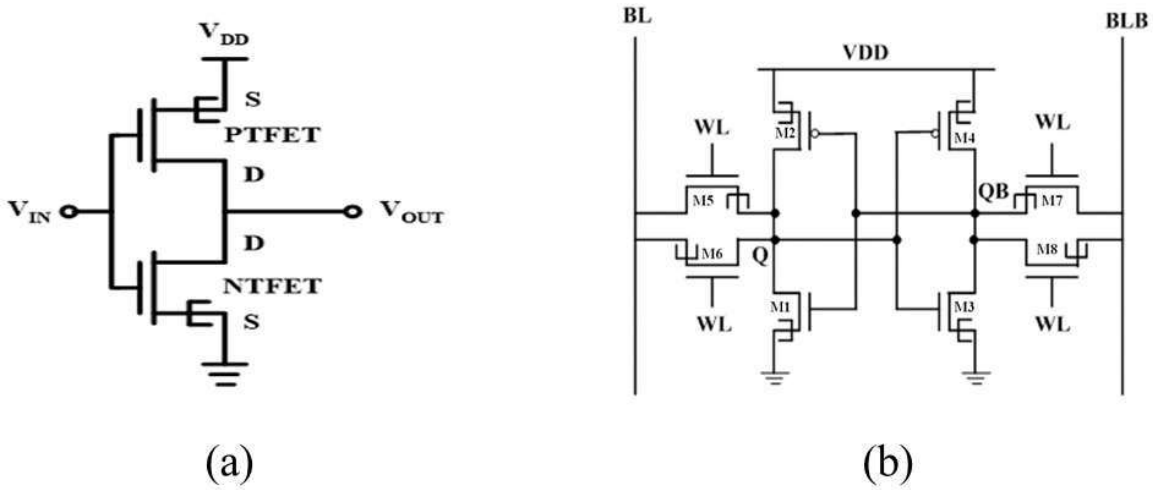

Fig. 5.2:(a) Schematic view of the inverter designed using presented VTFETs; (b) Schematic view of 8T SRAM designed with presented VTFETs.

[107]. The device level calibration for the used models in the model statement using SILVACO ATLAS^{TM} TCAD tool has been done in a similar way as discussed in Chapter-2 and circuit level calibration of the VTFETs is made in a similar manner as discussed in Chapter-4.

5.3 Results and Discussion

5.3.1 Device Level Performance Analysis

In the beginning of this section, device level performance parameters such as drain current, SS, I_{ON}/I_{OFF} ratio, transconductance (g_m), intrinsic gate to drain capacitance (C_{gd}), intrinsic gate to source capacitance (C_{gs}), cut-off frequency (f_T), and transconductance generation factor (TGF) for SPE GaSb/Si HJ VTFET, and SPE Ge/Si HJ VTFET have been analyzed whereas later in the section circuit level performance parameters such as static and time varying parameters of digital logic inverter and 8T SRAM cell have been analyzed.

To start the device level performance analysis, energy band (E-B) diagram is considered as the most important analysis to predict the behavior of the proposed TFET. Fig. 5.3(a) and (b) shows the E-B distribution of the presented tunnel FETs in OFF-state and ON-state respectively. When zero gate voltage is applied across gate to source terminal, the conduction band of the channel and the valence band of source are not properly aligned as shown in Fig. 5.3(a) and it is called OFF-state. Therefore, electrons cannot be transported through source-channel junction. However, with the application of positive gate voltage, a tunneling path is created due to the lowering of conduction band of the channel which makes suitable alignment between source of the valence band with the channel in conduction band. This in turn inhibits the tunneling phenomena where the

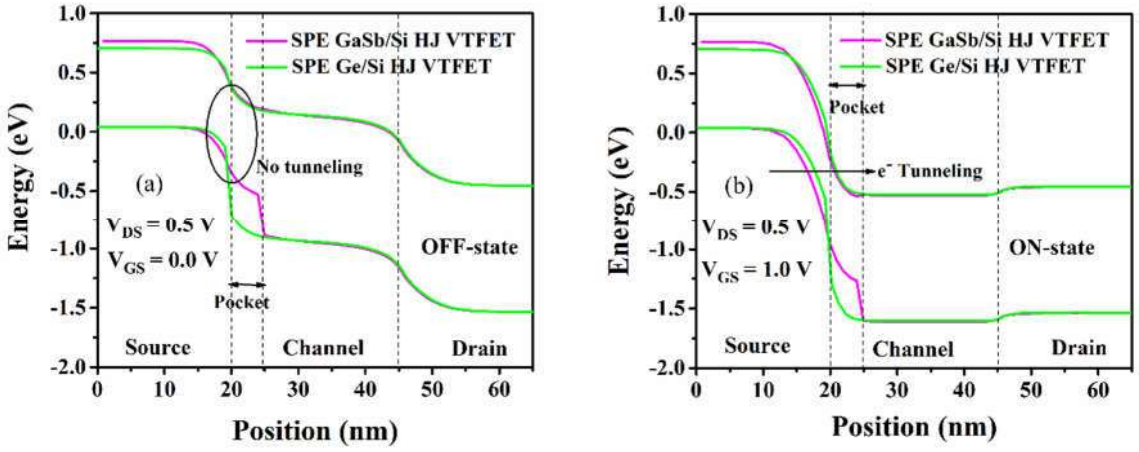

Fig. 5.3: (a) OFF-state energy band distribution of SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET, and (b) ON-state energy band distribution of SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET.

electrons can tunnel through the source-channel junction as shown in Fig. 5.3(b). This state is known as ON-state. Tunneling barrier width of the proposed SPE Ge/Si HJ VTFET is less than that of the SPE GaSb/Si HJ VTFET which leads to larger number of carrier tunneling in the SPE Ge/Si HJ VTFET. The reason for lower tunneling barrier for SPE Ge/Si VTFET over the SPE GaSb/Si VTFET is attributed to the smaller bandgap of Ge than GaSb at room temperature. This will lead to higher ON-current in SPE Ge/Si HJ VTFET than SPE GaSb/Si HJ VTFET which is discussed in the transfer characeristics analysis of both the VTFETs under study.

The transfer characteristics of the proposed SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET have been compared in Fig. 5.4(a) while transconductance (g_m) characteristics have been compared in Fig. 5.4(b). The transfer (I_D-V_G) characteristics is obtained for a drain voltage (V_{DS}) of 0.5 V while the gate to source voltage (V_{GS}) has been varied from 0 V to 1 V as shown in Fig.5.4(a). It has been shown in Fig. 5.4(a) that the ON-current is comparatively higher for SPE Ge/Si HJ VTFET than SPE GaSb/Si HJ

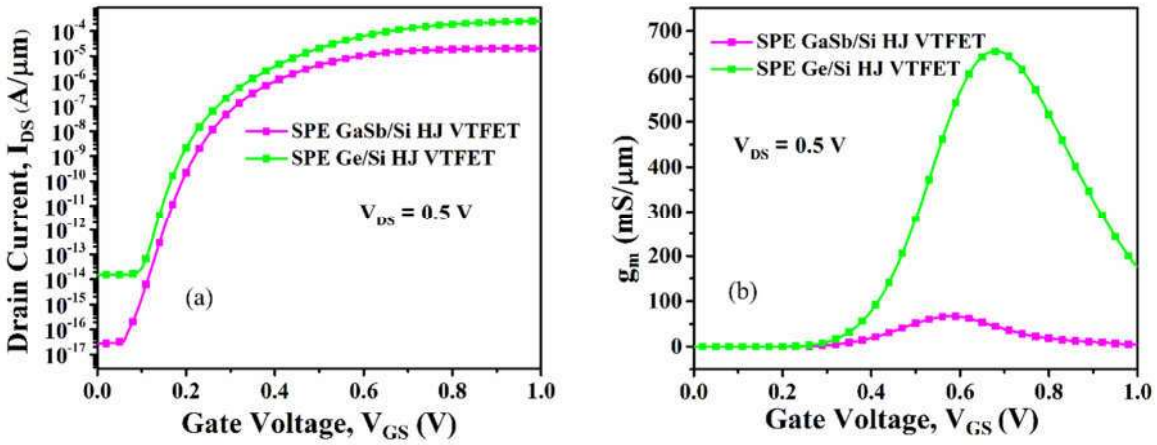

Fig. 5.4: Comparative plot of (a) Transfer characteristics, and (b) Transconductance (g_m) for SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET.

VTFET. The smaller room-temperature bandgap of Ge than GaSb leads to smaller tunneling barrier in the SPE Ge/Si VTFET than that in the SPE GaSb/Si VTFET. This causes more number of valence electrons to tunnel from the valence band of the Ge to the conduction band of Si in the channel region in the SPE Ge/Si VTFET than the tunnelling of electrons at the GaSb/Si junction in the SPE GaSb/Si VTFET counterpart. The increase in tunneling of carriers makes not only the ON-current higher but also the OFF-current higher in SPE Ge/Si VTFET than the OFF current in the GaSb/Si VTFET as observed in Fig. 5.4(a). This leads to lowering the I_{ON}/I_{OFF} ratio in the SPE Ge/Si HJ VTFET despite having higher ON-current. The I_{ON}/I_{OFF} ratios of 7.5×10^{11} and 1.616×10^{10} are obtained for SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET respectively. The parameters like I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, average SS and threshold voltage (V_T) of SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET are listed in Table-5.2. Clearly, for SPE Ge/Si HJ VTFET shows a better performance in terms of higher ON-current over the SPE GaSb/Si HJ VTFET. However, lower I_{OFF} in the SPE GaSb/Si HJ VTFET gives rise to improved I_{ON}/I_{OFF} ratio. The better I_{ON}/I_{OFF} ratio in SPE GaSb/Si

TABLE 5.2

DIFFERENT DC PARAMETERS OF THE VTFETS UNDER STUDY

Parameters	SPE GaSb/Si HJ VTFET	SPE Ge/Si HJ VTFET
I_{ON} (A/μm)	2.068 x10^{-5}	2.49× 10^{-4}
I_{OFF} (A/μm)	2.76x10^{-17}	1.54× 10^{-14}
I_{ON}/ I_{OFF}	7.5x10^{11}	1.616x10^{10}
Avg. SS (mV/dec)	26	26
V_{th} (V)	0.31	0.27

HJ VTFET gives better circuit-level performance which will be discussed later in this section. Fig. 5.4(b) compares the transconductance (g_m) characteristics of SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET. It is observed from Fig. 5.4(b) that g_m of SPE Ge/Si HJ VTFET is comparatively much higher than SPE GaSb/Si HJ VTFET with the maximum transconductance of 640 μS in SPE Ge/Si HJ VTFET larger than the maximum transconductance of 66 μS of SPE GaSb/Si HJ VTFET. As g_m represents the ability of the device to convert the gate voltage to drain current, the higher value of g_m in SPE Ge/Si HJ VTFET signifies better rate of gate voltage to drain current conversion than that of the SPE GaSb/Si HJ VTFET. The higher ON-current in SPE Ge/Si HJ VTFET is attributed to higher value of transconductance (g_m) in SPE Ge/Si HJ VTFET. The threshold voltage (V_T) and sub-threshold swing (SS) for both the VTFETs under study has been shown to have nearly same values. However, the higher I_{ON}/I_{OFF} ratio for the SPE GaSb/Si HJ VTFET than SPE Ge/Si HJ VTFET may influence the circuit level behaviour which will be discused later.

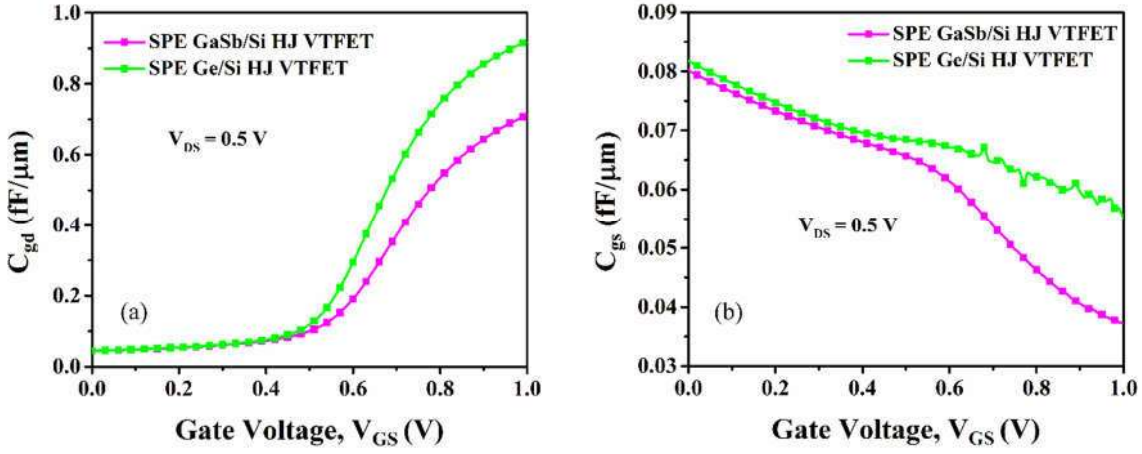

Fig. 5.5: Comparative plot of (a) intrinsic gate to drain capacitance (C_{gd}), and (b) intrinsic gate to source capacitance (C_{gs}) for SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET.

Now we will consider the intrinsic gate-drain capacitance (C_{gd}) and intrinsic gate-source capacitance (C_{gs}) which are important parameters for the RF performance analysis of any MOS transistor. Unlike conventional MOSFETs, C_{gd} in TFETs is treated as parasitic or Miller capacitance which is much larger than C_{gs} [71] as shown in Fig. 5.5 for both the presented VTFETs under consideration. Figure 5.5(a) compares the C_{gd} for two devices whereas Fig. 5.5(b) shows the comparison of C_{gs} of the devices under study. Fig. 5.5(b) shows C_{gs} for the two vertical TFETs where SPE GaSb/Si HJ VTFET has lesser C_{gs} value than that of the SPE Ge/Si HJ VTFET. Note that the larger bandgap of GaSb than Ge causes a larger potential across the GaSb/Si juntion than that of the Ge/Si juntion. This possibly enhances the depletion width under the gate at the Oxide/Si interface in GaSb/Si HJ VTFET than that formed in Ge/Si HJ VTFET device. Since the larger depletion width causes lesser capacitance, the GaSb/Si TFET shows smaller gate capacitance than that of the Ge/Si TFET. This implies that SPE GaSb/Si HJ VTFET with smaller C_{gd} has better circuit-level performance due to smaller parasitic effects

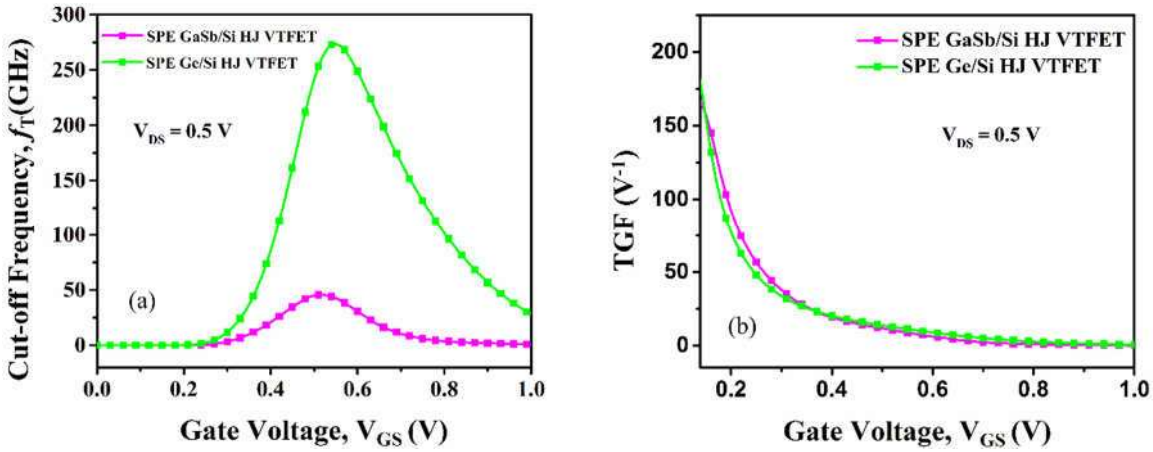

Fig. 5.6: Comparative plot of (a) cut-off frequency, and (b) Transconductance generation factor (TGF) for SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET.

which will be discussed later.

The cutoff frequency (f_T) and transconductance generation factor (TGF) are essential parameters for investigating the RF performance of any MOS transistor. The cut-off frequency (f_T), defined as the frequency at which the short-circuited current gain becomes unity. The formulation to calculate f_T has been given in Chapter-2. The comparison of f_T for both the VTFETs under study shown in Fig. 5.6(a) demonstrates that f_T increases initially with the gate-source voltage due to increase in g_m. But it starts to decrease with increase in gate-source voltage after a certain gate-source voltage due to decrease in g_m at higher gate-source voltage owing to mobility degradation [135]. The SPE Ge/Si HJ VTFET possesses a much larger value of f_T (~272 GHz) than that of the SPE GaSb/Si HJ VTFET (~46 GHz) due to larger g_m in the former TFET.

The transconductance generation factor (TGF) is defined as the capability of a device to convert the current into transconductance. It is a trade-off between power and high-speed operation of any MOS transistor. The mathematical formula to evaluate f_T has

been given in Chapter-2. Fig. 5.6(b) compares TGF as a function of gate voltage. It is noted that SPE Ge/Si HJ VTFET has higher device efficiency (TGF) than that of the SPE GaSb/Si HJ VTFET structure because of higher value in g_m and I_D in the former structure. The device-level performance shows SPE Ge/Si HJ VTFET has better device level performance than SPE GaSb/Si HJ VTFET. However, better I_{ON}/I_{OFF} and lower intrinsic capacitance in SPE GaSb/Si HJ VTFET has the ability to perform better in circuit-level. This is the reason we have focused our analysis on circuit-level performance of the presented TFETs to verify the superiority between the two VTFETs.

5.3.2 Circuit Level Performance Analysis

The circuit-level performance investigation of both the presented VTFETs has been analyzed where a basic digital inverter circuit and a 8T SRAM cell has been explored to analyze inverter performance.

5.3.2.1 Digital Logic Inverter Performance Analysis

The inverter circuit designed by using presented VTFETs i.e SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET is shown Fig 5.2(a). The DC performance of the inverter circuits is evaluated in terms of its static noise margin (SNM) with a supply voltage V_{DD} of 1V. The SNM of an inverter is defined as the maximum DC noise voltage a device can withstand without flipping its contents at the time of operation [91],[106],[107],[137]. It is calculated by placing the voltage transfer characteristics (VTC) along with its inverse simultaneously in a single plot in a pattern known as butterfly curve. Further, the extraction of SNM can be done by using square fitting method in butterfly curve. Fig. 5.7(a) and (b) shows the butterfly curve for the two inverter circuits designed by two different staggered heterojunction based SPE GaSb/Si

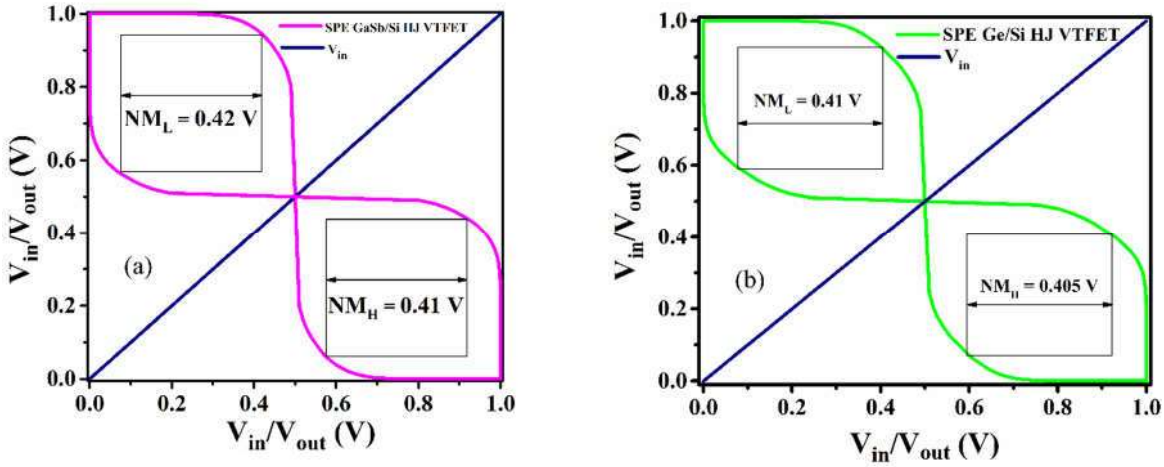

Fig. 5.7: Butterfly curve to calculate static noise margin (SNM) of the inverter based on (a) SPE GaSb/Si HJ VTFET, and (b) SPE Ge/Si HJ VTFET.

HJ VTFET and SPE Ge/Si HJ VTFET presented in this chapter. The largest square fitted in the butterfly curve gives the SNM of the two inverter circuits. The noise margin of the SPE GaSb/Si HJ VTFET based inverter circuit is higher than that of the circuit designed with SPE Ge/Si HJ VTFET because of higher I_{ON}/I_{OFF} ratio in the former structure. The voltages V_{IL} and V_{IH} denote the input voltages for which the voltage gain of the inverter is $dV_{out}/dV_{in} = -1$ [137]. The output voltages like V_{OL} and V_{OH} can also be calculated from the transfer characteristics by considering minimum and maximum value of voltage respectively. Low noise margin (NM_L) and high noise margin (NM_H) can be calculated from the formulas given below [137]:

$$NM_H = V_{OH} - V_{IH} \tag{5.1}$$

$$NM_L = V_{IL} - V_{OL} \tag{5.2}$$

Fig. 5.8(a) and (b) shows the transient behavior of V-TFET inverters simulated for a peak to peak voltage of 1 V for 30 ns without considering any load capacitance. The inset image of Fig. 5.8(a) and (b) show that overshoot in output voltage occurs when

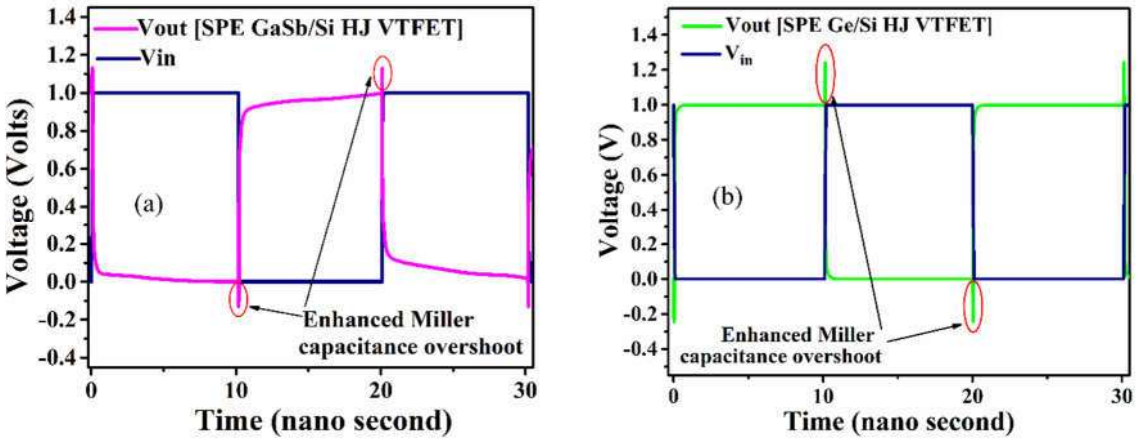

Fig. 5.8: Comparative plot of inverter transient response for (a) SPE GaSb/Si HJ VTFET, and (b) SPE Ge/Si HJ VTFET.

input voltage makes a transition from high to low or low to high. The output overshoot voltage is higher in the inverter designed by using SPE Ge/Si HJ VTFET due to its higher miller capacitance which is discussed earlier in device-level analysis. The higher overshoot voltage lowers the switching speed of the SPE Ge/Si HJ VTFET based inverter circuit. On the other hand, the SPE GaSb/Si HJ VTFET based inverter seems to have lower overshoot voltage than that of the SPE Ge/Si HJ VTFET based inverter which makes it a better candidate for faster switching applications.

5.3.2.2 8T SRAM Performance Analysis

In order to test the feasibility of presented VTFETs in IoT related applications, 8T SRAM memory cell as shown in Fig 5.2(a) has been designed using the presented VTFETs. As discussed in Chapter-4 that low power memory circuit plays essential role in IoT enabled processor and sensors, 8T SRAM cell based on presented VTFETs has been implemented here to evaluate SRAM memory cell related performance between the two VTFETs under study. The SRAM performance parameters such as read

stability, write ability, read delays and write delays are investigated for both the presented VTFETs in the similar manner as discussed in Chapter-4.

The read stability/read margin of a SRAM is calculated in terms of read static noise margin (RSNM) of the cross coupled inverter present in a SRAM. It is the measure of the highest noise value for which the value of the storage node does not change [150]. The RSNM is calculated graphically from the butterfly curve obtained by transfer characteristics of the cross coupled inverter under the operating condition BL= 'V_{DD}', BLB= 'V_{DD}' and WL= 'V_{DD}' and is equal to the side of the largest square that can be inscribed inside smaller lobe of butterfly curve. The voltage values of the storage node in 8T SRAM cell are affected by the bit line voltage due to the presence of inward access transistors (M5 and M7) as shown in Fig. 5.2(b). Hence, the 8T based SRAM cells show low values of read static noise margin (RSNN) as compared to the O-AT 6T SRAM cell. The RSNMs values are calculated graphically as the length of side of the largest square that can be inscribed inside the smaller lobe of the butterfly curve as discussed in Chapter-4. The RSNMs of 8T SRAM cell based on SPE Ge/Si HJ VTFET and SPE GaSb/Si HJ VTFET are plotted in Fig. 5.9(a) for different values of supply voltage. The 8T SRAM cells based on SPE GaSb/Si HJ VTFET shows higher RSNM value as compared to SRAMs using SPE Ge/Si HJ VTFET because of its higher value of I_{ON}/I_{OFF} ratio. The RSNM values are following a increasing trend with respect to the increase in supply voltage same as in Chapter-4.

The write ability is measured in terms of write static noise margin (WSNM) or write margin (WM) of the SRAM cell. For WM calculations, the butterfly curve is plotted for the transfer characteristics of the cross coupled inverter at asymmetrical bit line

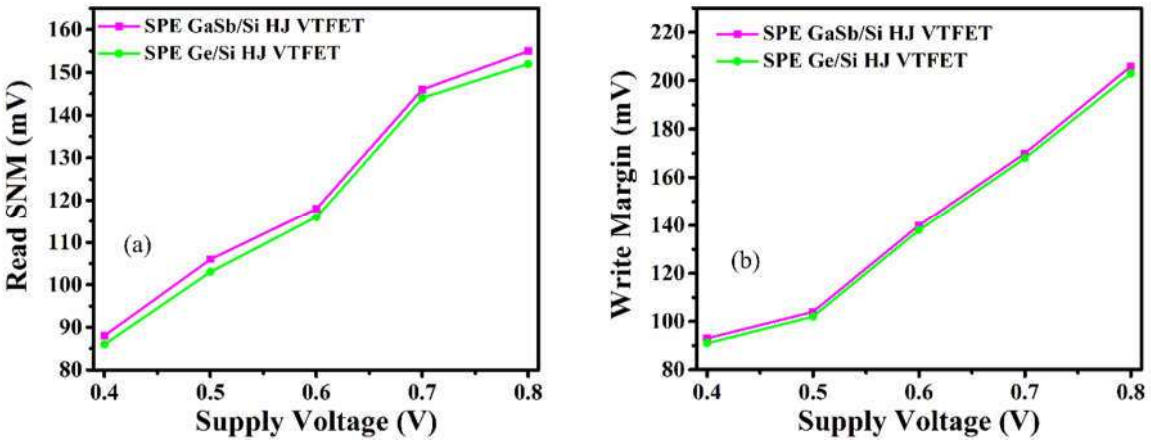

Fig. 5.9: Comparative plot of (a) read static noise margin (RSNM), and (b) write margin for SPE Ge/Si HJ VTFET and SPE GaSb/Si HJ VTFET.

condition i.e. BL= 'V_{DD}' ('0') and BLB= '0' ('V_{DD}') at WL= 'V_{DD}'. The WM is equal to the side of the smallest square that can be made touching both the VTCs. For successful write operation these VTCs should intersect at a single point [115]. Large write margin values are reported in 8T SRAM due to its bidirectional write operation owing to the presence of the transmission gate type access transistor path. Therefore, the WM of 8T SRAM shows a considerable improvement as compared to 6T SRAM structure. The WM plot for different supply voltages of 8T SRAM based on SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET are shown in Fig. 5.9(b). Moreover, the 8T SRAM based on SPE GaSb/Si HJ VTFET shows higher WMs as compared to SPE Ge/Si HJ VTFET. This can be again attributed to improved value of I_{ON}/I_{OFF} ratio of SPE GaSb/Si HJ VTFET over SPE Ge/Si HJ VTFET.

The read delay of the SRAM cell is a measure of the speed of its read operation. The read delay is calculated by pre-charging the bit line capacitances to 'V_{DD}' value and is equal to the time required to obtain 10 % of V_{DD} difference between BL and BLB value after word line voltage is raised to V_{DD} [150]. Fig. 5.10(a) shows the comparison plot of

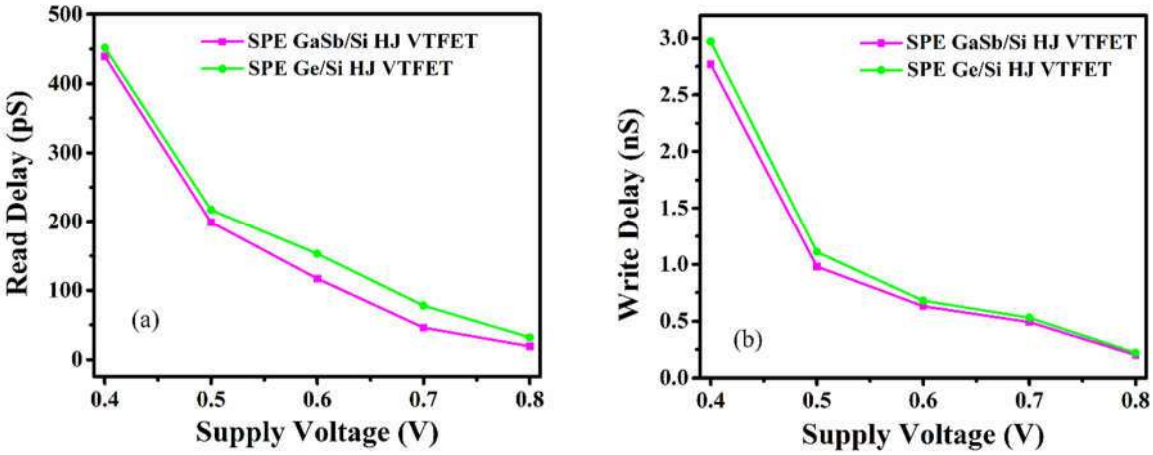

Fig. 5.10: Comparative plot of (a) read delay, and (b) write delay for SPE Ge/Si HJ VTFET and SPE GaSb/Si HJ VTFET.

Read delay of 8T SRAM based on SPE Ge/Si HJ VTFET and SPE GaSb/Si HJ VTFET for supply voltage range of 0.4 volts to 0.8 volts. The 8T SRAM cells based on SPE Ge/Si HJ VTFET have higher values of the read delays because of the enhanced intrinsic gate capacitances (parasitic capacitances) of SPE Ge/Si HJ VTFET compared to SPE GaSb/Si HJ VTFET. As low read delays are always preferred to have faster operation, the VTFET with GaSb/Si heterojunction is more useful than the VTFET Ge/Si heterojunction.

The write delay of the SRAM cell is equal to the time required for charging or discharging of the storage node to 50 % of its initial value after the word line is activated (WL= 'V_{DD}') [150]. The write delay variation of 8T SRAM employing SPE Ge/Si HJ VTFET, and SPE GaSb/Si HJ VTFET is given in Fig. 5.10(b). SPE GaSb/Si HJ VTFET shows low value of write delay compared to SPE Ge/Si HJ VTFET. This is because of higher I_{ON}/I_{OFF} ratio of the SPE GaSb/Si HJ VTFET compared to SPE Ge/Si HJ VTFET which causes faster charging and discharging of the storage nodes. It can be concluded from the above discussion that the SPE GaSb/Si HJ VTFET shows better

static noise margins with less read and write delays because of its higher higher I_{ON}/I_{OFF} ratio which in turn makes it suitable for faster memory related operations over SPE Ge/Si HJ VTFET.

5.4 Conclusion

In this chapter, device and circuit level performances have been investigated for two different source material (Ge and GaSb) based source pocket engineered VTFETs i.e SPE Ge/Si HJ VTFET and SPE GaSb/Si HJ VTFET. The device-level performance presented in this chapter has been analyzed by considering some important performance parameters such as drive current (ON-current), OFF-state current, SS, I_{ON}/I_{OFF} ratio, transconductance (g_m), intrinsic gate to drain capacitance (C_{gd}), intrinsic gate to source capacitance (C_{gs}), cut-off frequency (f_T), and transconductance generation factor (TGF) whereas circuit-level performance has been investigated in terms of static and time varying behavior by considering a digital logic inverter circuit and 8T SRAM cell for both the VTFETs under study. 8T SRAM has been considered because of use of bi-directional access transistor in 8T SRAM based TFET which provides higher margins and less delays compared to 6T counterpart. Although, the device level performance shows some improved performance parameters for SPE Ge/Si HJ VTFET than SPE GaSb/Si HJ VTFET, the higher I_{ON}/I_{OFF} ratio and lower intrinsic gate capacitance in SPE GaSb/Si HJ VTFET shows better circuit level performances. Although, Ge/Si heterojunction based TFET has been already explored in both device and circuit level analysis, GaSb/Si heterojunction based TFET shows improved performance parameters in circuit level which can be useful for low power IoT based applications.