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Memristive Ferroelectric FET for 1T-1R Nonvolatile Memory With Non-Destructive Readout

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ABSTRACT Energy-efficient non-volatile memory that supports non-destructive read capabilities is in high demand for random-access memory applications. This article presents the proposal and demonstration of a 1T-1R non-volatile memory cell, which has distinct read and write paths that utilize a memristive variant of the ferroelectric field effect transistor (MFeFET) for data storage. Through a combination of experimentally calibrated models and TCAD-based mixed-mode simulations, the proposed MFeFET-based memory cell is demonstrated to achieve a non-destructive read operation and higher read current at low operating voltages. Furthermore, the memory cell demonstrates a 50% reduction in read latency compared to spin transfer torque (STT) magneto-resistive random-access memory (MRAM) technologies, positioning it as a highly efficient solution for next-generation non-volatile memory applications.

INDEX TERMS Fin field effect transistor (FinFET), ferroelectric field effect transistor (FeFET), magnetic tunnel junction (MTJ), junctionless-accumulation-mode (JAM), ferroelectric random-access memory (FeRAM), spin transfer torque (STT).

I. INTRODUCTION

A one transistor one memristor (1T-1M) memory cell has been trending in nonvolatile memory and neuromorphic computing applications. 1T-1M hybrid memory structure [1] where one transistor is paired with one memristor to form a basic unit of memory storage. It leverages the switching behavior of memristors and the control provided by transistors. Different memory technologies like spin transfer torque magneto resistive random-access memory (STT-MRAM) [2], resistive random-access memory (ReRAM) [3], [4], and phase-change random access memory (PCRAM) [5] use this 1T-1M structure. However, these memory technologies still encounter challenges like high memory access energy and latency, limited compatibility with complementary metal oxide semiconductor (CMOS) processes, poor scalability, endurance limitations, and the complexity of peripheral circuitry. Therefore, further research on non-volatile memory (NVM), from the device level to the architectural level, is essential to enhance performance and flexibility [6].

The demand for memory elements based on ferroelectric field effect transistors (FeFET) [7] is driven by their ability to retain data without power, small physical footprint, ability to be rewritten, operation at low voltages, and fast programming times [8]. The remarkable compatibility of $Hf_{0.4}Zr_{0.6}O_2$ (HZO) [9], [10] with CMOS technology makes it an ideal material for FeFET and ferroelectric capacitors [11]. Moreover, these materials exhibit strong ferroelectric properties even at film thicknesses below 10 nm [11], while remaining compatible with CMOS technology. The FeFET based memory has one notable advantage compared to the one transistor one ferroelectric capacitor based (1T-1C) ferroelectric random-access memory (FeRAM) [12], [13] that is, the FeFET could perform the non-destructive read. FeFET is recognized as a potential next-generation embedded NVM device due to its relatively low write latency, non-destructive read [14], and ultralow switching energy.

The FeFET based 2-transisitor (2T) NVM [15] is shown in Fig. 1(a). This memory cell regulates the FeFET gate voltage through an access transistor, however, concurrently the source

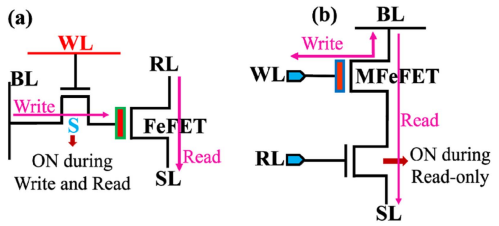

FIGURE. 1. FeFET memory cell proposed in (a) Ref. [15](b) in this paper.

and drain voltages of FeFET are zero during the write operation. This results in a coupled write and read path while also requiring high bit line (BL) voltages for writing to FeFET. This requires higher size and operating voltage requirement of the select transistor (S) to set/reset the memory state, leading to reduced energy and area efficiency. Further, they generally suffer from poor endurance [16] and require an additional read voltage to read the data when power is OFF, making the cell still vulnerable to destructive read operation.

In this paper we propose a new 1T-1FeFET memory cell which closely replicates the properties of 1T-1R [17], [18] or 1T-1M based NVM memory cells. Herein, we are modifying the properties of the traditional ferroelectric fin field effect transistor (FeFinFET) to make it work like a memristor. We can emulate the low-resistance state (LRS) and high-resistance state (HRS) of the memristor in our modified FeFinFET structure without changing the process of fabrication. The proposed cell further advances the 1T-1FeFET architecture as proposed in [19] and illustrated in Fig. 1(b), while incorporating modified FeFinFET devices that exhibit memristor-like characteristics. The proposed device is referred to as the memristive variant of FeFET (MFeFET) in the paper. Furthermore, through mixed mode simulations, we demonstrate a 1T-1FeFET-based memory cell using the proposed memristive variant FeFET. This memory cell architecture offers a unique feature, i.e., a non-destructive read when compared with a one-bit non-volatile memory circuit discussed in [15] and [19]. The previous implementations require an extra read voltage that reads the stored information by disturbing the polarization of ferroelectric material. The advancements achieved in the proposed memory cell are as follows:

1) This architecture allows data to be written directly to the gate of FeFET and enables data to be read without any read voltage applied to the FeFET, hence decoupling the write and read path and reducing the possibility of destructive read operation. The write and read paths are shown in Fig. 1(b).
2) The write and read paths are different, so it can enhance the performance of the memory system through easier access to the data, improve endurance, better scalability, increase energy and area efficiency. Herein, the size of the select transistor responsible for read operation can also be minimized.
3) It is compatible with 1T-1M memory counterparts like STT MRAM in terms of the peripheral circuitry-like sense amplifier, as the proposed cell can use current/voltage mode sense amplifiers to directly sense the current flowing through the MFeFET.
4) Like other memristors, it has the ability to store multiple levels of resistance, which enables multi-bit storage in a single cell. This means more data can be stored in the same physical space, increasing the possibility of high storage capacity within the same footprint.
5) MFeFET involves modifications in the device structure only. Therefore, it is compatible with front-end-of-the-line (FEOL) systems. The existing 1T-1R counterparts like STT-MRAM and ReRAM require additional back-end-of-line (BEOL) processing, significantly increasing the cost overheads. These advancements are summarized in Fig. 2.

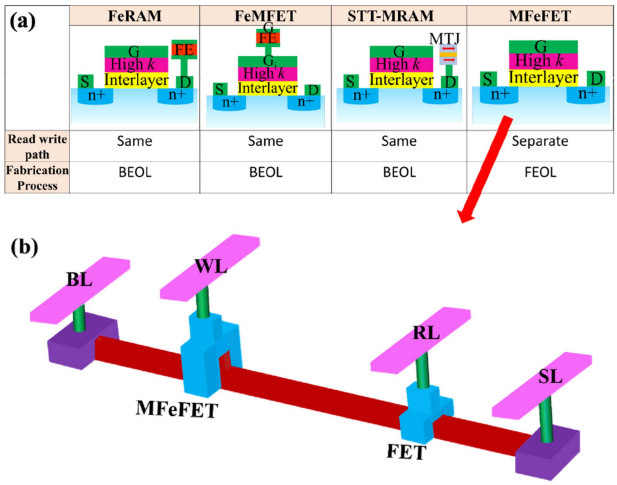

FIGURE. 2. (a) Comparison of MFeFET-based memory with other types of NVM memory. (b) 3D visualization of 1T-1MFeFET.

In this paper, we propose and demonstrate MFeFET and the proposed memory cell using a well-calibrated technology computer-aided design (TCAD) simulation setup. We further use NVSim to estimate the predictive read performance at the system level and show the performance improvement and suitability in memory applications compared with the MRAM. This paper is organized into five distinct sections. Section II presents the device architecture, calibration of the TCAD simulation setup, and parameters of MFeFET. Transfer and memory cell characteristics of the proposed device are presented in Section III. In Section IV, the architectural-level design estimation is discussed. The article concludes in Section V.

II. PROPOSED MEMRISTIVE VARIANT OF FEFET (MFEFET)

This section discusses the process of converting a scaled ferroelectric FinFET into an MFeFET. Section A covers the optimal device parameters as selected from previously reported designs. In Section B, the calibration of the TCAD simulation setup with reported experimental data is discussed. The threshold voltage analysis, along with variations in the width and height of the fin, is discussed in Section C, while the modified device parameter for MFeFET is elucidated in Section D.

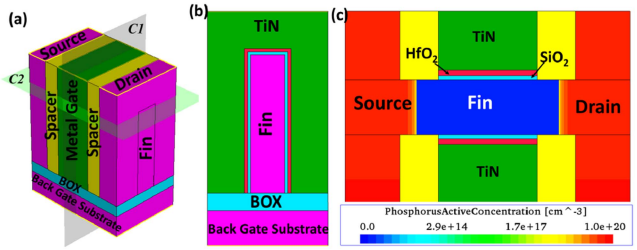

FIGURE. 3. (a) 3D n-MOS SOI FinFET structure, created through process emulation. The 2D cross-section of the three-dimensional FinFET is shown along cut-plane (b) *C1* and (c) *C2*.

A. DESIGN CONSIDERATION OF PROPOSED MFEFET

In the usual ultra-scaled FinFETs, the threshold voltage (V_{th}) is primarily influenced by the gate work function [20]. However, the dimensions of fin height (H_{fin}) and width (W_{fin}) also affect the V_{th}. In [21], [22], [23] for inversion-mode (IM) FinFET, the variation of V_{th} roll-off with W_{fin} and H_{fin} is observed, and similar types of variation are also shown in [24], [25] for junctionless accumulation mode (JAM) FinFET. G. Pei et al. [22] and Kedzierski et al. [23] have observed that for a specific combination of H_{fin} and W_{fin}, the V_{th} of FinFET is negative. The same concept can be implemented in FeFinFET devices. Hence, in this paper, we propose the novel idea of obtaining a high drain current of FeFinFET at zero gate voltage by selecting specific values of H_{fin} and W_{fin} in FeFinFET, so that we can read the stored data in memory without applying read voltage. This device has been referred to as MFeFET, and has been detailed in Section D. Through TCAD simulations, we demonstrate negative low and high threshold voltages by appropriately designing the device. Herein, a low threshold is associated with the down polarization of the ferroelectric material and a high threshold with the up polarization. Typically, the high threshold voltage (V_{thH}) is positive, with zero gate bias. To ensure the FeFinFET device operates in a normally ON state, behaving like a memristor, both low threshold (V_{thL}) and high threshold (V_{thH}) voltages must be negative to allow sufficient drain current to flow at zero gate voltage.

B. CALIBRATION OF TCAD SIMULATION SETUP

We have considered 3-D FinFET, which was created through process emulation in Sentaurus TCAD [26]. The design is based on the SOI device architecture. Fig. 3 presents the 3D device structure alongside a 2D cross-section of the n-type FinFET. Further, the nominal TCAD simulation deck parameters of FinFET are shown in Table 1. The n-type FinFET structure illustrated in Fig. 3(a) is simulated using TCAD. In aggressively scaled FinFET devices, the contact area within the S/D region is gradually reduced. This reduction leads to a notable increase in contact resistance [30]. To address this, contact physics is incorporated by introducing contact resistance (R_T) in series with the drain and source terminals, as depicted in Fig. 4(a) and (b). The value of contact resistivity (ρ_C) between the n-type epitaxial layer and the silicide is based on experimental data given in [29] and [31] for aggressively scaled FinFETs at 7 nm and beyond. The contact physics incorporated has been benchmarked against experimental data.

TABLE 1. Experimentally Calibrated TCAD Simulation Deck Parameters [27], [28], [29]

Device Parameter	Value
Fin Width	10 nm
Fin Height	40 nm
Fin Pitch	26 nm
Gate length	18 nm
Channel Doping (p-type)	1 x 10^{16} (cm^{-3})
Source/Drain Doping (n+ type)	1 x 10^{20} (cm^{-3})
Interface Oxide (SiO_2)	0.75 nm
Gate Oxide (HfO_2)	1 nm
Spacer width	7 nm
Gate Work-function	4.5 eV
Contact resistivity (ρ_c)	5 × 10^{-10} Ω-cm^2

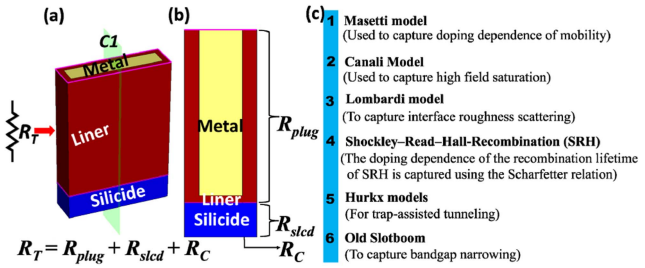

FIGURE. 4. (a) 3D contact structure created with the structure editor in TCAD. (b) 2-D cross-sectional view of the contact along section *C1*. (c) The list of models is included in the calibrated Sentaurus TCAD deck.

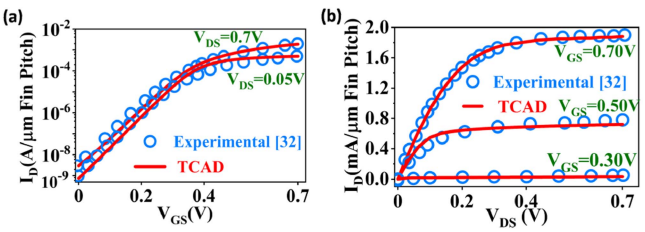

FIGURE. 5. (a) $I_D - V_G$ characteristics, along with a comparison with experimental data presented in [32]. (b) $I_D - V_D$ characteristics, along with a comparison with experimental data presented in [32].

The electrostatic and transport properties of the FinFET were calibrated by comparing them to the experimental data collected from Intel's measurements in [32]. The list of models included in the TCAD deck is shown in Fig. 4(c). Further, Fig. 5(a) and (b) show $I_D - V_G$ and $I_D - V_D$ characteristics, respectively, with a comparison made using experimental data [32].

On this calibrated FinFET, a metal-ferroelectric-insulator-semiconductor (MFIS) gate stack that covers the entire fin is inserted so that the FinFET device is turned into FeFinFET [see Fig. 6(a)]. The parameters of ferroelectric material are shown in Table 2. Fig. 6(b) presents the 2D view of the FeFinFET device across cut-plane *C1*, where a 10 nm thick HZO

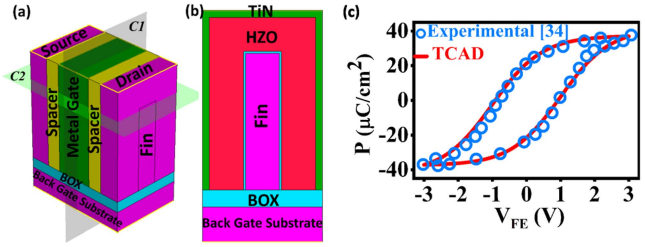

FIGURE. 6. (a) 3D n-MOS SOI FeFinFET structure, created through process emulation. (b) The 2-D cross-section of the three-dimensional FeFinFET across Cut-plane *C1*, (c) P-V calibration of FECap based on the experimental data presented in [34].

TABLE 2. Experimentally Validated Model Parameters for FeCAP

Parameter	Value
HZO thickness	10 nm
Remnant Polarization (P_r)	25 x 10^{-6} C cm^{-2}
Saturation Polarization (P_s)	42 x 10^{-6} C cm^{-2}
Coercive Field (F_C)	1 x 10^{6} V cm^{-1}

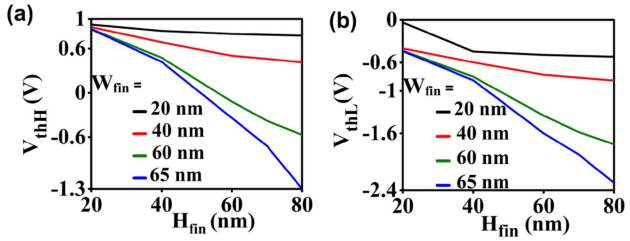

FIGURE. 7. Dependence of threshold voltage roll-off on H_{fin} for (a) forward voltage sweep and (b) reverse voltage sweep.

ferroelectric layer is above the gate oxide layer, and forms a ferroelectric capacitor (FeCap).

The structure of the FeFinFET, as shown in Fig. 6, includes a 10 nm thick HZO in the gate stack to integrate non-volatile characteristics. The history dependence of FeCap, as well as the transient behavior in ferroelectric, was accounted by using a computationally efficient model of the ferroelectric capacitor as shown in [26], [33]. The model parameters were tuned [see Table 2] to accurately match the polarization-voltage characteristics that were experimentally observed in [34]. Fig. 6(c) displays the comparison for a FeCap, highlighting an accurate representation of the Preisach hysteresis along with all essential properties necessary for our simulations.

C. DEPENDENCE OF THRESHOLD VOLTAGE (V_{TH}) ROLL-OFF ON HEIGHT (H_{FIN}) AND WIDTH (W_{FIN}) OF FIN

The dependences of V_{th} roll-off on H_{fin} and W_{fin} of FeFinFET are demonstrated in Figs. 7 and 8, respectively. Herein, the threshold voltage is measured at a drain current of 10^{-6} A at $V_{DS} = 0.1$ V. In Fig. 7, as H_{fin} is increased from 20 to 80 nm, the V_{th} of the device is decreased for different W_{fin}. Fig. 7(a) depicts the high threshold voltage (V_{thH}) variations when the gate voltage sweeps from -4 V to $+4$ V, while

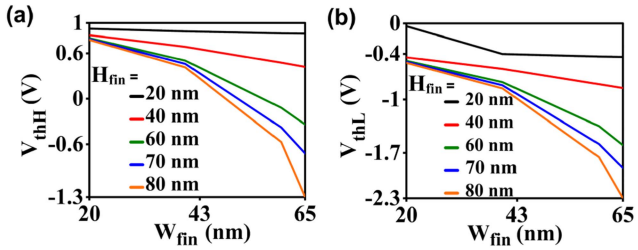

FIGURE. 8. Dependence of threshold voltage roll-off on W_{fin} for (a) forward voltage sweep, (b) reverse voltage sweep.

Fig. 7(b) displays the low threshold voltage (V_{thL}) variations when the gate voltage sweeps from $+4$ V to -4 V. Similarly, the variations of V_{thH} and V_{thL} as W_{fin} are increased from 20 to 65 nm for different H_{fin} are shown in Fig. 8(a) and (b), respectively. Herein, we have observed a similar trend for V_{th} in our calibrated FeFinFET, as seen in [22]. So, from the above analysis of V_{th}, we have found a critical value of H_{fin} and W_{fin} for which both the voltages are negative so that the device is ON while the gate voltage is zero. This confirms the normally-ON memristor like characteristics with a distinct low resistance state (due to up polarization in the ferroelectric material) and a high resistance state (due to down polarization in the ferroelectric material).

D. DEVICE PARAMETER FOR MFEFET

In scaled FinFETs, where H_{fin} is significantly greater than W_{fin}, the threshold voltage does not become negative. However, from the above section, it is clear that the V_{thH} and V_{thL} both are negative for $W_{fin} = 60$ nm and $H_{fin} = 70$ nm. This is due to the weaker electrostatic control of the gate over the channel and increased drain-induced barrier lowering (DIBL) [22]. This behavior is observed in both IM and junctionless-accumulation-mode (JAM) FeFinFET architectures, as confirmed by the TCAD simulation results shown in Figs. 7 and 8. Herein, a current of 39 μA (2 μA) is obtained at $V_{GS} = 0$ V, $V_{DS} = 0.1$ V for down (up) polarization, making MFeFET a normally-on device. In these simulations, the parameters of the proposed MFeFET device are the same as those specified in Table 1, with the exception of the values of W_{fin} and H_{fin}, which are 60 nm and 70 nm, respectively.

III. TRANSFER AND MEMORY CELL CHARACTERISTICS

To confirm the retention of non-volatile data, we obtain the $I_D - V_G$ curve of the MFeFET under both forward and reverse bias conditions, as described in Section A. The working of proposed 1T-1MFeFET memory cells, which have non-destructive read, is discussed in Section B. Further, the comparison of current during a read operation is explained in Section C.

A. TRANSFER CHARACTERISTICS AND MEMORY WINDOW (MW) OF PROPOSED MFEFET

Fig. 9(a) illustrates the hysteretic behavior of MFeFET, which arises from the presence of a ferroelectric layer in the gate

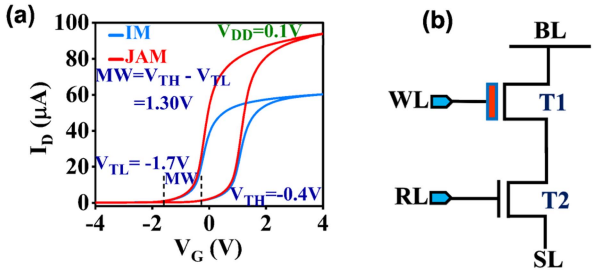

FIGURE. 9. (a) Comparison of transfer characteristics of MFeFET for JAM and IM architecture (b) proposed 1T- 1MFeFET-based NVM.

stack. The memory window (MW) calculated from the $I_D - V_G$ curve is 1.30 V, which is the same as IM FeFinFET. Here, during the reverse sweep (+4 V to −4 V), the device exhibits a low threshold voltage (V_{thL}) of −1.7 V, whereas, under the forward sweep (−4 V to +4 V), it demonstrates a high threshold voltage (V_{thH}) of −0.4 V.

The proposed MFeFET has the capability to read at zero gate voltage because its V_{thH} and V_{thL} are both negative. Here, we are also demonstrating the characteristics of MFeFET by utilizing a JAM architecture [24], [25], [35] of FinFET. Additionally, the device parameters for the JAM FeFinFET are identical to those in Table 1, except for the doping levels. In the n-channel JAM device, the drain, channel, and source regions follow an n+ - n- - n+ configuration. The doping concentration for the drain and source is 1×10^{20} /cm^{-3}, whereas channel doping is 1×10^{16} /cm^{-3}. From Fig. 9(a), it is observed that JAM architecture-based MFeFET has high on-current when V_{DS} is high, i.e., beyond 1 V, in comparison to the result from IM architecture.

B. PROPOSED 1T-1MFEFET NON-VOLATILE MEMORY CELL WITH A NON-DESTRUCTIVE READ OPERATION

This subsection demonstrates the proposed circuit operation of 1T-1MFeFET-based NVM. To demonstrate the non-destructive read functionality of the MFeFET device, transient mixed-mode simulations were conducted using Sentaurus TCAD for the 1T-1MFeFET memory cell shown in Fig. 9(b). Herein, MFeFET (T1) is normally ON and works like a memristor. Due to the three-terminal architecture of the MFeFET, the cell is constructed with independent paths for writing and reading, enabling the simultaneous optimization of both operations. The write path includes an MFeFET (T1) that is activated by a write select line (WL) and a bit line (BL) to allow for targeted writing to the cell when the WL is set to 'HIGH.' In the read path, a pristine n-FinFET (T2) is utilized, with the read select line (RL) connected to its gate and the source line (SL) grounded. Note that the bit line (BL) is connected to the drain of T1 and could vary from 0 to 2 V when write and read operations are performed. During the writing process, RL is kept at a 'LOW' state. Conversely, in the reading phase, both RL and BL are set to 'HIGH.' The transient analysis demonstrating these write and read operations and a comparison with the 1T-1FeFET cell implemented in [19] is presented in Fig. 10.

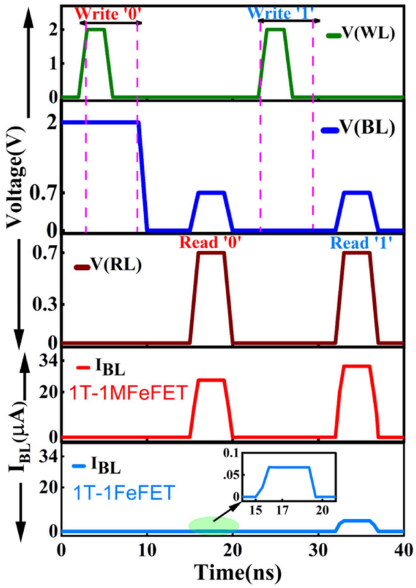

FIGURE. 10. 1T-1MFeFET memory cell transient waveform.

1) WRITE OPERATION

- During the write operation, WL is 'HIGH' and RL is 'LOW'
- To write '0', a positive voltage is applied to BL, which causes T1 to enter an HRS. In contrast, to write '1', BL goes 'LOW', which causes the V_{GS} of T1 to be positive, leading to the LRS of T1. The LRS and HRS are confirmed by the current obtained at BL through simulations during a read operation, which is also shown in Fig. 10 and discussed further.

2) READ OPERATION

- Throughout the read operation, the RL and BL are 'HIGH. The WL is set to 'LOW' to ensure that the gate of T1 is unbiased for a non-destructive read operation. The RL voltage applied to the gate terminal turns the transistor T2 to an ON state, and the current through SL can be sensed for the stored bit normally through a sense amplifier. The resulting drain current in T2 is influenced by the stored polarization, as shown in Fig. 10, verifying the memory cell characteristics. The current is high (32 μA) when MFeFET is in LRS and low (25 μA) when it is in HRS. The 1T-1FeFET cell remains in an OFF state during read '0' operation and a very low current of 50 nA flows through it as opposed to 25 μA for the 1T-1MFeFET cell. Hence, the 1T-1FeFET memory cell displays significantly lower sensitivity compared to the 1T-1MFeFET if the voltage/current mode sensing scheme is used. These read schemes are employed in other non-volatile memristor-based memory technologies like STT-MRAM and ReRAM.

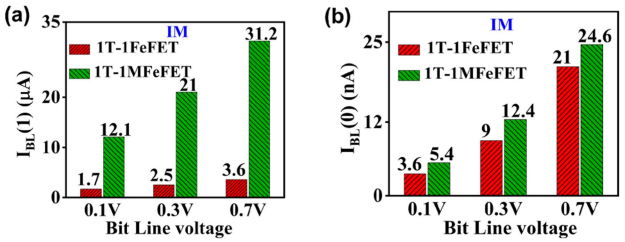

FIGURE. 11. Comparison of Bit line current in 1T-1MFeFET based memory cell for different Bit line voltage during (a) Read '1' (b) Read '0'.

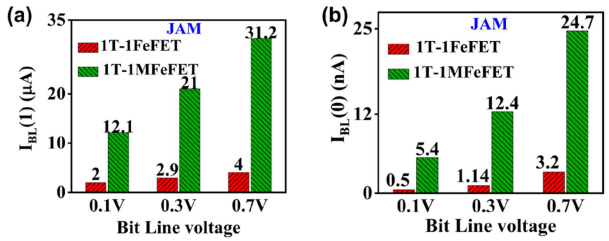

FIGURE. 12. Comparison of Bit line current in 1T-1MFeFET based memory cell for different Bit line voltage during (a) Read '1' (b) Read '0'.

C. COMPARISON OF CURRENT DURING READ OPERATION

In a memory cell, a higher read current generates a stronger signal, which enhances the signal-to-noise ratio. This makes it easier for the sense amplifiers to distinguish between different data states (e.g., between a '0' and a '1'). A higher read current can increase the sensitivity of the memory cells to the stored charge/state. This can be especially useful in detecting weakly stored data, ensuring that even marginally stored bits are accurately read. In our proposed memory cell, described in the above subsection, we have used an MFeFET device, which offers two advantages during the read operation: firstly, the cell does not need an extra read voltage to the gate of MFeFET, and secondly, it provides a higher read current at low read voltages and hence, enhances the read signal reaching the sense amplifiers. The comparison of read current flowing through the bit line in a 1T-1MFeFET-based memory cell is presented in Figs. 11 and 12. Herein, the proposed MFeFET device shows a higher read current in comparison to the IM counterpart. In Fig. 11, we have used the FinFETs IM structure, while in Fig. 12, the JAM structure is used for 1-bit data storage.

IV. PERFORMANCE EVALUATION OF 1T-1MFEFET MEMORY CELL ARRAY ARCHITECTURE USING NVSIM

We utilize NVSim [37] to extend our device-level estimation study to memory array architecture. Since NVSim does not inherently support FeFET memory cells, we created a custom definition for the memory cell. In this work, we have used NVSim software to model a 1T-1MFeFET cell, emulating it as the STT MRAM cell that uses magnetic tunnel junction (MTJ) as a memristive device. Specifically, we redefined the LRS and HRS of the MTJ to mimic the behavior of FeFET. The

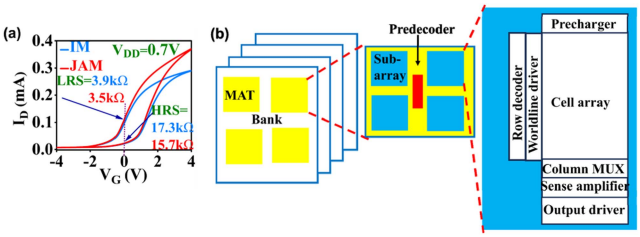

FIGURE. 13. (a) Representation of LRS and HRS in transfer characteristics of MFeFET. (b) NVsim Framework.

TABLE 3 Key Parameter for MFeFET and MTJ

Parameter	MFeFET		MTJ
	IM	JAM	[36]
LRS (kΩ)	3.9	3.5	3.12
HRS (kΩ)	17.3	15.7	5.41
Read voltage (V)	0.7	0.7	0.7
Sensing mode	Current		Current

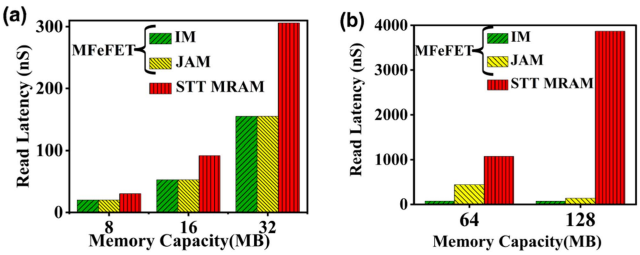

FIGURE. 14. (a) And (b) comparison of read latency for different memory capacities.

LRS, typically corresponding to the parallel magnetization of the MTJ layers, is treated analogously to the downward polarization state of an MFeFET, whereas the HRS is associated with anti-parallel magnetization and corresponds to the upward polarization state of MFeFET. This redefinition allows for the estimation of the read performance of the proposed architecture within the MTJ framework, facilitating the study of its performance in memory and logic circuits.

We integrate a MFeFET cell definition using the LRS and HRS results obtained from transient analysis MFeFET using TCAD simulations. The downward polarization state of the MFeFET, referred to as the LRS, is calculated as 3.9 kΩ at $V_{GS} = 0$ V and $V_{DS} = 0.7$ V, as depicted in Fig. 13(a). Conversely, the upward polarization state, corresponding to the HRS, yields a resistance of 17.3 kΩ under the same bias conditions, as shown in Fig. 13(a).

NVSim simulates the non-volatile architecture in the same manner as the framework shown in Fig. 13(b) for both IM and JAM FeFinFET cell configurations across a range of array capacities, from 1 MB to 128 MB. The parameters of a 1T-1MFeFET cell are listed in Table 3. The performance metric, such as read latency, is obtained from the simulation. We compared the read latency projections of the 1T-1MFeFET with STT-MRAM, as illustrated in Fig. 14, using NVSim.

TABLE 4. Benchmarking MFeFET With Other Nonvolatile Memories

Parameter	FeFET [8]	FeRAM [13]	FeMFET [38]	STT-MRAM [39]	RRAM [40]	MFeFET (This Work)
Structure	1T	1T-1C	1T-1C	1T-1MTJ	1T-1R	1T-1R
Read scheme	Non-Destructive	Destructive	Non-Destructive	Non-Destructive	Non-Destructive	Non-Destructive
Write voltage	4.0 V	3.3 V	1.8 V	1.5 V	4 V	1.5 V
Multi-bit	Good	Bad	Good	Bad	Good	Good
Read latency	Medium	High	Medium	Medium	Medium	Low
Read voltage requirement	Yes	Yes	Yes	Yes	Yes	No
Multi-port	Yes	No	Yes	No	No	Yes

The proposed NVM architecture shows a 50% improvement in read latency over STT MRAM.

V. CONCLUSION

The comparison of the proposed 1T-1MFeFET memory with other types of embedded NVM is shown in Table 4. The predictive performance of NVM using MFeFET is better in terms of write voltage, read speed, read latency, fabrication process, and eliminates the requirement of an extra read voltage. Thus, MFeFET is a promising NVM option for high-performance, low-power RAM applications.

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