Chapter 2

SVM techniques to reduce the CMV in USMC

2.1 Introduction

Modulation techniques play a crucial role in producing output voltages in AC-AC converters. Various modulation techniques have been reported to control the switches of the USMC. Initially, MC is controlled by the Venturini algorithm [11,74]. However, this switching strategy limits lower voltage gain ($G \leq 0.5$). The maximum voltage gain obtained by using the Venturini switching strategy is 0.5. In [75], the authors introduced the scalar modulation technique. The term "scalar" implies that only the magnitude of the vectors is modified while their direction remains unchanged. This modulation technique often achieves control objectives such as output voltage regulation and input power factor correction. The scalar modulation method involves adjusting the amplitude of the input voltage vectors to achieve the desired output voltage and current waveforms. The scalar modulation method primarily adjusts the magnitudes of vectors while keeping their directions constant, which can lead to limited control precision compared to more advanced modulation techniques. The maximum voltage gain of this method is 0.5. In [11], the successful integration of third harmonics into both input and output voltage waveforms has been implemented to improve the maximum voltage transfer ratio, achieving a ratio of up to 0.866. The carrier modulation technique is another modulation technique to control matrix converter switches, but the main limitation of this method is to generate a variable gradient carrier for the output stage

(VSI) [76, 77]. To achieve balanced sinusoidal input and output waveforms with an adjustable input displacement angle, matrix converters are controlled by Space Vector Modulation (SVM) technique. The SVM approach was initially suggested in [78–81]. This evolution aims to fully harness the potential of matrix converters by enabling control over the input power factor, irrespective of the output power factor, maximizing the utilization of input voltages, and minimizing the number of switch commutations in each cycle period. Additionally, this strategy offers a clear understanding of the modulation process without necessitating a fictitious DC-link and eliminates the need to incorporate third-harmonic components. The significant advantages of the SVM technique are:

- SVM efficiently uses the input voltage, leading to improved converter output voltage. It helps to maximize the power transfer capability of the converter without causing over-modulation issues.
- SVM provides better output waveform quality with reduced harmonic distortion than scalar modulation. It helps in meeting power quality standards by minimizing the presence of harmonics in the output voltage.
- SVM enables precise control over the output voltage's magnitude and phase. This is particularly beneficial in applications where accurate control of the output is essential, such as motor drive applications.
- SVM allows for better utilization of the available voltage vectors in the converter. It optimally distributes the available voltage vectors in the space vector diagram, resulting in a higher voltage utilization factor. This can lead to higher output voltage and better utilization of the converter's capacity.

Due to the advantages mentioned above, the conventional SVM technique for USMC is discussed in this chapter, along with the different space vector modulation techniques used to reduce the CMV in USMC. Figure 2.1 shows the ultra sparse matrix converter circuit diagram. It consists of CSR and VSI. Because the USMC is a two-stage topology, the modulation of the CSR and VSI can be done separately. Afterward, the resulting dwell times from this analysis can be combined to complete the USMC modulation process. The SVM technique controls both CSR and VSI switches. Implementation of the SVM technique at each stage is explained below:

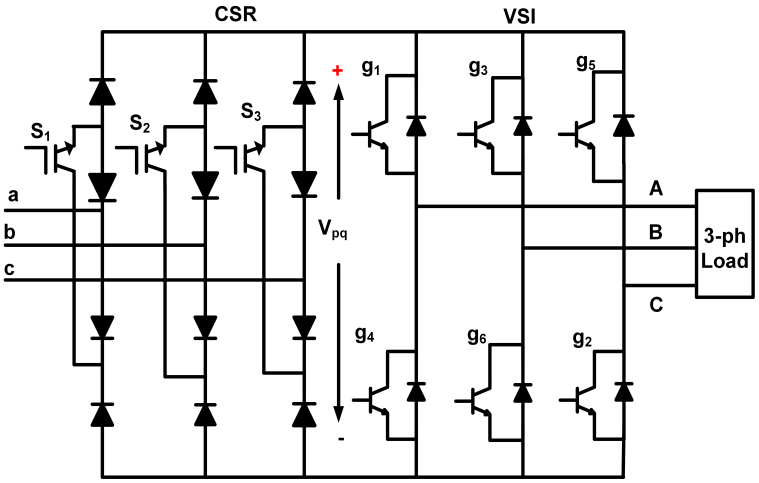


Figure 2.1: Ultra sparse matrix converter

2.2 SVM for CSR

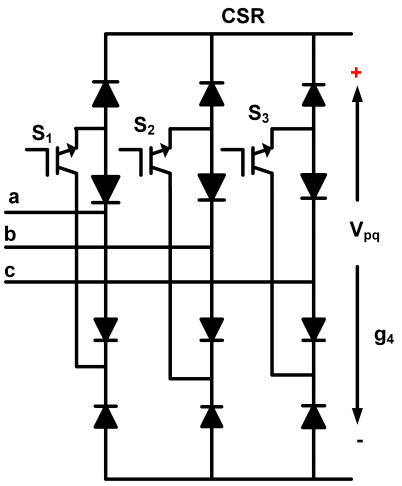


Figure 2.2: USMC's current source rectifier

CSR of USMC consists of three unidirectional switches (S_1, S_2, S_3) and twelve diodes, as shown in Figure 2.2. There are three input terminals (a, b, c) and two output terminals (p, q). So, nine (3^2) switching states are present in the space vector diagram, as shown in Figure 2.3. It consists of six sectors, six active vectors (I_{ab}, I_{ac}, I_{bc}, I_{ba}, I_{ca}, I_{cb}) and three zero vectors (I_{aa}, I_{bb}, I_{cc}). The reference input current vector I_{ref} is created with the help of two adjacent active vectors in each sector. The dwell times of the active vectors are given by equation (2.1). Here dI_{ab} and dI_{ac} are dwell times for the active vectors I_{ab} and I_{ac}, respectively. m_i is the CSR modulation index, and α is the angle between the active vector and reference vector.

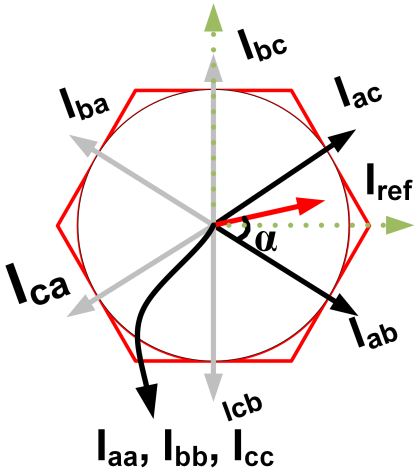


Figure 2.3: Space vector diagram for CSR

$$
\begin{aligned}
I_{ref}e^{j(\alpha)} &= \frac{2}{\sqrt{3}}[dI_{ab}I_i e^{-j(\pi/6)} + dI_{ac}I_i e^{j(\pi/6)}] \\
dI_{ab} &= m_i sin(\frac{\pi}{3} - \alpha), \quad dI_{ac} = m_i sin(\alpha) \\
dI_o &= 1 - dI_{ab} - dI_{ac} \\
m_i &= \frac{I_{ref}}{I_i}
\end{aligned}
\tag{2.1}
$$

The switching pattern of the CSR is shown in Figure 2.4. The switching sequence starts and ends with the active vector I_{ab}. The switching sequence in one cycle (T_S) is ${}_0|I_{ab}$ - I_{ac} - I_{aa} - I_{ac} - $I_{ab}|_{T_S}$. After applying three-phase balanced supply (v_{an}, v_{bn}, v_{cn}) to the CSR, the obtained DC-link voltage is

$$
\begin{aligned}
v_{an} &= \hat{V}_m sin(\omega t), \quad v_{bn} = \hat{V}_m sin(\omega t - \frac{2\pi}{3}), \quad v_{cn} = \hat{V}_m sin(\omega t - \frac{4\pi}{3}) \\
V_{pq} &= dI_{ab}v_{ab} + dI_{ac}v_{ac} + 0dI_o \\
&= \frac{3}{2}m_i\hat{V}_m
\end{aligned}
\tag{2.2}
$$

This DC-link voltage V_{pq} acts as a source to the VSI.

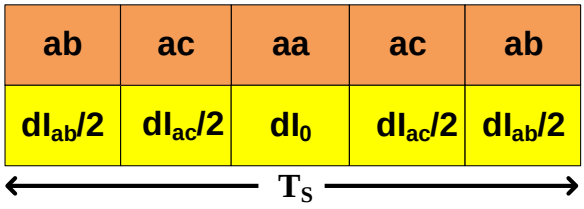


Figure 2.4: CSR switching sequence

2.3 SVM for VSI

The VSI circuit diagram is shown in Figure 2.5. It comprises six unidirectional switches ($g_1,\ g_2,\ g_3,\ g_4,\ g_5,\ g_6$) with three output terminals (A, B, C). SVM of the VSI involves six equal sectors, with each sector modeled by two active vectors [$V_1,\ V_2,\ V_3,\ V_4,\ V_5,\ V_6$] and zero vectors [$V_0,\ V_7$] as shown in Figure 2.6. The reference output voltage vector (V_{ref}) is constructed with the adjacent active and zero vectors. The reference vector voltage equation and corresponding active and zero vector duty ratios are given by equation (2.3). Here, d_{V1}, d_{V2} are the duty ratios of the two active vectors and m_v is

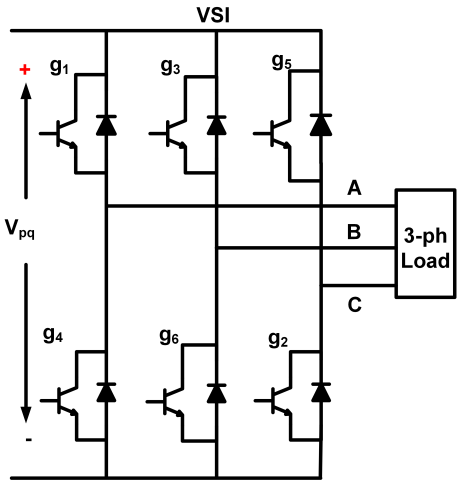


Figure 2.5: Voltage source inverter

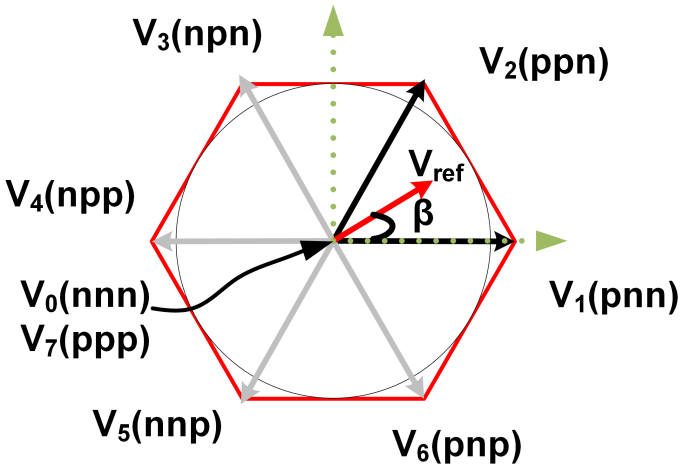


Figure 2.6: VSI space vector diagram

the VSI modulation index.

$$
\begin{aligned}
V_{ref}e^{j(\beta)} &= \frac{2}{3}[d_{V1}V_{pq} + d_{V2}V_{pq}e^{j(\pi/3)}] \\
d_{V1} &= \sqrt{3}m_v sin(\frac{\pi}{3} - \beta) \\
d_{V2} &= \sqrt{3}m_v sin(\beta) \\
d_{V0} &= 1 - d_{V1} - d_{V2} \\
m_v &= \frac{V_{ref}}{V_{pq}}
\end{aligned}
\tag{2.3}
$$

The switching pattern of the VSI is shown in Figure 2.7. The switching sequence starts with a zero vector. The switching sequence in one cycle (T_S) is $_0|nnn(V_0)$ - $pnn(V_1)$ - $ppnn(V_2)$ - $ppp(V_7)$ - $ppn(V_2)$ - $pnn(V_1)$ - $nnn(V_0)|_{T_S}$. The obtained output voltage of the VSI is

$$\hat{V}_o = \frac{m_v}{\sqrt{3}}\hat{V}_{pq} \tag{2.4}$$

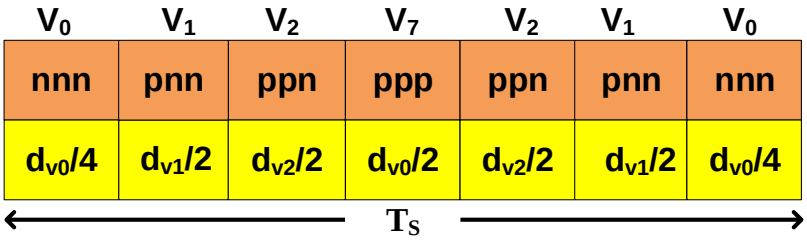


Figure 2.7: VSI switching sequence

After the successful implementation of SVM for both CSR and VSI, there should be coordination between both CSR and VSI switching states to achieve the USMC SVM technique.

2.4 SVM for USMC

USMC operates as a CSR to synthesize sinusoidal input currents and generates pulsed DC voltage at the DC-link and the load side converter is a conventional VSI that generates the output voltages. From Figure 2.1, The DC-link establishes a connection between the CSR and VSI. In order to achieve a balance between the input currents and the output voltages [82] within the same switching period, coordination between CSR

and VSI is essential due to no storage elements between CSR and VSI. Achieving this coordination involves overlaying CSR onto VSI or vice versa. There are two ways to do this coordination: one is placing the CSR switching state constant while changing the VSI switching states, called zero current switching sequence, and the other is keeping the VSI switching state constant and changing CSR switching states, called zero voltage switching sequence. Both sequences are explained below:

Zero current switching (ZCS):

Fig .2.8 shows the superimposition of Voltage vectors onto the Current vectors. Considering a situation when both current and voltage vectors are lying in sector 1, voltage vectors of V_0, V_1, V_2, V_7 from VSI space vectors (VSV) will occupy a place within the length of vectors I_{ab}, I_{ac} from CSR space vectors (CSV). Here, $I_{ab,pnn}$ represents a com-

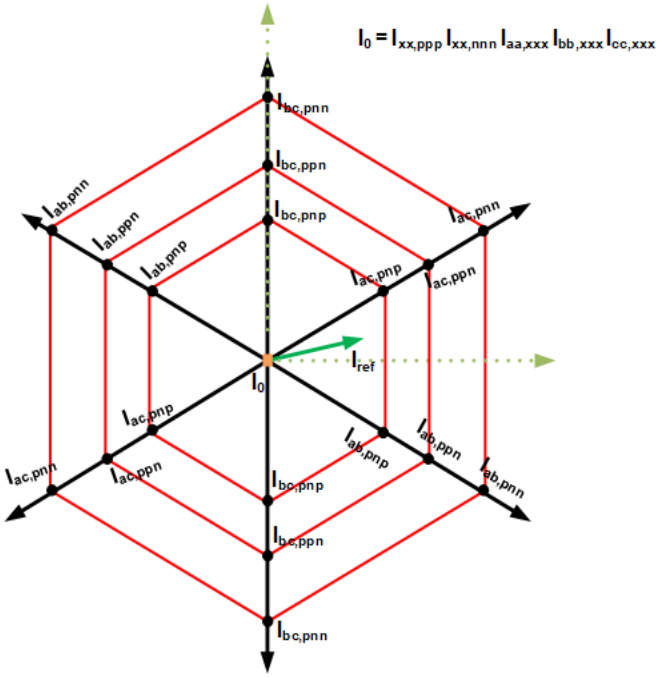


Figure 2.8: Zero current switching

bination of ab state in the rectifier with pnn state in the inverter. The dwell time of this combination is achieved by multiplying $dI_{ab} \times d_{V1} \leftrightharpoons ab \times pnn$. Similarly, remaining dwell timings are given in equation (2.5)

$$\begin{aligned} d_1 &= dI_{ab} \times d_{V1}, \quad d_2 = dI_{ab} \times d_{V2} \\ d_3 &= dI_{ac} \times d_{V2}, \quad d_4 = dI_{ac} \times d_{V1} \\ d_0 &= 1 - d_1 - d_2 - d_3 - d_4 \end{aligned} \tag{2.5}$$

Figure 2.9 shows the indirect matrix converter switching placements to achieve Zero current switching. In this, initially placing the input stage in the switching state (ab), while the output stage goes through the switching state sequence $(nnn) - (pnn) - (ppn) - (ppp)$. In this manner, the input current space vector along the (ab) direction remains fixed. Following this, the switching state of the input stage transitions to (ac). Consequently, only input current space vectors oriented in the (ab) direction are produced, while the output stage conveniently repeats the switching state sequence in reverse order: $(ppp) - (ppn) - (pnn) - (nnn)$. The resulting sequence of switching states can be expressed as:

$$_0|(ab)(nnn) - (ab)(pnn) - (ab)(ppn) - (ab)(ppp) - (ac)(ppp) - (ac)(ppn) - (ac)(pnn) - (ac)(nnn)|_{\frac{T_s}{2}} \quad (2.6)$$

The switching of the input stage occurs during the freewheeling state of the output stage in the described modulation scheme. This ensures that the change in the input stage switching state coincides with the point when the DC-link current is zero, preventing any switching losses in the input stage.

Zero voltage switching (ZVS):

Similarly, another combination is zero voltage switching, which can be obtained by superimposing Current vectors onto Voltage vectors, as shown in Figure 2.10. The corresponding switching state placement is shown in Figure 2.11. The switching sequence starts with (pnn) at the output stage, and the input stage cycles through the switching state sequence $(ab) - (ac) - (aa)$ while maintaining a constant switching state in the output stage. This results in forming a current space vector triangle at the input. Following this, the switching state of the output stage is altered from (pnn) to (ppn). The input stage then cycles through the switching state sequence in reverse order, following

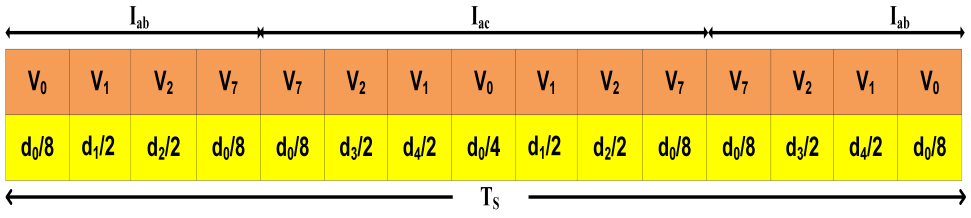


Figure 2.9: ZCS switching placement

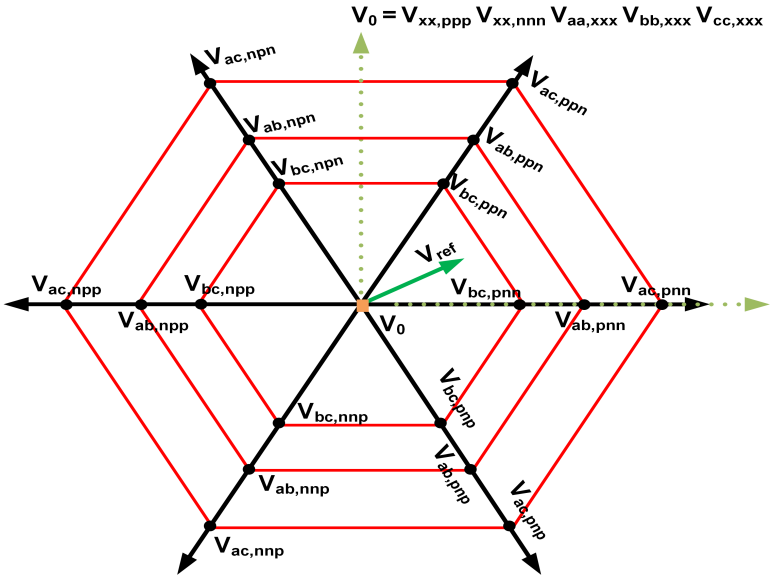


Figure 2.10: Zero voltage switching

$(aa) - (ac) - (ab)$. The resulting sequence of switching states can be expressed as:

$$_0|(pnn)(ab) - (pnn)(ac) - (pnn)(aa) - (ppn)(aa) - (ppn)(ac) - (ppn)(ab)|_{\frac{T_s}{2}} \quad (2.7)$$

In ZVS modulation scheme, the transition of the switching state in the input stage is required to take place at the rated DC-link current. Hence, the USMC needs to employ a relatively complex multi-step commutation strategy. So, the conventional

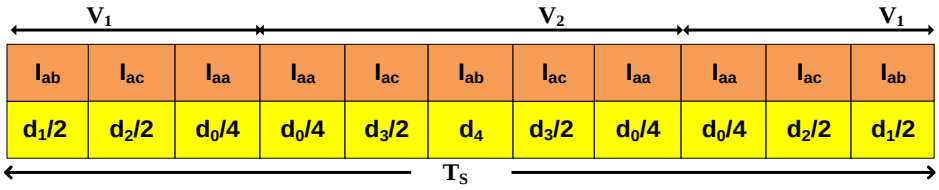


Figure 2.11: ZVS switching placement

SVM for matrix converters uses zero current switching modulation. After applying this zero current switching modulation to USMC, can get the desired output voltage and frequency. From equations (2.2) and (2.4), the overall output voltage of the USMC is

$$\hat{V}_o = \frac{\sqrt{3}}{2} m \hat{V}_m \quad (2.8)$$

Even though the SVM method is more popular than other modulation techniques, this method still has the following limitations:

- Limited voltage gain, the maximum voltage gain obtained by the SVM method is 0.866.
- Limited load phase angle operating range ($\pm\frac{\pi}{6}$).
- Produces more common mode voltage results in increased bearing currents and damages the system.

2.5 CMV in USMC

Common mode voltages in USMC typically refer to unwanted voltages that appear equally with respect to the ground at the output of the converter. These voltages are common in power electronics circuits. The types of common-mode voltages in inverters can be categorized based on their sources and characteristics:

- **High switching ($\frac{dV}{dt}$) CMV**: This type is generated due to the high-speed switching actions of the converter's power electronic devices (such as IGBTs or MOSFETs).
- **Parasitic CMV**: Generated by parasitic capacitances and inductances in the converter circuit and the associated wiring.
- **DC CMV**: This is a steady-state voltage that can appear due to imbalances in the converter's circuitry or the power supply.
- **AC CMV**: This type of voltage oscillates with a certain frequency and can be induced by the converter's AC output.

This thesis focuses on high switching ($\frac{dV}{dt}$) CMV or CMV. Common mode voltage (v_{CMV}) of the USMC is defined as the voltage potential difference between three-phase load neutral (N) to three-phase input neutral (n) as shown in Figure 2.12. This CMV plays a critical role in applications such as AC motor drive, which is an integral compact in wind turbine applications. The CMV results in

1) Increases in voltage across bearings lead to bearing current in the Permanent Magnet Synchronous Motor (PMSM). This current flows through the PMSM frame to the ground, damaging the system. It has been demonstrated to cause bearing system deterioration, accounting for over 50% of motor failures [53–55].

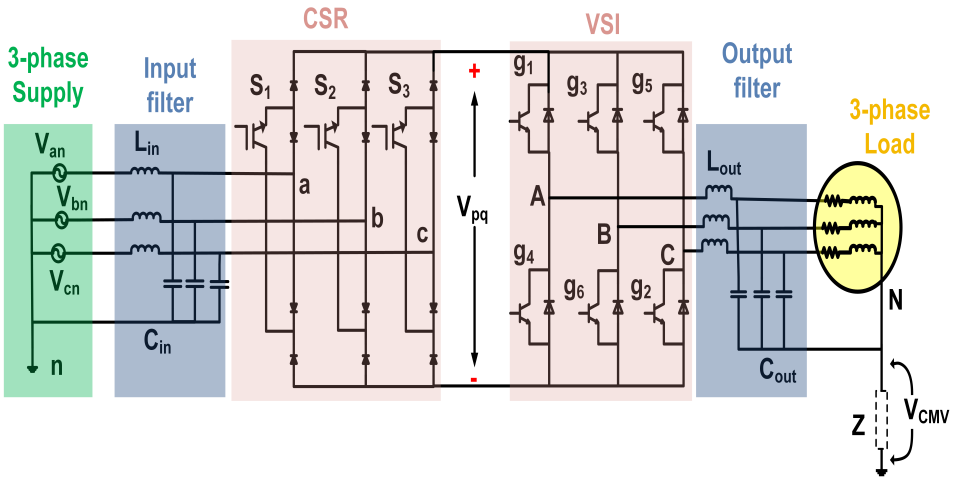


Figure 2.12: Common mode voltage of the USMC

2) High frequency bearing current creates Electromagnetic interference (EMI) noise, which disturbs the operation of the relay and other electronic devices in the environment [53, 56–58]. These problems have increased due to high frequency pulse width modulation (PWM) techniques like Sinusoidal Pulse Width Modulation (SPWM) and SVM techniques.

Hence, minimizing the CMV to improve the reliability of the drive system is necessary. To reduce the CMV, it is essential to know the behaviour of the CMV in each sector.

2.5.1 Calculation of CMV in USMC

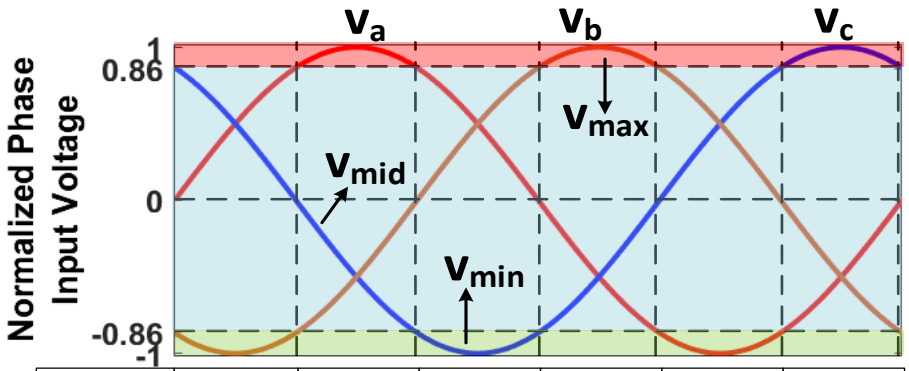
The conventional USMC is connected to the three-phase balanced load as shown in Figure 2.12. The output voltage equations are written as

$$\begin{aligned} v_{An} &= v_{AN} + v_{Nn} \\ v_{Bn} &= v_{BN} + v_{Nn} \\ v_{Cn} &= v_{CN} + v_{Nn} \\ v_{Nn} &= \frac{v_{An} + v_{Bn} + v_{Cn} - v_{AN} - v_{BN} - v_{CN}}{3} \end{aligned} \tag{2.9}$$

In the above equation (2.9), V_{Nn} is the CMV, for the balanced load $v_{AN}+v_{BN}+v_{CN} = 0$. So, the relation between CMV and instantaneous output voltages (v_{An}, v_{Bn}, v_{Cn}) is provided in equation (2.10).

$$v_{CMV} = \frac{1}{3}[v_{An} + v_{Bn} + v_{Cn}] \tag{2.10}$$

The magnitude of the instantaneous output voltages depends on the SVM CSR and VSI switching states. For instance, both CSR and VSI reference vectors are in sector 1, then the applied active vectors in CSR are I_{ab}, I_{ac} and applied vectors in VSI are V_0,



CSR sector	6	1	2	3	4	5
Clamp	S_2	S_1	S_3	S_2	S_1	S_3
Switching	S_1, S_3	S_2, S_3	S_1, S_2	S_1, S_3	S_2, S_3	S_1, S_2

Figure 2.13: Common mode voltage of the USMC

V_1, V_2, and V_7. For (ab)(nnn) state, all three load phases are connected to negative DC-link. From Figure 2.13, the voltage of phase-a varies from $\frac{\sqrt{3}}{2}\hat{V}_m$ to $\hat{V}_m$ and the voltages of phase-b and phase-c varies from $-\frac{\sqrt{3}}{2}\hat{V}_m$ to 0. Here $\hat{V}_m$ is the peak magnitude of the input. So from equation (2.10), the maximum CMV during this state is $\frac{\sqrt{3}}{2}\hat{V}_m$. Similarly, for the (ab)(ppp) state, the maximum CMV is $\hat{V}_m$. As a result, the peak CMV magnitude relies on the selection of the current, voltage space vectors, and input supply voltage, shown in Table 2.1. When zero vectors are applied, peak CMV attains its maximum value, that is, $(\hat{V}_m)$.

Table 2.1: Peak magnitude of CMV in the conventional SVM

VSI vector	**Peak CMV in CSR sector(1,3,5)**	**Peak CMV in CSR sector(2,4,6)**
V_0	$\frac{\sqrt{3}}{2}\ \hat{V}_m$	$-\hat{V}_m$
V_7	$\hat{V}_m$	$-\frac{\sqrt{3}}{2}\ \hat{V}_m$
$[V_1, V_2, V_3, V_4, V_5, V_6]$	$\frac{1}{\sqrt{3}}\ \hat{V}_m$	$-\frac{1}{\sqrt{3}}\ \hat{V}_m$

In 2012, Tuyen D. Nguyen et al. proposed two methods [83] to reduce the peak CMV by modifying the conventional SVM. In the first method, the voltage reference vector is synthesized by four active vectors instead of active and zero vector combinations. Two are the same as the conventional method, and the remaining two active vectors are neighbours (V_3, V_6), as shown in Figure 2.6. The switching sequence of this method for sector 1 is shown in Figure 2.14; inverter stage space vectors are arranged as double sides. This method reduces the peak CMV to 42%. The main limitations of this method are:

- This method lost the capability of soft switching at CSR stage
- A constrained modulation index range results in a restricted operational range for controlling the output voltage.

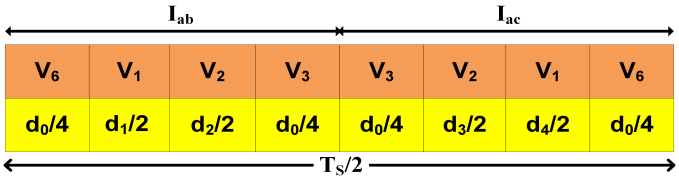


Figure 2.14: Switching strategy of the method I in Ref. [83]

In the second method of reference [83], medium and lowest input line voltages are used to set up the DC-link voltage produced by the CSR stage. In contrast, the inverter stage is the same as the conventional method (two active and two zero vectors), as shown in Figure 2.15. With this arrangement, CMV is reduced to $\frac{1}{\sqrt{3}}V_m$ but at the same time, the maximum available DC-link voltage is limited to $1.5V_m$, and the average voltage is reduced to restrict the voltage transfer ratio to 0.5. The main limitation of this method is the limited voltage transfer ratio. The maximum voltage transfer ratio by using this method is 0.5. In [68], Padhee et al. used three active vectors on the

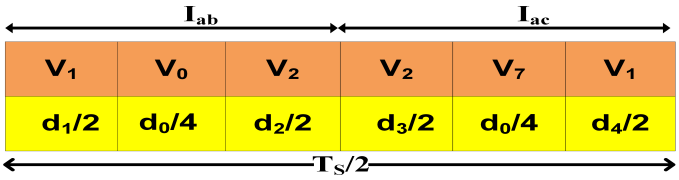


Figure 2.15: Switching strategy of the method II in Ref. [83]

rectifier side to develop DC-link voltage. To illustrate this method, consider sector 1

operation, in which I_{ab}, I_{ac}, I_{bc} active vectors are used to construct DC-link voltage, as shown in Figure 2.6. I_{ab}, I_{ac} vectors are having high and medium values whereas I_{bc} vector has the smallest value among them. In this method, DC-link voltage varies from $1.5\hat{V}_m$ to 0. So, the ripple in DC-link voltage is more in this method. The inverter stage reference vector synthesized by only active vectors. Hence, VSI modulation is kept at maximum ($m_v = 1$), and CSR modulation (m_i) controls the USMC gain. switching pattern of this method is presented in Figure 2.16 and the reduced peak CMV is ($\frac{1}{\sqrt{3}}V_m$). The main limitations of this method are:

- More ripple in the DC-link voltage.
- A limited modulation index range results in a restricted operational range for the output voltage.
- Loosing the soft switching capability at CSR stage.

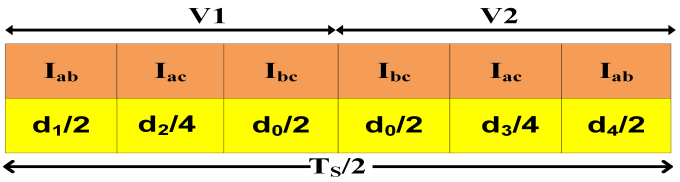


Figure 2.16: Switching strategy of the Ref. [68]

In 2014, Tuyen D. Nguyen et al. developed another switching strategy [69] to limit the peak CMV. In this method, three active vectors are used for the VSI stage and two active vectors are used for the CSR. The switching pattern of this method is presented in Figure 2.17, and the reduced peak CMV is ($\frac{1}{\sqrt{3}}V_m$). This method also has the same limitations as the method 1 in ref. [83]. R Vargas et al. developed a new

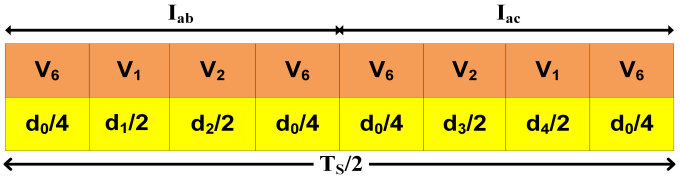


Figure 2.17: Switching strategy of the Ref. [69]

solution to mitigate the CMV [84]. According to this method, the Quality Function (Q.F) [84, 85] given in equation (2.11) is defined as the sum of the predicted load

current, the predicted source current and the predicted common mode voltage. Here 'x' manages the relation between source and load instantaneous reactive power and 'y' is the weighting factor related to common mode voltage. The predicted common mode voltage can be known by using equation (2.10), which decreases by increasing the weighting factor 'y'. Later, this function is modified as equation (2.12) and renamed as Cost Function (C.F) [86]. Here, superscript '$*$' indicates the reference values, 'w' indicates the predicted values and 'y' is the weighting factor related to CMV.

$$Q.F = |I^{*}_{out,\alpha} - I^{w}_{out,\alpha}| + |I^{*}_{out,\beta} - I^{w}_{out,\beta}| + x|Q^{w}| + y|V_{cmv}| \tag{2.11}$$

$$C.F = \Delta I_{out}(k+1) + \gamma_i \Delta I_{in}(k+1)\gamma_v |V_{cmv}(k+1)|^2 \tag{2.12}$$

Limitations of this method are:

- The computational complexity of the predictive control algorithm requires higher processing power compared to traditional SVM.
- Higher sampling frequencies can be required to implement this method.

Mei Su et al. modified the CSR control strategy and introduced the new zero vectors [67] to achieve the CMV reduction. According to this method, each sector has its own zero vectors, given in Table 2.2. The DC-link voltage is constructed by two active

Table 2.2: Zero vectors of [67]

Sector	$[S_1, S_2, S_3, S_4, S_5, S_6]$	$[G_1, G_3, G_5, G_4, G_6, G_2]$
Sector 1	[0,0,0,0,0,0]	[1,0,0,0,1,1]
Sector 2	[0,0,0,0,0,0]	[1,1,0,0,0,1]
Sector 3	[0,0,0,0,0,0]	[0,1,0,1,0,1]
Sector 4	[0,0,0,0,0,0]	[0,1,1,1,0,0]
Sector 5	[0,0,0,0,0,0]	[0,0,1,1,1,0]
Sector 6	[0,0,0,0,0,0]	[1,0,1,0,1,0]

vectors and a newly defined zero vector for the CSR stage, while for VSI, only two active vectors are used. The switching pattern for this method is shown in Figure 2.18. DC-link voltage varies between maximum value ($\sqrt{3}\hat{V}_m$) to minimum value (0). Limitations of this method are:

- This switching strategy is inconvenient under transient conditions and unsuitable for high gain impedance matrix converters.
- More ripple in the DC-link voltage.
- There is no soft switching at the CSR stage.

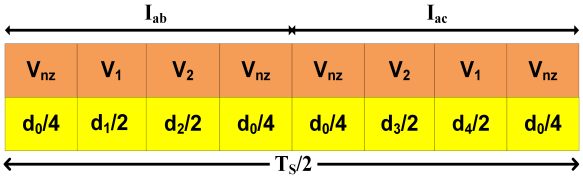


Figure 2.18: Sector 1 switching pattern for [67]

A different control strategy for the CSR stage to produce DC-link voltage is mentioned in [87]. This operation uses three active vectors in the CSR stage to get variable DC-link voltage. The suggested SVM employs three positive line-to-line voltages per sector to generate the DC-link voltage. This approach inherently eliminates zero voltage vectors, reducing peak common-mode voltage (CMV). Adjustable DC voltage is given by equation (2.13), where d_I and d_{II} are the controllable duty ratios. The switching pattern of this method is similar to method II of the [68], as shown in Figure 2.19. The limited operating range of this method leads to a limited control range.

$$\begin{aligned} V_{dc_{ref}} &= d_I V_{pq1} + d_{II} V_{pq2} \\ d_I + d_{II} &= 1 \end{aligned} \tag{2.13}$$

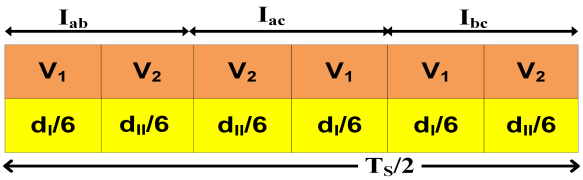


Figure 2.19: Sector 1 switching pattern for [87]

Most of the above methods reduce peak CMV by utilizing only active vectors in both the input and output stages of the USMC, resulting in a limited modulation index range and loss of zero current switching at the CSR side. Some methods reduce CMV by switching off CSR switches; this control strategy is still inconvenient under transient

conditions and unsuitable for high-gain impedance matrix converters. Some approaches mandate a microcontroller with excellent processing capabilities and higher sampling frequencies. So, to address these drawbacks in the coming chapter, defined new zero vectors with the help of three additional auxiliary shoot-through (AST) switches on the VSI side. This method avoids hard switching at CSR, reduces CMV, and improves the modulation index range as the conventional method.