Chapter 5

Generalized Switched Inductor Cell Multilevel Converter

5.1 Introduction

Traditionally, two level impedance source converters are suitable for high gain DC to AC conversion. However, two level impedance source converter suffers from high voltage THD, high dv/dt, high voltage stress across the switches. Multilevel inverter(MLI) has potential to address these issues [120]. MLI offers better EMI compatibility as compared to traditional VSI, lower THD, reduced filter size, low dv/dt and low voltage stress across the switch [121]. Nevertheless, these features incorporated at the cost of increased switches count. Broadly, MLI is of three types: Flying capacitor(FC) [122], Neutral point clamped(NPC) [123] and cascaded multilevel inverter(CMLI) [124]. Both FC and NPC inverter uses the capacitor and diode to clamp the undesired signals. This arrangement increases the number of switches and passive components. Also, the capacitor used must be balanced to avoid circulating current. However, in practical cases, uneven degradation of capacitor effects voltage balancing. To get rid of these problems, CMLIs are introduced. The CMLI uses the half bridge inverter(HBI) for converting DC to AC. CMLI offers the advantage of balanced load across the device, least number of switches and constant switching frequency of the device [125]. Furthermore, the extra levels can be produced at the output without introducing much complexity into the circuit. However, CMLI uses the increased number of isolated voltage source. This sometimes may lead to unbalance in three phase output if voltage is not shared equally among the three phases.

There are other MLI topologies which have different arrangement of switches for DC-AC conversion depending on desired levels. These include MLIs having either single DC source or multi DC sources. Single DC source MLI has inherent capability to buck the voltage since the maximum level of output voltage is equal to input voltage. On the other hand, multiple DC source MLI steps up the voltage according to the number of sources. These converters also imbibe the feature of fault tolerant capability. Asymmetric MLI are also introduced to produce more level without adding extra element in the circuit. This arrangement is only possible when more than one source is present in the circuit.

After having so much attention in terms of levels, switches count and DC voltage source for MLI, there are still problems in existing MLI. These MLI are only capable to produce step down voltage in case of single source or sum of total voltage source when multiple source concept is used. To overcome this problem, Z-source concept is an attractive solution [126]. Initially, it was developed to mitigate the problem of boosting in VSI. However, with high voltage demand along with better inverter characteristics, Z-source converter are cascaded with CMLI and NPC [127].

NPC was integrated with Z-source firstly in 2007. This configuration uses two Z-source network for boosting the voltage. To reduce the passive elements count, Z-source NPC is modified. Z-source concept is further integrated with CMLIs. Quasi Z-source is integrated with CMLIs for photovoltaic application because of its continuous nature of input current. Design criterion is developed from wide band gap power device point of view. Several control methods are developed to optimize the performance of the Z-source CMLI. To provide the isolation between the output and grid, a front end isolated q-ZSI based CMLI is proposed. With much improvement in NPC and CMLI, they still have the problems of high switch count and high number of voltage source in NPC and CMLI respectively.

Recently a modular multilevel converter(MMC) is proposed which uses the reduced component count with same number of levels produced at the output [128]. However, voltage gain is restricted. To improve the gain of the inverter, this work presents a generalized switched inductor approach. The modified inverter is named as switched inductor multilevel inverter(SL-MLI). The performance of SL-MLI is compared in case of full shoot through and combination of upper shoot through and lower shoot through. In addition to continuous current mode(CCM) of inductor current, discontinues current

mode(DCM) of the inductor current is also analyzed. It is proved that under DCM, the converter exhibit the higher gain.

5.2 Revisiting Z-Source converter and motivation

The concept of Z-source inverter was introduced to mitigate the problem of EMI and inherent buck capability of traditional voltage source inverter(VSI). The interesting feature of Z-source converter is to provide boosting in single stage [129]. For buck boost operation, the control of Z-source inverter utilizes the zero pulses which are forbidden in traditional VSI control. During zero states of the traditional VSI, shoot through pulses are generated and sandwiched between the active states of VSI. The shoot through pulses to inverter can be applied in 7 different ways depending on the number of legs used. In VSI only eight states are present during one switching period while due to shoot through insertion, Z-source converter consists 15 states. These states are combined effect of 8 states of VSI and 7 states due to shoot through pulses. Different Z-source topology had been reported in the literature. However, in most topology, the inverter used was either two level conventional inverter or neutral point clamped inverter(NPC). The large filter requirement in conventional inverter to produce sinusoidal output is a serious concern. The size of filter however reduced in NPC at the cost of extra switches and degraded reliability. These concern motivated us to implement Z-source network in most appropriate configuration of multilevel inverter.

5.3 Topology and operation of proposed converter

5.3.1 Topology introduction

For integration of Z-source concept in MMC, switched inductor topology is considered. This topology is named as L-Z source. For same gain, L-Z source inverter uses reduced number of passive elements as compared to conventional Z-source inverter. So, better reliability and compactness are its attractive features. However, in L-Z source inverter, a snubber circuit is required to clamp electromagnetic noise created due to switching of inductance between the load and source. Although a resistance and capacitor in series serve as snubber but this incurs losses in the circuit. To overcome this an active snubber

is proposed in this chapter. In an active snubber a capacitor in series with a MOSFET is connected across the inverter. The proposed topology with generalized n-switched inductor cells and snubber circuit is presented in Fig-5.1, which is named as switched inductor multilevel converter(SL-MLI).

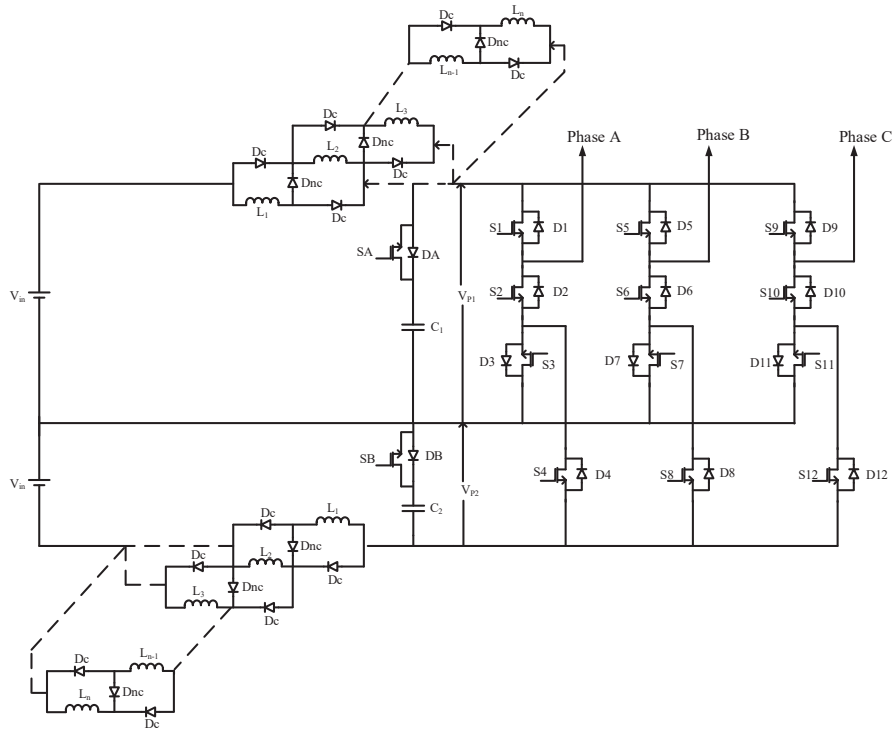


Figure 5.1: Proposed Z-source multilevel inverter

5.3.2 Operation

The operation of SL-MLI consists three states: full shoot through state(FST), combination of upper shoot through state(UST) and lower shoot through state(LST) and active state.

Full shoot through state

During FST, the ST is inserted in all the switches of the same leg. The diode D_c is forward biased and D_{nc} is reversed biased. The inductor slope is positive and charges through the MLI switches as shown in Fig-5.2. However, as the output voltage is zero during ST, FST produces distorted output.

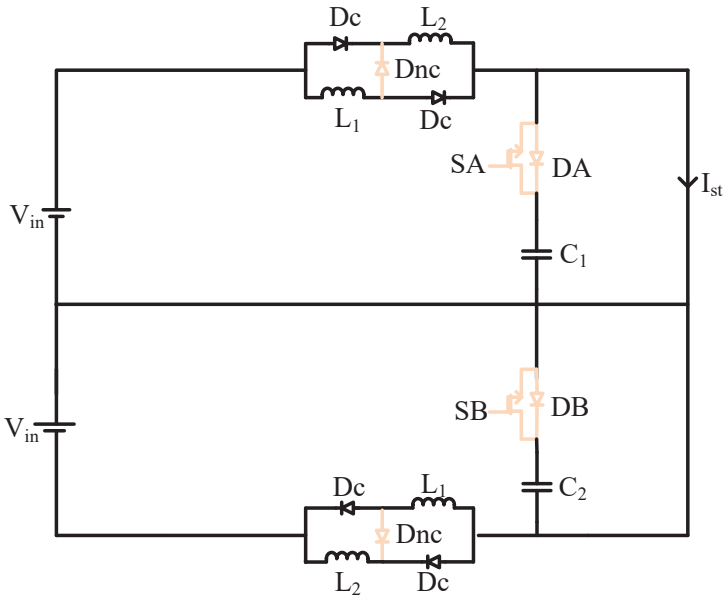


Figure 5.2: Full shoot though state of SL-MLI

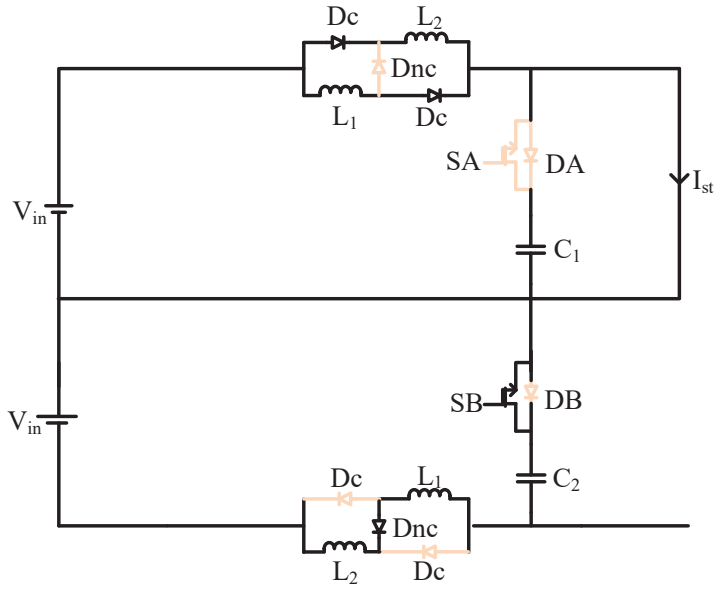


Figure 5.3: Upper shoot through state of SL-MLI

Upper shoot through state

During UST, ST is achieved by the switches of upper half of the SL-MLI without disturbing lower half. The switches of one of the legs are turned ON simultaneously as shown in Fig-5.3. As soon as the ST is inserted, both the diodes(D_c) are forward biased while D_{nc} is reverse biased in switched inductor of upper half. The inductors comes in parallel and charged through the input voltage. During this state, lower half inductor arrangement kept on supplying the power to the load.

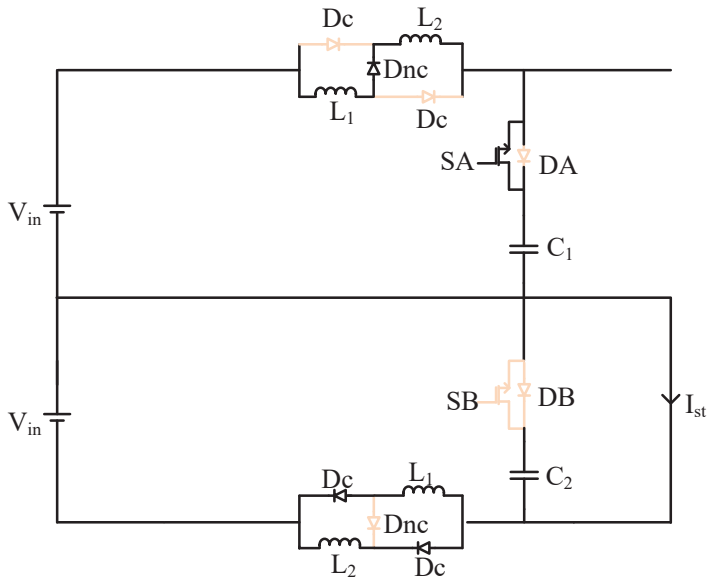


Figure 5.4: Lower shoot through state of SL-MLI

Lower shoot through state

Lower ST state is brought into the circuit by turning the lower half of switches as shown in Fig-5.4. Similar to UST, the switches of one of the legs are turned ON simultaneously from lower half. Both the D_c present in the switched inductor of lower half are turned ON and D_{nc} is reverse biased. The inductors slope is positive during ST and charged through the input voltage in parallel. In this state, upper half of inductor arrangement kept supplying power to the load.

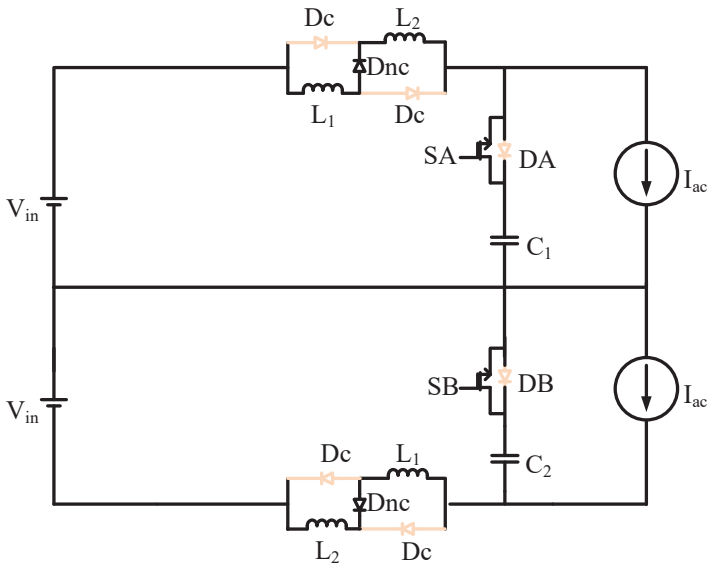


Figure 5.5: Active state of SL-MLI

Active state

The active state of SL-MLI, for FST or combined effect of UST and LST, is same. During this state, the ST is removed and MLI is returned to its normal switching as indicated in Table-5.2. Three phase load is connected to the supply voltage through switched inductors as shown in Fig-5.5. To felicitate the discharging, the inductors reverse their polarity. Thus the diode D_c are reverse biased and D_{nc} becomes forward biased. Both the inductors are connected in series and discharges through the load.

Table 5.1: Switching state under shoot through

	FST	**UST**	**LST**
Leg 1	S_1, S_2, D_3	S_3,S_4	S_1,S_2,D_3,S_4
Leg 2	S_5, S_6, D_7	S_7,S_8	S_5,S_6,D_7,S_8
Leg 3	S_9, S_{10}, D_{11}	S_{11},S_{12}	S_9,S_{10},D_{11},S_{12}

5.4 Steady state analysis of SL-MLI

In steady state analysis, the switches and diodes are assumed ideal. Analysis is presented in context to UST. Similar analysis can be extended for the FST and LST. Moreover, average value of V_{P1} is equal to V_{P2}.

Table 5.2: Switching state under active state

V_{AB}	V_P	$2V_P$	$2V_P$	$2V_P$	V_P	0
V_{BA}	$-2V_P$	$-2V_P$	$-V_P$	0	V_P	$2V_P$
V_{CA}	V_P	0	$-V_P$	$-2V_P$	$-2V_P$	$-2V_P$
Switches	S_2,S_3,S_6 S_8,S_9	S_1,S_6 S_8,S_9	S_1,S_6,S_8 S_{10},S_{11}	S_1,S_6 S_8 S_{10},S_{12}	S_1,S_6 S_7 S_{10},S_{12}	S_{10} S_{12}

5.4.1 Boosting under CCM

Steady state waveform for SL-MLI under CCM is shown in Fig-5.6(i). From Fig-5.2, during charging, voltage equation is

$$V_{in} - V_L = 0 \tag{5.1}$$

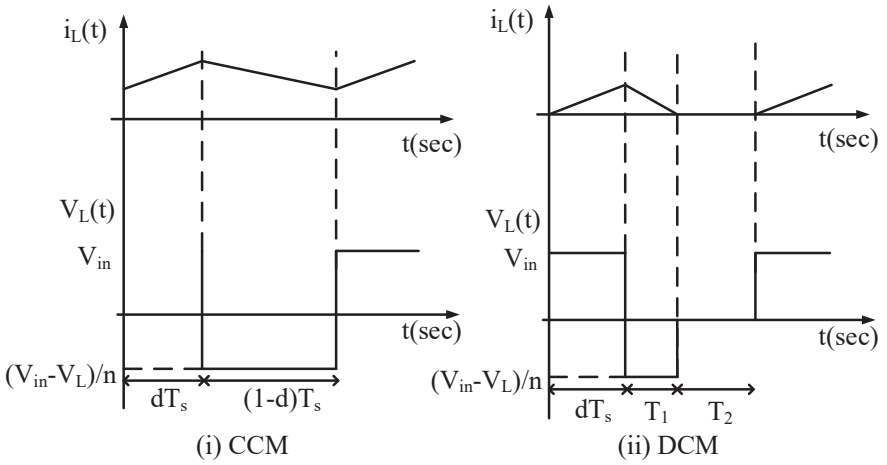


Figure 5.6: Steady State waveform for SL-MLI under CCM and DCM

During discharging

$$V_{in} - nV_L - V_{P1} = 0 \tag{5.2}$$

Averaging over a switching period, the voltage equation is written as

$$\int_0^{dT_s} V_L dt + \int_{dT_s}^{T_s} V_L dt = 0 \tag{5.3}$$

From this, the output voltage(V_{P1}) is given by

$$V_{P1} = \frac{1 + (n-1)\,d}{1-d} V_{in} \tag{5.4}$$

where n is number of switched inductors and V_P is DC link voltage across the MLI. From this, the voltage available at output will be equal to either V_P or $2V_P$ instead of V_{in} or $2V_{in}$. Gain of the proposed converter for different number of cells is plotted in Fig-5.7.

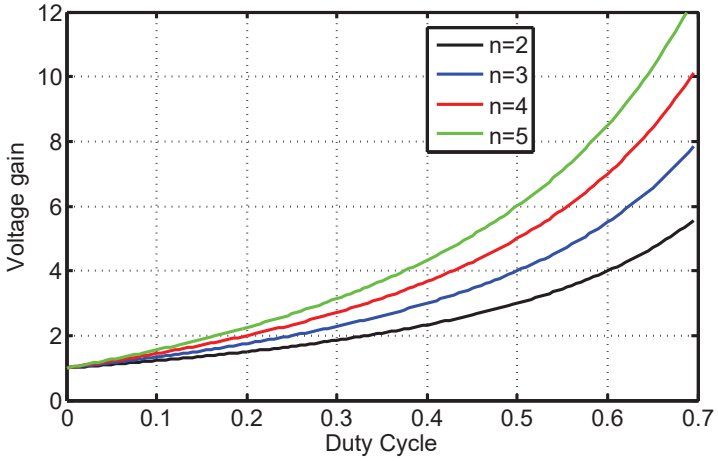


Figure 5.7: Gain of SL-MLI at different cell

5.4.2 Boosting under DCM

During charging and discharging of the inductors, the voltage across the inductor will be same as Equ-(5.1) and Equ-(5.2), respectively. When the converter enters into DCM, the current in the inductor will be zero as shown in Fig-5.6(ii). So the voltage across the inductor is

$$V_L = 0 \tag{5.5}$$

Averaging inductor voltages over a switching period, the voltage equation is

$$\begin{aligned} &\int_0^{dT_s} V_{L1}dt + \int_{dT_s}^{T_1+dT_s} V_{L2}dt + \int_{T_1+dT_s}^{T_s} V_{L3}dt = 0 \\ &ndT_sV_{in} + (1-d-d_2)\,T_s\,(V_{in} - V_{P1}) = 0 \end{aligned} \tag{5.6}$$

From Equ-(5.1), (5.2) and (5.6), the output voltage is given as

$$V_{P1} = \frac{1+(n-1)\,d-d_2}{1-d-d_2}V_{in} \tag{5.7}$$

where d_2 is duty cycle corresponds to DCM period. As the converters enters more into DCM, the gain of the proposed converter kept on increasing. Comparison between CCM and DCM is plotted in Fig-5.8. It can be seen that the DCM gain is higher than CCM for same n(for e.g. at d=0.5 and d_2=0.3, CCM gain =3 while DCM gain=6)

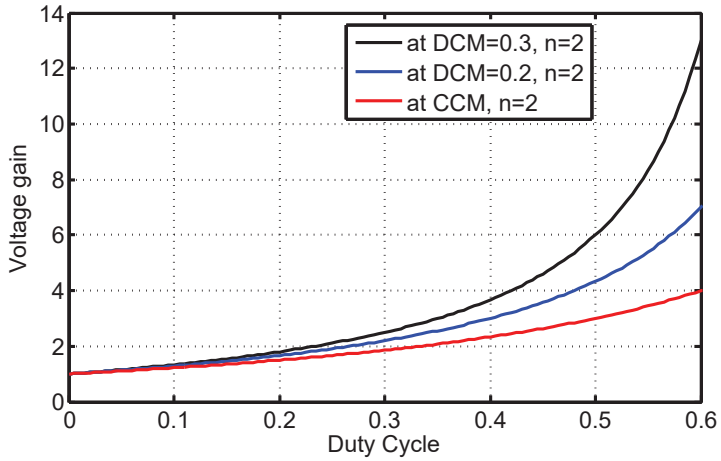


Figure 5.8: Comparison of gain for SL-MLI under CCM and DCM

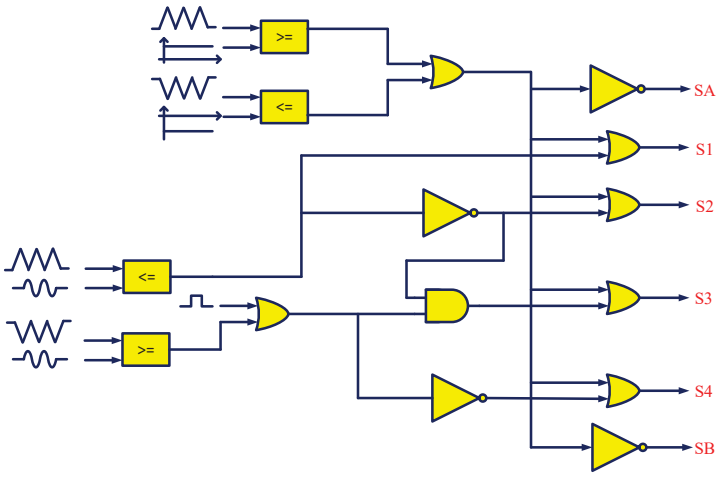


Figure 5.9: Pulse generation for SL-MLI under FST

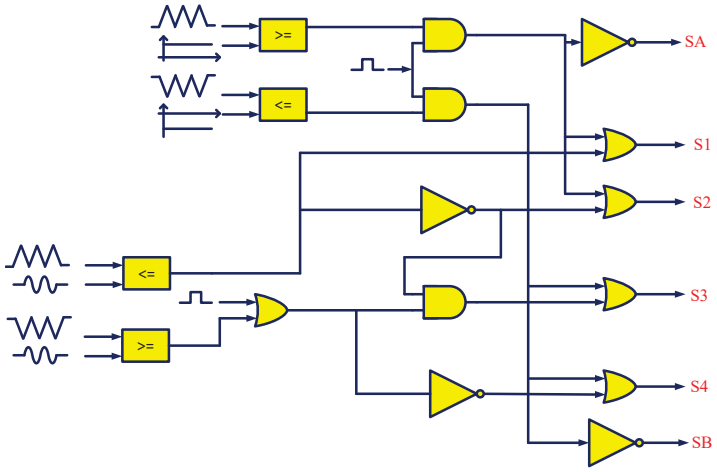


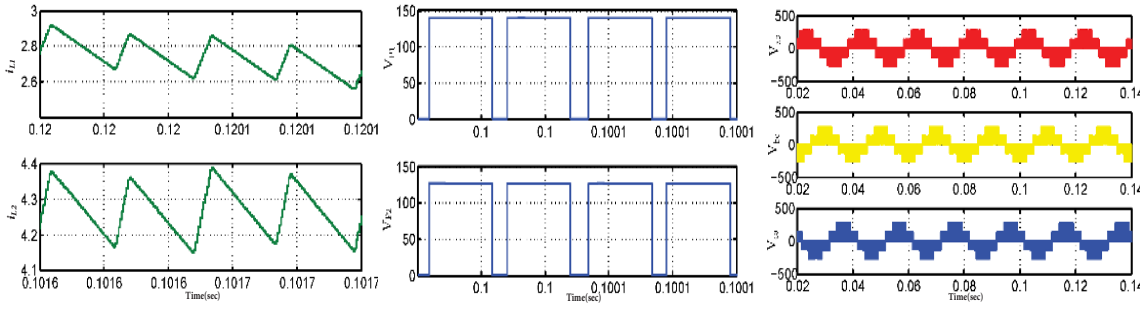
Figure 5.10: Pulse generation for SL-MLI under UST and LST

5.5 Control of proposed converter

Broadly two types of modulation techniques are available for MLI: 1) Low frequency modulation technique(LFM) and 2) High frequency modulation technique(HFM). There is always a trade-off among the selection of modulation techniques. LFM provides the lower switching loss while HFM is suitable for achieving better quality output. However, in case of Z-source MLI, the size of passive elements inversely depend on the switching frequency. So, for SL-MLI, high frequency is selected for modulation purpose at the cost of higher switching losses. The high frequency triangle carrier signal is compared with the three phase sinusoidal reference signals together with constant amplitudes to generate ST and active pulses for SL-MLI. The control logic for generating the controlling pulses for Phase A, for FST and UST/or LST is shown in Fig-5.9 and Fig-5.10, respectively.

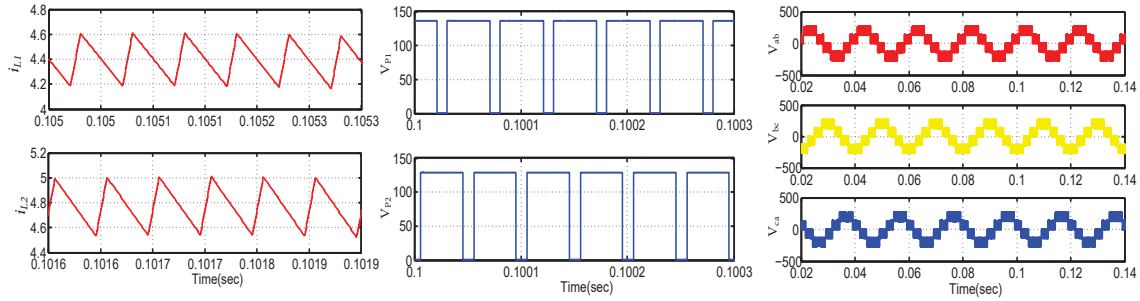
5.6 Simulation results

For validation of proposed idea, the model is designed and simulated on MATLAB/Simulink platform. The parameters for the SL-MLI are chosen as follows: L_1=L_2=2 mH, C_1=C_2=100 μF and V_{in}=90 V, d=0.2, m=0.8. The SL-MLI performance is evaluated under CCM and DCM. The CCM is considered at f_s=20 kHz, R_{ac}=30 Ω. In case I for CCM, FST is inserted in SL-MLI for boosting purpose. During FST, all the switches of same leg are short circuited. This makes the SL-MLI output voltage zero during FST. This is indicated by occurrence of zero DC link voltages in V_{P1} and V_{P2} simultaneously, as shown in Fig-5.11. This effect propagates to the MLI output, leading to zero output during FST. This introduces higher THD in the output voltage(typically 90 % without any filter).



(a) Inductor currents in CCM (b) DC link voltage in CCM (c) Line voltage in CCM

Figure 5.11: CCM: Operation under FST

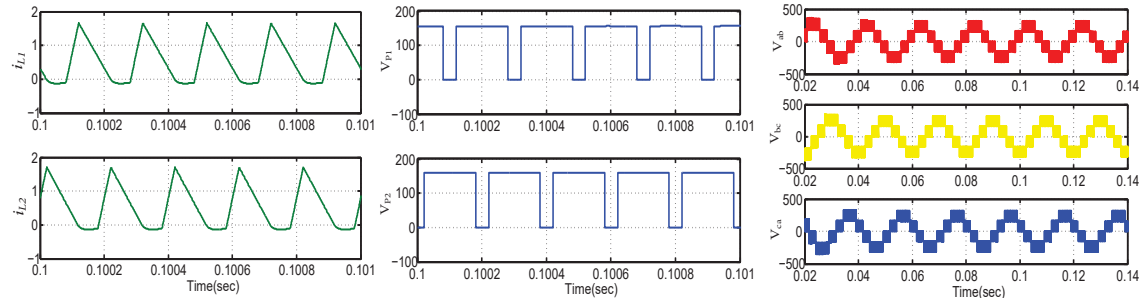


(a) Inductor currents in CCM (b) DC link voltage in CCM (c) Line voltage in CCM

Figure 5.12: CCM: Operation under UST and LST

For case II of CCM, UST and LST are given to upper leg and lower leg, respectively. The DC link voltages V_{P1} and V_{P2} never reaches zero simultaneously. Due to this, the voltage available at output of MLI does not become zero. The corresponding results are shown in Fig-5.12, the THD is improved to 42%(without any filter) which indicates huge improvement over FST.

For validation of DCM f_s=5 kHz and R_{ac}=200 Ω are taken. Only UST and LST are considered for DCM analysis as FST creates higher THD. The current reaches to zero before the start of next ST as shown in Fig-5.13a. During this period switches SA and SB are turned ON and capacitor supplies the power to the load. At same duty cycle and modulation index as in CCM, the gain of the converter is lifted from 135 V to 160 V, which indicates higher gain than the CCM as shown in Fig-5.13b. The DC link voltages V_{P1} and V_{P2} observe zero value at different instant, therefore THD in MLI output is almost same as CCM.



(a) Inductor currents in DCM (b) DC link voltage in DCM (c) Line voltage in DCM

Figure 5.13: DCM: Operation under UST and LST

5.7 Conclusion

This chapter presented the idea of including the switched inductor cell into the MLI. The gain of the converter may be increased to as high as demanded, by increasing the switched inductor cell, however, analysis in this paper is restricted to two inductors. Two control algorithm are proposed to produce the desired output and simulated. Combination of UST and LST is found better than the FST in terms of THD. Moreover, CCM and DCM analysis are reported to verify the higher gain in DCM.

In the preceding chapters, DC and AC converter are proposed for DC and AC load. However, the demand for DC and AC load can be fulfilled by a single hybrid converter. In the next chapter, boost derived hybrid converter(BDHC) will be analyzed in wider duty cycle variation. The solution will be proposed to overcome the problem of BDHC. Modified BDHC will be experimentally validated.