CHAPTER-1

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1.1 Thesis Abstract

With the evolution of artificial intelligence (AI) and the internet of things (IoT), the semiconductor industry needs to fulfill the demands of high-speed, large data processing, higher integration density, and power efficiency. The fundamental requirement for efficient data processing is the availability of large and high-speed memory systems, such as complementary metal-oxide-semiconductor (CMOS) based static random-access memory (SRAM). Conventional CMOS technology, enhanced through device scaling, has improved parameters such as dynamic power dissipation, chip area, and delay. In modern high-performance computing, especially in AI applications that can involve moving up to terabytes of data per second, most power consumption arises from data transmission between memory and processing units. This is due to the separation between memory and processing units in traditional Von Neumann architectures. Hence, this high-speed data processing requirement cannot be met by traditional CMOS-based memory solutions and conventional computing architectures. These limitations of CMOS have prompted the exploration of emerging technologies for memory and information processing.

The emerging non-volatile memory (NVM) technologies have enabled us to look toward some of the memory-centric computing paradigms beyond the Von Neumann architecture. One of the new paradigms is neuromorphic computing to mitigate the bottlenecks of the conventional Von Neumann architectures. NVMs are well-suited for neuromorphic computing, a paradigm inspired by the human brain, which aims to mimic the functionality of the human brain by integrating memory and computation into a unified framework. Neuromorphic systems leverage non-volatile devices to replicate synaptic functionalities, enabling highly energy-efficient and parallel processing for AI. Furthermore, emerging NVM

technologies, which offer energy efficient solutions and data retention under zero power supply, have shown strong potential to replace CMOS-based memory technologies. Amongst different NVM solutions, magnetic tunnel junction (MTJ) and ferroelectric field-effect transistor (FeFET) based NVM are focused in this work.

This dissertation focuses on the design and optimization of novel devices to enhance the performance of spin-transfer torque magneto-resistive random-access memories (STT-MRAM) and FeFET-based NVM at the bit-cell level. Firstly, we have developed a novel silicon-on-insulator (SOI) based junctionless-accumulation-mode (JAM) ferroelectric FinFET along with a proposed process flow at a 3-nm node. This device can be utilized as a synaptic element in neuromorphic computing applications. Secondly, we have also developed a 1T-1R-based memory cell featuring distinct read and write paths that utilize a memristive variant of the ferroelectric field effect transistor (MFeFET) for data storage. This memory cell architecture offers a unique feature, *i.e.*, a non-destructive read, better scalability, enhanced energy and area efficiency, and compatibility with one transistor, one memristor memory (1T-1M) technologies like STT-MRAM and resistive random-access memory (RRAM). Furthermore, we developed a 3-D asymmetric FinFET device structure at a 3nm technology node using process emulation in TCAD. Subsequently, we utilized this asymmetric FinFET design to achieve performance improvements in the STT-MRAM cell. All simulations presented in this thesis were performed using Sentaurus TCAD simulation tool. The work in this dissertation is structured into five chapters, as outlined below:

Chapter 1, provides an overview of neuromorphic computing with a brief background of various non-volatile memory technologies. Additionally, this chapter reviews the literature on device modeling and logic circuits co-design of non-volatile memory cells,

specifically the bit cell used in STT-MRAM and FeFET. We explore novel device architectures aimed at improving the performance of these memory cells. Furthermore, this chapter explores the fundamental physics, memory cell operation, and structural details of FeFET-based memory devices and MTJ. Finally, a brief summary is provided towards the formulation of the research problem statement for this thesis.

In ***Chapter 2,*** we present an SOI-based JAM ferroelectric FinFET designed to function as a synaptic weight device in neuromorphic computing architectures. The proposed device aims to enhance the non-volatile conductance range in the ON-state compared to existing junctionless and conventional ferroelectric FinFET devices. Our simulations demonstrate that the device offers linear conductance variation and symmetric switching characteristics, which are crucial for synaptic weight applications. Additionally, we have shown the experimental and process feasibility of this novel synaptic weight device through process emulation using Sentaurus TCAD. The proposed device offers zero process overhead and is fully compatible with the pristine FinFET process flow.

In ***Chapter 3,*** we introduce a 1T-1R memory cell that employs a memristive variant of the ferroelectric field effect transistor (MFeFET) for data storage. This 1T-1R memory architecture features distinct write and read paths, enabling non-destructive read operations and higher read currents at lower operating voltages. This novel memory architecture also offers lower read latency than STT-MRAM technologies.

After this chapter, in ***Chapter 4,*** we propose a novel asymmetric FinFET device in terms of drive-current from source to drain and drain to source. The proposed device is targeted towards increasing the efficiency of the STT-MRAM cell, which consists of an MTJ as the data storage element. The MTJ has an asymmetric bidirectional write current, which

can be exploited to achieve power savings by using an asymmetric select/access device in the STT-MRAM bit-cell. Further, the simulation and process emulation carried out in this chapter show that the proposed device provides better asymmetry and easy compatibility with the existing FinFET fabrication flow, respectively. The proposed device provides an additional benefit of lower gate capacitance over existing symmetric and asymmetric FinFET device architectures. Low gate capacitance provided by the proposed asymmetric device highlights the other vital improvement, which could result in lower write-line capacitance in STT-MRAM bit-cells.

Chapter 5 concludes the thesis by highlighting the key contributions and summarizing the research results achieved. Furthermore, it outlines the potential directions for future work based on the findings presented in the thesis.

1.2 Introduction

Today's semiconductor industry demands faster and more extensive data processing capabilities, higher integration density, and improved power efficiency. The rapid growth of artificial intelligence (AI) and the internet of things (IoT) has intensified the need for high-performance and energy-efficient computing systems. However, traditional CMOS-based computing architectures are encountering numerous obstacles, including the imminent end of Moore's Law and performance limitations imposed by the Von Neumann bottleneck. As fabrication costs continue to rise and physical scaling reaches its limits, further miniaturization of devices becomes increasingly difficult. Additionally, the energy inefficiencies and latency caused by data transfer between memory and processors severely hinder performance improvements, even if scaling continues. These challenges have compelled the semiconductor industry to explore innovative solutions built on novel devices and emerging computing

paradigms. Inspired by biological systems, neuromorphic computing has emerged as a promising approach, offering a framework for developing novel devices and optimizing computing systems for future applications.

1.2.1. The gradual slowdown of CMOS scaling and emerging innovations

In 1965, Gordon E. Moore introduced the well-known "Moore's Law," predicting that the number of transistors in a densely packed integrated circuit would double approximately every 18 months [1]. However, over the past decade, scaling has begun to slow down due to several technical and economic limitations. The primary reasons for this slowdown include transistor sizes shrinking to nanoscale dimensions, quantum effects, and increased leakage currents. Furthermore, the "dark silicon" phenomenon arises, where significant portions of a chip remain underutilized due to thermal constraints [2],[3]. Additionally, as transistor scaling approaches atomic levels, further miniaturization faces fundamental physical limits, creating barriers to further scaling.

To address these limitations," Beyond CMOS" technologies [4],[5] were introduced in the early 2000s. This approach explores advanced emerging devices and technologies that transcend the limitations of CMOS scaling [6]. Among these advanced technologies, devices like memristors[7], ferroelectric field-effect transistors (FeFETs) [8], and spintronic devices [9] have gained considerable attention due to their potential to meet the growing demands of future storage and computing systems.

1.2.2. The Von Neumann bottleneck

Another key challenge in traditional computing is the ''Von-Neumann Bottleneck''. In 1945, John Von Neumann introduced a computing architecture where the processing units and memory are physically separated, which is shown in **Figure 1.1** [10]. In this architecture,

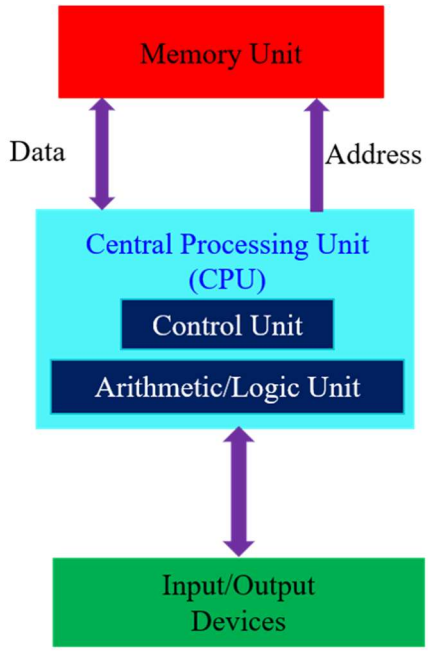

Figure 1.1 Von Neumann architecture

data must be constantly transferred back and forth between the memory and processor through a shared communication bus. However, this frequent data movement causes considerable energy consumption and delays, significantly impacting system efficiency for high-speed data-intensive applications. In modern high-performance applications, especially AI and the IoT, this data movement creates a bottleneck that severely limits the system performance.

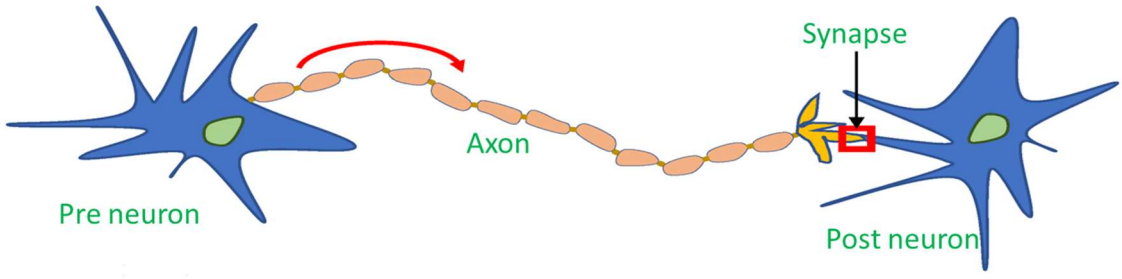

Figure 1.2 Connection of two neurons in the human brain.

1.2.3. Overview of neuromorphic computing

The term "neuromorphic" was first introduced in the late 1990s by Carver Mead, refers to a field inspired by the architecture and functionality of the human brain [11],[12]. It aimed to design electronic systems that emulate the brain's architecture and operation. Over the years, researchers have explored the concept of developing machines capable of thinking and learning in ways similar to humans. The human brain has billions of neurons that are connected to each other through trillions of synapses [13], allowing it to process and share information as shown in **Figure 1.2** [14].

Neuromorphic computing represents a transformative approach to computing inspired by the structure and function of the human brain. Unlike traditional Von Neumann architectures that separate processing units and memory, neuromorphic systems aim to emulate the interconnected network of neurons and synapses, as shown in **Figure 1.3**. These systems integrate memory and computation within a unified framework [15]. By processing data locally, neuromorphic systems minimize the need for energy-intensive data movement, addressing a major limitation of traditional architectures [16],[17]. This approach offers significant advantages in terms of energy efficiency, adaptability, and the ability to process large volumes of unstructured data, such as that encountered in AI and IoT applications.

The backbone of neuromorphic computing lies in its hardware implementations, particularly the choice of memory technology that can emulate synaptic behavior effectively. Non-volatile memory (NVM) technologies [18] have emerged as key candidates to fulfill these requirements due to their capability to retain data without power, fast switching speeds, scalability, and compatibility with advanced fabrication processes.

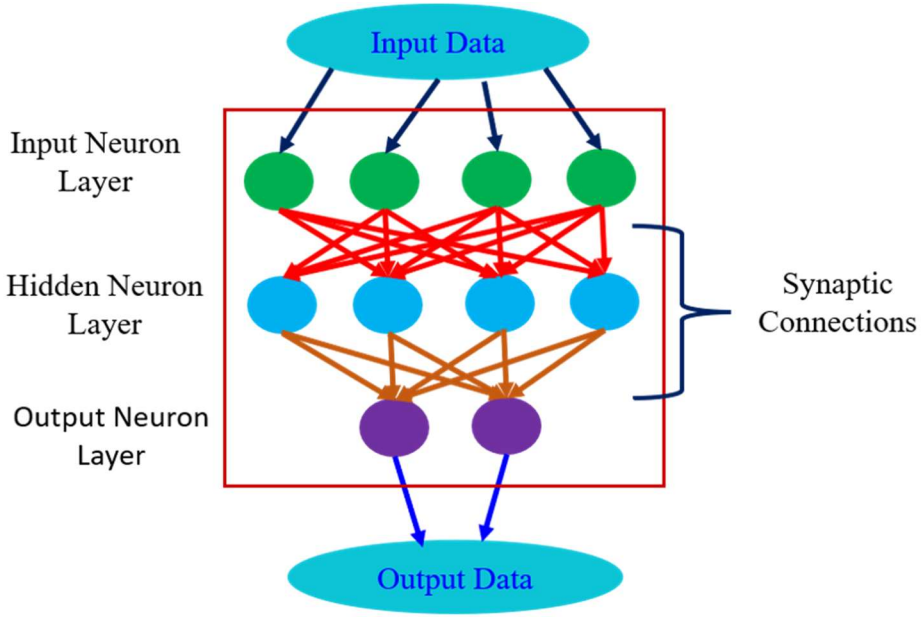

Figure 1.3 Neuromorphic architecture.

1.3 Role of Synaptic Devices in Neuromorphic Computing

Synaptic devices function as artificial synapses in neuromorphic systems [19]. It is the fundamental component in neuromorphic computing, as it emulates the behavior of biological synapses, which form the communication bridges between neurons in the human brain [20]. These devices are responsible for storing and modulating synaptic weights, enabling efficient learning and adaptive behavior in neuromorphic systems [21]. The ideal synaptic device should offer key features such as low power consumption, high endurance, non-volatility, history-dependent conductance, and scalability. These characteristics are crucial for replicating the dynamic behavior of synapses in a compact and energy-efficient manner.

Emerging NVM technologies, including resistive random-access-memory (RRAM) [22],[23], phase-change memory (PCM) [24], spin-transfer torque magneto-resistive random-access memories (STT-MRAM) [25], and FeFET [8],[26],[27], have demonstrated significant potential as synaptic devices for neuromorphic applications [28],[23].

1.3.1. Non-volatile memory as a synaptic device in neuromorphic computing

NVM technologies have been extensively researched as alternatives to conventional volatile memories like static random-access memory (SRAM) [29] and dynamic random-access memory (DRAM) [30]. Conventional memory technologies suffer from limitations such as high leakage power, scalability challenges, and endurance issues, making them less efficient for next-generation computing. Hence, emerging NVM technologies are designed to address the growing need for low power consumption, data retention without power, and high integration density, offering a potential solution to the limitations of traditional memory systems. The development of high-density NVMs is crucial for meeting the ever-increasing storage demands driven by big data, IoT, and AI applications.

Emerging memory devices, as illustrated in **Figure 1.4**, play a pivotal role in neuromorphic computing. These devices simulate synaptic functions by offering high memory density, low power operation, and the ability to process and store data simultaneously. Their non-volatility and multi-level resistance states make them ideal candidates for implementing brain-like computational processes [31]. As depicted in **Figure 1.4**, various emerging NVM technologies include ferroelectric random-access memory (FeRAM), FeFET, STT-MRAM, spin-orbit torque magneto-resistive random-access memory (SOT-MRAM) [32],[33], RRAM, and PCM. Among these, FeRAM, STT-MRAM, RRAM, and PCM are two-terminal devices, while FeFET is a three-terminal device. The two-terminal NVMs are preferred due to their smaller size and scalability, making them ideal for large memory arrays, such as those used in data storage or cache memory however, the inherent gate control facilitates three-terminal NVM provides precise control over write/read operations, reduced leakage currents and faster cell selection in memory array, making them suitable for applications requiring

high reliability, performance, and neuromorphic computing.

In the subsequent sections of this thesis, we will delve into the exploration of ferroelectric and magneto-resistive-based non-volatile memory technologies. Section 1.4 provides a comprehensive discussion of the fundamental aspects of ferroelectric materials, including their structure, properties, and underlying physics. Subsequently, Sections 1.5 and 1.6 focus on ferroelectric-based memory devices, detailing their operational principles and characteristics. The application of ferroelectric memory as a synaptic device is examined in Section 1.7, highlighting its potential for neuromorphic computing.

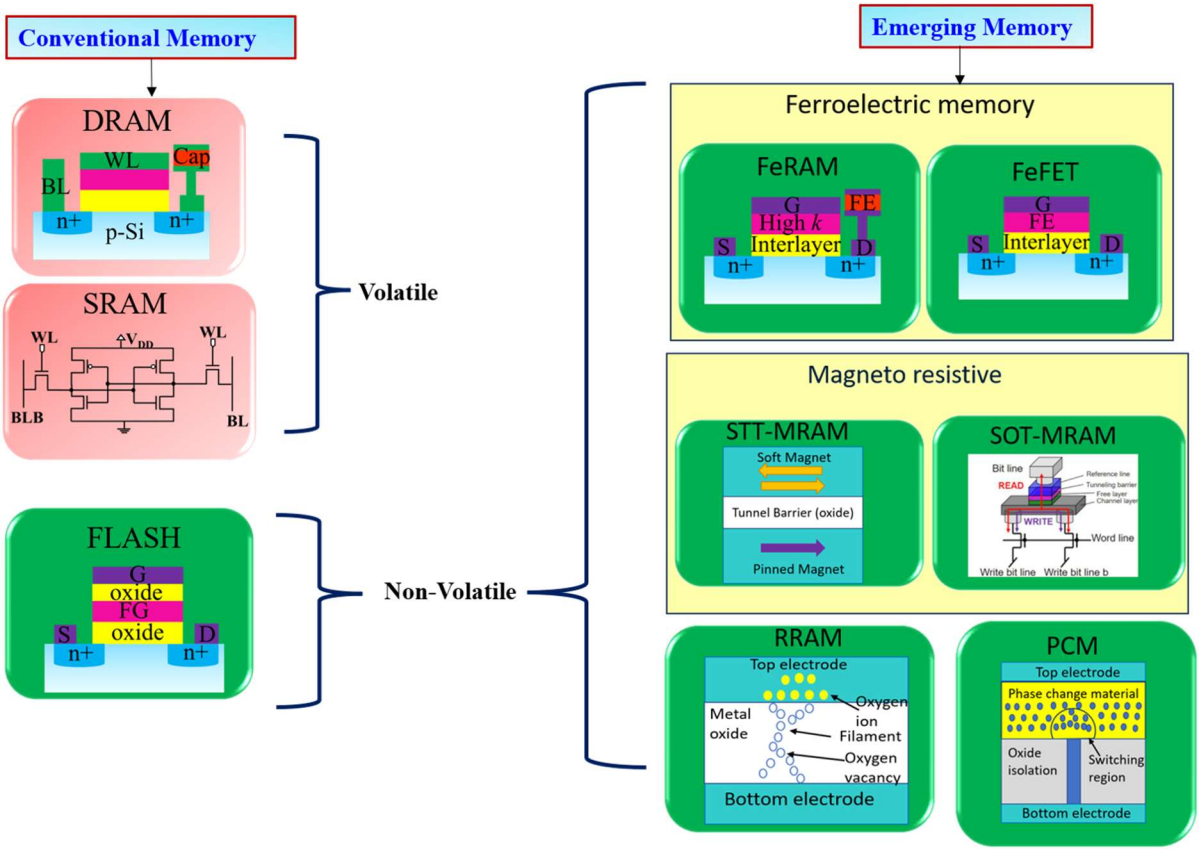

Figure 1.4 Classification of conventional and emerging memory devices/technology.

Section 1.8 introduces the concept of a 1T-FeFinFET-based memory cell, discussing its design and functional advantages. Finally, Section 1.9 presents an analysis of performance enhancements in magneto-resistive memory, with a particular emphasis on the optimization of a 1-bit STT-MRAM cell.

1.4 Ferroelectric-based Memory

1.4.1. Ferroelectricity and ferroelectric material

The concept of ferroelectricity was first observed in Rochelle salt ($NaKC_4H_4O_{6.4}H_2O$) in 1921 [34],[35] leading to the discovery of other ferroelectric materials. Ferroelectricity is a property of certain piezoelectric materials, characterized by the presence of spontaneous electric polarization [36].This polarization can be reconfigured by the application of an external electric field, enabling bistable switching behavior essential for NVM applications [37]. The materials that exhibit these properties are called ferroelectric materials. The process of changing the polarity of a ferroelectric material by applying an external electric field is known as "switching''. These materials have the unique ability to retain their polarization state even after the external electric field is no longer present. However, when a sufficiently strong electric field is applied in the opposite direction, the polarization reverses [**Figure 1.5**].

In 1957, researchers at Bell laboratories [38] first suggested using ferroelectric materials to control the surface conductivity of semiconductor layers. Their aim was to develop a device capable of non-volatile switching, data storage, and non-destructive readout [36]. Later, Zuleeg *et.al*. [39] demonstrated that this ferroelectric field effect also influenced the transistor's threshold voltage (V_{th}), which plays a key role in modern FeFET devices.

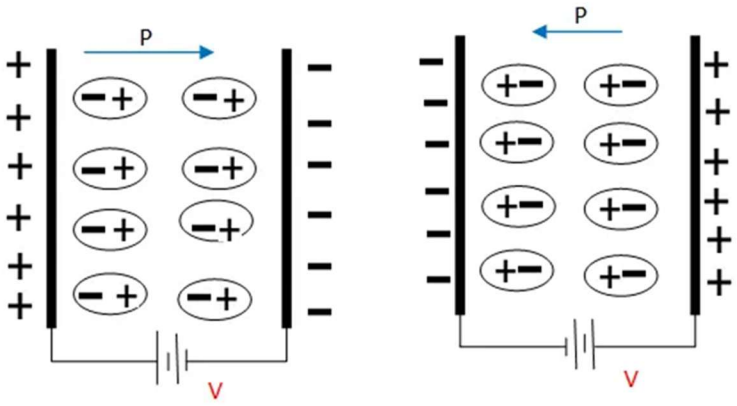

Figure 1.5 Polarization direction is changing by changing the direction of the voltage.

1.4.2. Ferroelectric Materials: Structure, Properties, and Memory Applications:

Ferroelectric materials have a non-centrosymmetric crystal structure, which allows them to exhibit spontaneous polarization [8]. Most ferroelectric materials, such as barium titanate ($BaTiO_3$) [40], lead zirconate titanate (PZT) [41], and strontium bismuth tantalate (SBT) [42], have a perovskite structure (ABO_3 type). This consists of a cubic or tetragonal lattice, where the A-site (e.g., Ba^{2+} or Pb^{2+}) is a large cation, the B-site (e.g., Ti^{4+} or Zr^{4+}) is a smaller transition metal cation, and oxygen ions (O^{2-}) form an octahedral coordination around the B-site ion. In the ferroelectric phase, the B-site ion shifts (up or down, as shown in **Figure 1.6**), breaking symmetry and leading to spontaneous polarization. Below the Curie's temperature (T_C), the crystal undergoes a phase transition [43], and the B-site ion moves off-center, creating an electric dipole shown in **Figure 1.6**. The alignment of these dipoles leads to macroscopic polarization, which can be reversed by an external electric field. Since Intel introduced high-*k* metal gate (HKMG) MOSFETs in 2007 [44], HfO_2 has been widely adopted as a gate dielectric in the semiconductor industry due to its seamless integration with CMOS technology. Unlike perovskite materials such as PZT and SBT, zirconium (Zr)-doped HfO_2 is fully CMOS-compatible and significantly reduces parasitic leakage in the gate stack, making it

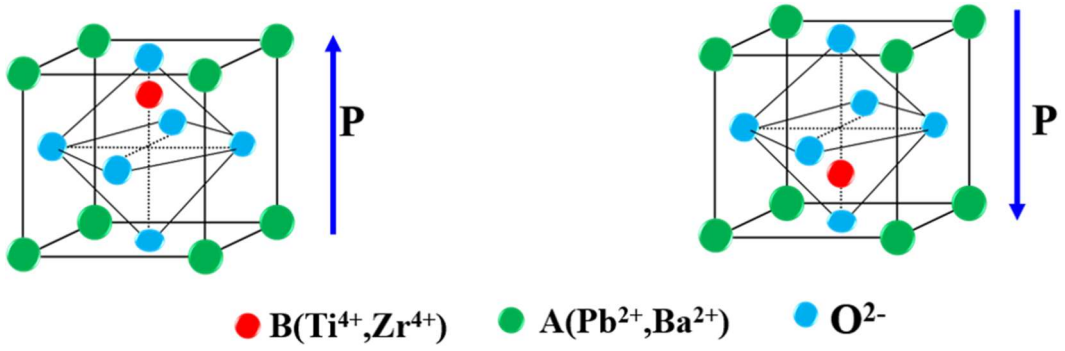

Figure 1.6 Tetragonal structure and polarization (a) Up polarization (b) Down polarization.

ideal for advanced memory and logic applications [45]. Hence, hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$ or HZO) has emerged as a superior ferroelectric material [46], offering several advantages over traditional perovskite-based materials [e.g., $Pb(Zr_xTi_{1-x})O_3$ – PZT, $SrBi_2Ta_2O_9$ – SBT)], making it highly suitable for modern semiconductor applications [47].

Boscke *et al.*[48] first reported ferroelectricity in doped HfO_2 ($Hf_{0.4}Zr_{0.6}O_2$), which is compatible with CMOS technology, in 2011. Unlike traditional perovskite-based ferroelectrics, HZO exhibits ferroelectricity in ultrathin films (<10 nm), making it highly suitable for modern semiconductor applications [49]. One of the biggest advantages of $Hf_{0.5}Zr_{0.5}O_2$ is its compatibility with CMOS technology because hafnium oxide (HfO_2) is already used as a high-*k* dielectric in advanced transistors, ensuring easy integration [50],[51]. Additionally, $Hf_{0.5}Zr_{0.5}O_2$ maintains its ferroelectric properties even at sub-10 nm thickness, unlike traditional ferroelectric materials that require significantly thicker films. Moreover, it can be integrated using standard atomic layer deposition (ALD), a widely used process in semiconductor fabrication. The integration of FeFET memory devices into 28 nm HKMG technology was first demonstrated in [52] using $Hf_{0.5}Zr_{0.5}O_2$. It enables non-volatile data storage by modulating the transistor's threshold voltage (V_{th}) through ferroelectric polarization.

Ferroelectricity arises due to the non-centrosymmetric arrangement of ions within a ferroelectric crystal lattice, as depicted in **Figure 1.7**. This unique characteristic enables ferroelectric materials to exhibit spontaneous polarization, which can be retained even in the absence of an external electric field (E) [37]. This property is crucial for non-volatile memory applications, as it allows ferroelectric devices to maintain stable polarization states. By applying an electric field in the opposite direction, the polarization (P) can be reversed, leading to distinct electrostatic behaviors between the up and down polarization states. The properties of a ferroelectric material are strongly dependent on temperature [53]. Above the Curie's temperature, ferroelectric materials make a transition into a paraelectric phase, which is inherently a centrosymmetric structure, meaning no spontaneous polarization occurs, and no polarization-electric field (P-E) hysteresis loop is observed. Below T_C, the material enters the ferroelectric phase, where a P-E hysteresis loop emerges when an external electric field is applied. This behavior can be described using the Landau-Ginzburg-Devonshire theory [54],[55] which predicts two local minima in the Gibbs free energy (G) vs. polarization curve [illustrated in **Figure 1.7 (b)**]. These minima correspond to the two stable polarization states, which can be switched by applying a sufficient external field.

The P-E hysteresis loop in ferroelectric materials shown in **Figure 1.7(c)** represents the response of polarization to an applied electric field. It allows for the extraction of important material parameters, including spontaneous polarization (P_S), remnant polarization (P_r), and coercive electric field (E_C). This loop demonstrates the non-linear and bistable nature of ferroelectric materials, making them suitable for NVM applications. When an external electric field is applied to a ferroelectric material, its spontaneous polarization aligns with the field

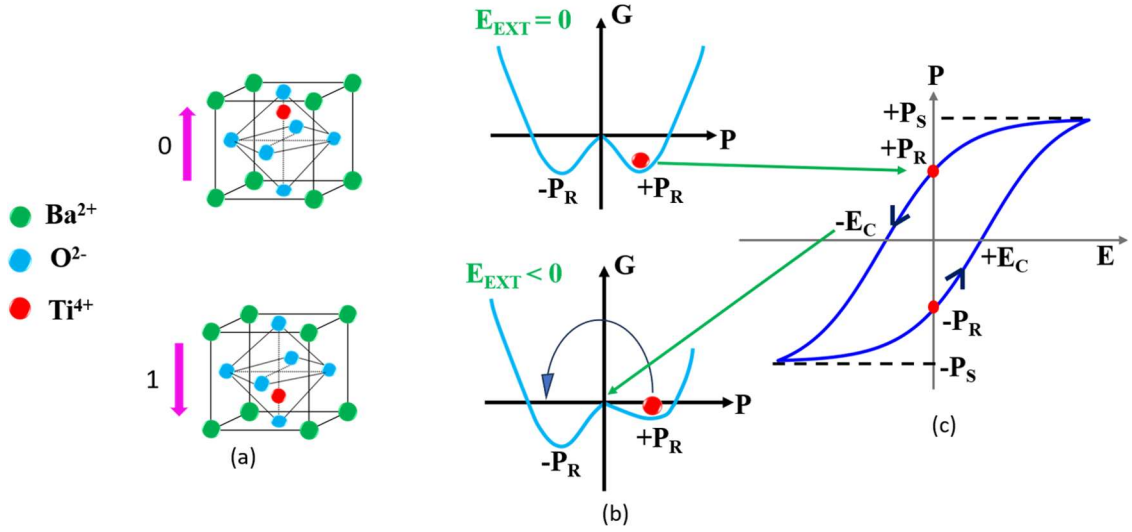

Figure 1.7 (a) The unit cell of a barium titanate ($BaTiO_3$) crystal illustrates two stable positions where the central Ti ion shifts upward or downward relative to the adjacent oxygen ion along the tetragonal symmetry axis. This displacement results in a net electric polarization oriented upward (state "0") or downward (state "1"). (b) The Landau energy profile of the ferroelectric material depicts the polarization states. The two energy minima represent the stable polarization configurations. (c) The polarization vs electric field curve shows hysteresis nature.

direction. As the field increases, the polarization reaches a maximum value called saturation polarization, where all dipoles are aligned. When the field is reduced back to zero, the material retains some polarization, known as remnant polarization, indicating that the material has a memory of its previous state. A field in the opposite direction must be applied to completely reverse the polarization. The minimum required field to achieve zero net polarization is called the coercive field. As the reverse field strength increases, the polarization eventually reaches negative saturation ($-P_s$), completing the hysteresis loop.

1.5 Ferroelectric Memory Devices

Ferroelectric memories utilize the spontaneous and reversible polarization of ferroelectric materials to store data. Unlike conventional semiconductor memories, ferroelectric memories retain stored information without requiring a constant power supply, making them highly

energy-efficient and well-suited for neuromorphic applications [56]. Due to their non-volatile nature, low power consumption, and capability to exhibit multi-level resistance states, ferroelectric memories have emerged as promising candidates for synaptic devices. In this thesis, we investigate advancements in ferroelectric memory technologies, focusing on ferroelectric field-effect transistors and their potential applications in neuromorphic computing. Advancements in thin ferroelectric film fabrication have resulted in the emergence of two fundamental types of ferroelectric memories: FeRAM [57],[58] and FeFET-based memory [8],[59]. The FeFET device and FeFET-based memory are discussed in the following sections.

1.5.1. Ferroelectric field-effect transistor (FeFET) memory

During the late 1950s, the concept of FeFET memory emerged [38]. This approach involves replacing the conventional insulating layer in the gate stack of a field-effect transistor with a ferroelectric layer. **Figure 1.8** illustrates an example of an n-channel silicon-on-insulator (SOI) FeFET device [60]. The transistor channel's conductivity is modulated by the polarization charge emanating from the ferroelectric layer, which can be modified through the application of a voltage to the gate electrode. When a positive gate voltage is administered, a positive polarization charge materializes at the junction in the ferroelectric layer between the metal and semiconductor layers. It exerts an electrostatic force on electrons in the body and changes the conductivity of the channel [**Figure 1.8(a)**]. In this configuration, the FeFET transistor operates in the low threshold voltage state.

On applying a negative gate voltage induces the formation of a negative polarization charge, resulting in the repulsion of electrons at the interface of ferroelectric and semiconductor and a reduction in channel conductivity [**Figure 1.8(b)**]. Consequently, the FeFET

transistor resides in the high-threshold voltage state. The readout of this cell can be performed non-destructively by monitoring the drain current without causing any alteration to the

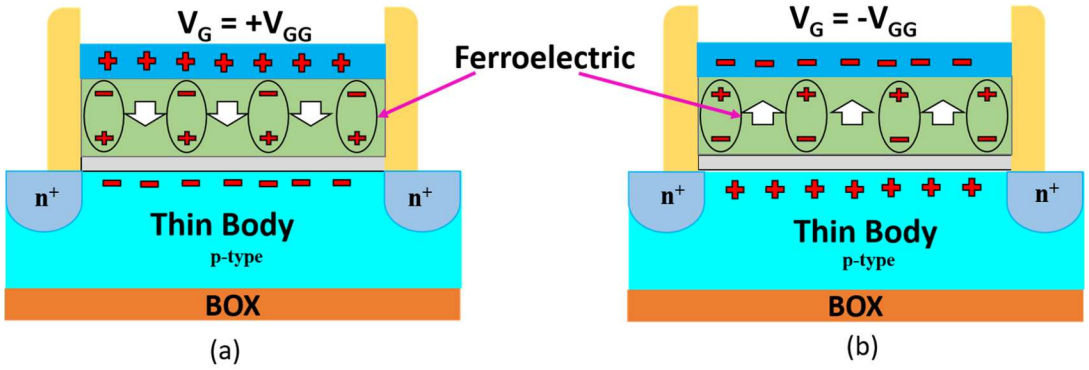

Figure 1.8 Basic structure of early FeFET (a) ON-state (b) OFF-state.

polarization of the ferroelectric layer. An advantageous aspect of FeFET technology lies in its ability to address the scaling limitations faced by FeRAM [61]. This advantage stems from the fact that the ferroelectric capacitance and oxide capacitance are no longer treated as independent components, presenting a potential solution to the challenges of downscaling the cell.

Furthermore, due to the close proximity of the semiconductor channel and ferroelectric material, charge injection from the channel becomes inevitable, resulting in compensation of the polarization charge and negatively impacting retention properties [62]. In early FeFET devices [62], [63], this charge trapping phenomenon was particularly severe, overpowering the voltage threshold shift that occurs during the write operation and obscuring the ferroelectric polarization [64]. To address the issues of inter-diffusion and charge trapping [65], a high-*k* interface buffer layer was introduced between the semiconductor and ferroelectric layers [66]. This innovation led to the development of the metal-ferroelectric-insulator-semiconductor (MFIS) cell type, as depicted in **Figure 1.9**.

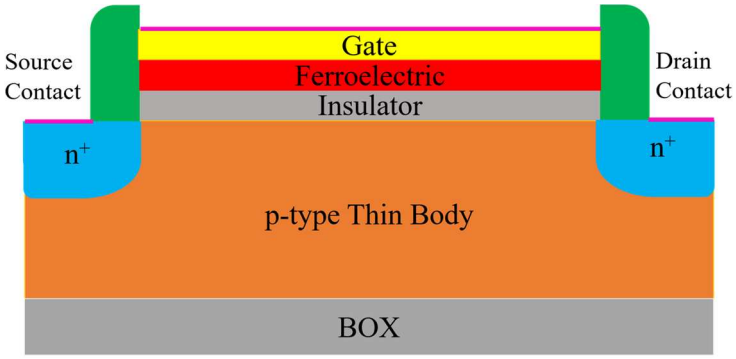

Figure 1.9 MFIS FeFET Structure.

1.6 FinFET Architecture-based Ferroelectric Memory: FeFinFET

Compared to conventional planar CMOS transistors, fin field-effect transistor (FinFET) technology offers superior control over leakage current due to its unique 3-D fin-shaped channel structure, as shown in **Figure 1.10** [67]. By wrapping the gate around the fin on three sides, FinFETs provide better electrostatic control over the channel, effectively reducing leakage currents. As a result, FinFETs offer higher energy efficiency and lower power consumption, making them well-suited for cutting-edge semiconductor applications [68]. Additionally, FinFETs are highly scalable, enabling superior performance and improved integration density compared to traditional planar CMOS transistors [69], making them the preferred choice for advanced technology nodes [70],[71]. So, in this thesis, we have focused exclusively on FinFET architecture-based FeFET devices referred to as ferroelectric fin field-effect transistors (FeFinFET). Furthermore, for neuromorphic applications, we have utilized the SOI FinFET architecture, which offers several advantages over bulk FinFET architecture. In SOI FinFETs, a buried oxide (BOX) layer beneath the silicon channel (as shown in **Figure 1.10**) is present, which isolates the device from the substrate, providing the following advantages compared to bulk FinFET architecture.

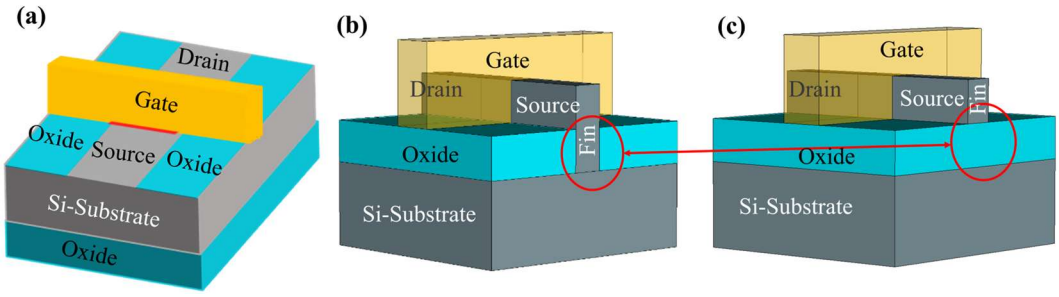

Figure 1.10 3-D structure of (a) Planar MOSFET (b) Bulk FinFET (c) SOI FinFET.

1. The BOX layer prevents leakage paths through the substrate, reducing off-state leakage currents. This enhances power efficiency, making SOI FinFETs well-suited for low-power applications.
2. SOI FinFET provide better electrostatic control over the channel due to their isolation from the substrate, which helps reduce short-channel effects such as subthreshold swing and drain-induced barrier lowering (DIBL).
3. The insulating layer in SOI FinFETs reduces parasitic capacitance between the source/drain (S/D) and the substrate, which enhances switching speed and reduces power consumption.

FeFinFET is an emerging device architecture that incorporates a ferroelectric layer ($Hf_{0.4}Zr_{0.6}O_2$) into the gate stack of a conventional FinFET. **Figure 1.11** illustrates a 3-D representation of FeFinFET along with its 2-D cross-sectional view, where the HZO layer within the gate stack is clearly visible. FeFinFET leverages the ferroelectric properties of materials like HZO to introduce remnant polarization in the gate dielectric. Unlike traditional FinFETs, FeFinFETs exhibit hysteresis in their transfer characteristics, enabling bistable states for non-volatile memory applications. This modification enhances device performance by providing non-volatile memory functionality, improved subthreshold characteristics, and

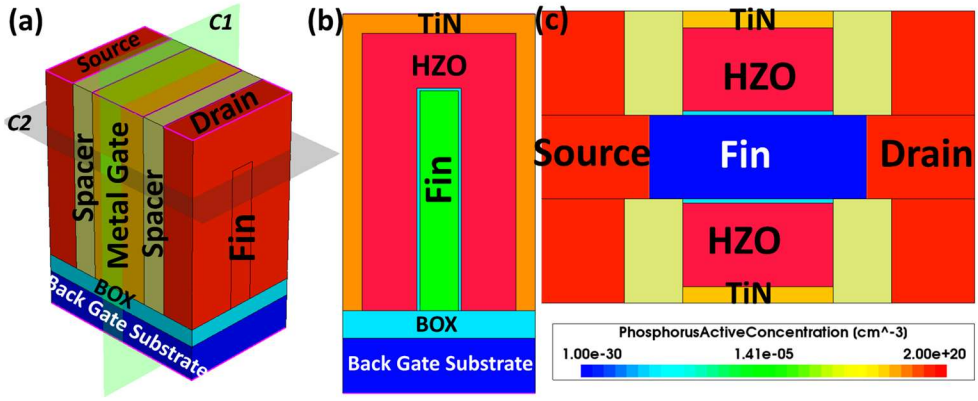

Figure 1.11 (a) 3-D structure of an n-MOS SOI FeFinFET. The 2-D cross-sectional views of the three-dimensional FinFET are depicted along the cut planes (b) *C1* and (c) *C2*.

energy-efficient operation. Over the past decade, extensive research has been conducted on FeFinFETs, focusing on their design, electrical characteristics, and potential applications in memory and neuromorphic computing.

1.6.1. Junctionless FeFinFET

In 2010, the concept of junctionless transistors was reintroduced to eliminate the need for ultra-steep doping profiles. This led to the experimental demonstration of nanowire field-effect transistors without junctions [72],[73]. These devices, referred to as junctionless field-effect transistors (JLFET), consist of a uniformly doped semiconductor film, where the gate electrode regulates the channel resistance and thereby controls the current flow. Due to this behavior, JLFETs are also known as gated resistors [74]. As transistor sizes continue to shrink, fabricating junction-based transistors becomes increasingly challenging. The complex manufacturing process of these transistors has led to the development of alternative structures known as junctionless (JL) transistors [75],[76],[77],[78],[79]. These JL transistors were developed as a solution to simplify the manufacturing process while still achieving smaller transistor sizes. Just like FeFinFET, JL FeFinFET is also a 1T cell of non-volatile

memories. It is called 'Junction-less' because there are no junctions and no doping concentration gradients[72], [80],[81]. The omitted requirement of source and drain implantation is an advantage of JL FeFinFET over FeFinFET [82]. Some of the JL FeFinFET based non-volatile memory are shown in [83],[84].

1.6.2. Enhancing JL FeFET through accumulation mode

In order to address the effects of moderately doped source/drain regions in JLFET, the high series resistance has a notable impact on reducing the ON-state current. Consequently, this leads to an increased intrinsic delay in JLFET compared to conventional FET, ultimately resulting in a decreased operating frequency for digital circuits. To tackle this challenge, researchers have investigated the use of JLFET with an additional S/D implantation. This approach aims to enhance the S/D doping and minimize the series resistance, leading to the development of junctionless accumulation-mode field-effect transistors (JAM FET) [85],[86],[87]. The heavily doped S/D regions in JAM FET result in the creation of high-low junctions at the source-channel and channel-drain interface. As a result, JAM FETs exhibit a pseudo-junctionless behavior [88].

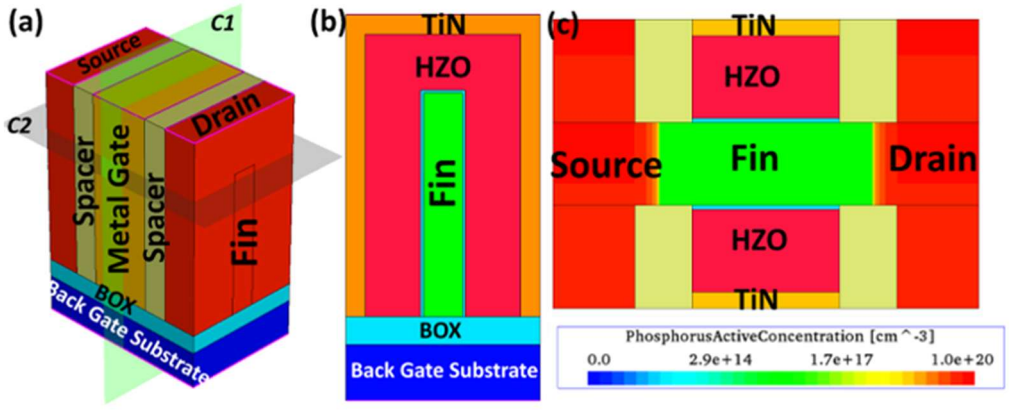

Figure 1.12 Structure of 3-D JAM FeFinFET. A 2-D cross-sectional view of JAM FeFinFET along the plane (a) C1 and (b) C2.

By integrating HZO as a ferroelectric layer in the gate stack of a JAM FinFET, the device is transformed into a JAM FeFinFET. **Figure 1.12** illustrates the 3-D architecture of the JAM FeFinFET, while the 2D cross-sectional view along the cut-plane *C1* highlights the HZO layer within the gate stack. In contrast to JL FeFinFET, JAM FeFinFET has heavily doped source and drain regions. The low doping concentration in the channel region of JAM FeFin-FET allows it for volume depletion even with gate electrodes having midgap work functions (ranging from 4.5 to 4.7 eV) [89]. As a result, JAM FeFinFET simplifies the fabrication process since they don't necessitate gate electrodes with excessively high work functions, unlike JL FeFinFET [86]. Further, the log/linear scale comparison of transfer characteristics of the JAM FinFET and conventional FinFET are shown in **Figure 1.13(a)**. The OFF current refers to the leakage current that flows when the transistor is in its "OFF" state, *i.e.*, when the gate voltage is below the threshold voltage. Here the measured threshold voltage of JAM and conventional FinFET are 0.33 V and 0.35 V, respectively. The benchmark for obtaining the threshold voltage is a drain current of 10^{-6} A at V_{DS} = 0.1V. The difference in the threshold voltage of both devices is very small, and this is because of the 3nm node FinFET structure.

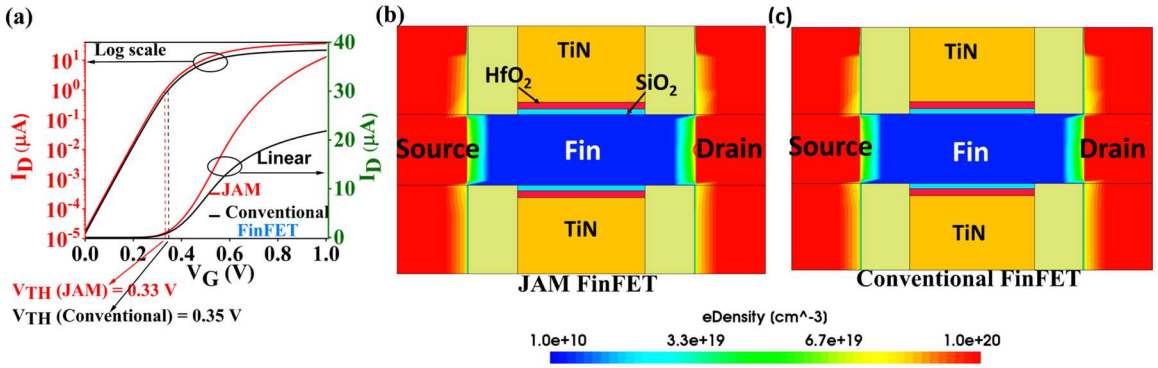

Figure 1.13 (a) Comparison of I_D-V_G curve of (a) JAM and conventional FinFET in log/linear scale, (b)-(c) shows the two-dimensional cross-section of the 3-D FinFET along the cut-plane C1. (b) Describes the electron density profile of JAM FinFET for biasing condition V_{GS} = V_{DS} = 0.1 V, (c) Describes the electron density profile of Conventional FinFET for biasing condition V_{GS} = V_{DS} = 0.1 V. (Here, we have used HfO_2 as a high-*k* dielectric material).

The technology computer-aided design (TCAD)-simulated comparison of OFF state (*i.e.*, $V_{GS} = V_{DS} = 0.1$V) electron density in the channel region for JAM and conventional FinFET is shown in **Figure 1.13(b)**. It shows that in both devices, carrier density is reduced, which confirms the depletion of charge carriers when the gate voltage is small and less than the threshold voltage of the device. In conclusion, both accumulation mode (AM) and inversion mode (IM) devices offer similar leakage current characteristics and almost equal threshold voltage in ultra-scaled FinFETs, thus corroborating the findings from [90]. Additionally, when ferroelectric material is introduced in the gate stack of both JAM and IM FinFET, Only the ON state current shows a significant variation. Hence, The JAM FeFinFET structure offers advantages over the IM FeFinFET by providing higher ON current and history-dependent conductance at low voltages, making it a promising candidate for synaptic applications.

1.7 Ferroelectric Memory as a Synaptic Device

A key element in neuromorphic systems is the synaptic device, which plays a crucial role in enabling intelligent tasks with low power consumption and reducing chip size. This is achieved by integrating high-density synapse arrays within deep neural network (DNN) hardware [91], enhancing computational efficiency and scalability [92],[93]. Ferroelectric memory has attracted significant interest as a synaptic device due to its non-volatility, low power consumption, and memristive behavior [94]. Additionally, its multi-level conductance states enable efficient synaptic weight modulation, making it well-suited for neuromorphic applications. The memristive behavior of ferroelectric materials is commonly observed through their reversible polarization [95],[96],[97]. Jiankun Li *et al.*[98] reported an artificial synapse utilizing ferroelectric tunnel junction devices based on Pt/$BaTiO_3$/Nb-doped $SrTiO_3$.

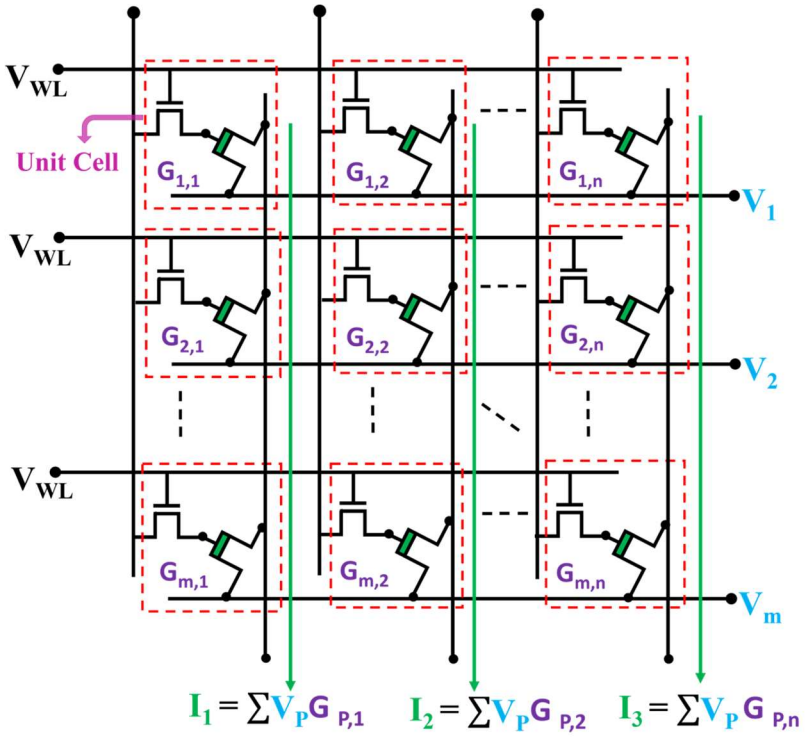

Figure 1.14 FeFET-based pseudo crossbar array.

This device effectively emulates neural signal transmission, making it a promising candidate for neuromorphic computing applications. Furthermore, FeFET exhibits significant potential for synaptic transistor applications. These devices can be employed to develop a crossbar array, as shown in **Figure 1.14** [99]. In this crossbar array, each unit cell representing a synaptic weight consists of an access transistor and a FeFET, which functions as both a synaptic and storage device. **Figure 1.14** illustrates the operating mechanism of a three-terminal FeFET-based synaptic weight modification within the crossbar structure. In this configuration, the synaptic weight is controlled by the gate voltage (V_{WL}), which operates independently of the input line in the three-terminal design. The transistor's conductivity (G_{ij}), representing the synaptic weight, can be modulated to increase (potentiation) or decrease (depression) through either pulse amplitude modulation or pulse width modulation.

1.7.1. The potential of FeFinFET as a synaptic device

An outstanding feature of FeFinFET is its capability to emulate the functions of biological synapses. This characteristic enables it to perform essential synaptic tasks like weight storage and modifiable plasticity, which are vital for constructing efficient and adaptable neural networks. Numerous studies have illustrated the feasibility of utilizing FeFinFET as a synaptic device by demonstrating its capacity to replicate synaptic plasticity, spike-timing-dependent plasticity (STDP), and other synaptic functionalities. A compact synapse based on a single FeFET was previously reported with high-*k* metal gate technology [100], and a FeFET analog synapse with symmetric potentiation and depression characteristics has been demonstrated in [101]. The advantages of FeFinFET, including its low power consumption, enhanced device scalability, and compatibility with complementary metal-oxide-semiconductor processes, have been recognized by researchers. These characteristics position FeFinFET as a promising choice for synaptic devices in neuromorphic systems [100]. However, there is still an opportunity to develop the synaptic crossbar array with higher integration density by using a junctionless feature. Back-end-of-line (BEOL) compatible junctionless FeFET devices have been introduced by Halter *et al.* [82] and are used as synaptic devices. However, integrating these devices into the BEOL process introduces significant cost overhead. Additionally, these devices feature a planar design which may pose scalability challenges. On the other hand, a front-end-of-line (FEOL) FeFinFET synaptic device has been demonstrated in [84], but it requires a separate fabrication process. Moreover, the device's ability to modulate conductance or resistance in response to electrical signals may be restricted due to its high operating voltage requirements, potentially limiting its efficiency for low-power neuromorphic applications. Mulaosmanovic *et al.*[100] demonstrates the transmission of weighted

signals in FeFET and the implementation of asymmetric spike-timing-dependent plasticity. Additionally, it examines how spike timing and resistance variations influence the modulation of STDP.

In addition to its unique characteristics, FeFinFET shows advantages over other synaptic devices like, RRAM [102] and PCM [103] in several aspects. It demonstrates enhanced compatibility with CMOS processes and offers improved scalability. Furthermore, FeFinFET has a low power consumption which further enhances its appeal as an energy-efficient choice for neuromorphic systems.

Therefore, in this thesis, we introduce and demonstrate a FEOL JAM FeFinFET, which is fully compatible with SOI process flow. The proposed synaptic weight device effectively emulates conductance modulation with greater precision while operating at low voltage. Additionally, it offers seamless integration with standard SOI FinFET technology without introducing any processing overhead, making it a highly efficient solution for neuromorphic applications.

1.8 FeFinFET-based Memory Cell

FeFinFET-based memory cells have gained significant attention due to their non-volatility, low power consumption, and potential for high-speed operation. These advantages make FeFET-based memory cells well-suited for array-based and distributed data storage applications [59],[27], as well as for emerging neuromorphic computing technologies. This subsection covers various FeFET-based memory cell architectures, including 1-transistor (1T) and 2-transistor (2T), highlighting their advantages, limitations, and recent advancements. The different 2T cell architectures are shown in **Figure 1.15**.

Traditional FeFET-based NVM relies on a one-transistor-per-cell (1T/cell) architecture

[104], which offers high storage density. However, it also presents several drawbacks:

(i) Write disturbance in unselected cells because there is no shielding transistor to isolate them.

(ii) Increased power supply complexity due to the requirement for multi-level voltage control.

(iii) Higher write energy consumption due to the need to charge two-bit lines simultaneously.

1T/cell architecture offers a significant advantage over the traditional one-transistor-one-capacitor (1T-1C) design used in FeRAM [105],[57],. Specifically, the FeFET enables non-destructive read operations. FeFET is considered a promising candidate for next-generation embedded NVM due to its fast write speed, non-destructive read capability [106], and extremely low energy consumption during switching. However, the FeFET-based 2T NVM described in [107] utilizes an access/select transistor to control the gate voltage of the FeFET shown in **Figure 1.15 (a)**. During the write operation, both the source and drain voltages of the FeFET remain at zero. This architecture results in a coupled read and write path while also requiring high bit-line (BL) voltages for FeFET programming. Consequently, the select transistor must be larger and operate at higher voltages to set or reset the memory state, reducing both energy and area efficiency. Moreover, these memory cells typically exhibit poor endurance [64] and require an additional read voltage to retrieve data when power is turned off, making them susceptible to data corruption due to destructive read operations. Furthermore, the 1T-1FeFET architecture proposed in [108] ,and shown in Figure **1.15 (b)** requires an extra read voltage to retrieve stored information, which disturbs the polarization of the ferroelectric material.

Hence a new memory cell configuration consisting of one transistor and one memristor

(1T-1M) has gained significant attention in the fields of non-volatile memory and neuromorphic engineering. In this hybrid design [109], a transistor is coupled with a memristor to create a primary storage element, for data retention and processing.

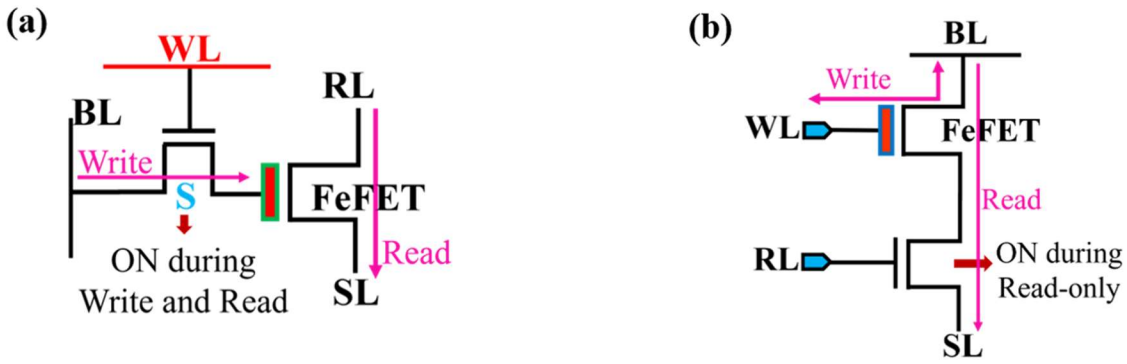

Figure 1.15 2T memory cell proposed in references (a) [107] (b) [108].

1.9 Magneto-Resistive based Memory

Magneto-resistive-based memory refers to non-volatile memory technologies that store data using the magnetoresistance effect, where the electrical resistance of a device depends on the relative magnetization of its layers. The most well-known example is magneto-resistive random-access memory (MRAM), particularly STT-MRAM.

1.9.1. Bit cell in spin-transfer torque magneto-resistive random-access memories (STT-MRAM)

STT-MRAM is a non-volatile memory technology that leverages the principles of spintronics to store information [110]. Unlike conventional charge-based memory technologies, STT-MRAM utilizes the spin orientation of electrons to represent binary data, offering advantages such as high endurance, low power consumption, and scalability [111]. The fundamental building block of STT-MRAM is the 1-bit memory cell, which consists of a magnetic tunnel junction (MTJ) and an access transistor. This section provides a comprehensive

description of the 1-bit STT-MRAM cell, including its structure, operating principles, and key performance metrics.

1.9.2. Structure of the 1-bit STT-MRAM cell

The 1-bit STT-MRAM cell is composed of two primary components: the MTJ and an access/select transistor. The MTJ serves as the storage element, while the transistor controls access to the MTJ during read and write operations. The architecture of a 1-bit STT-MRAM cell is shown in **Figure 1.16**. The MTJ is a trilayer structure consisting of two ferromagnetic layers separated by a thin insulating barrier (typically MgO) [112]. The two ferromagnetic layers are the reference layer and the free layer. The reference layer or pinned layer has a fixed magnetization direction, which is typically pinned by an adjacent antiferromagnetic layer (e.g., IrMn or PtMn), while the free layer has a switchable magnetization direction that can be aligned either parallel or antiparallel to the reference layer, representing binary states "0" and "1," respectively. Further, the insulating barrier is thin enough (typically 1-2 nm) to allow quantum mechanical tunneling of electrons between the two ferromagnetic layers. A silicon-based NMOS transistor connected in series with the MTJ to control read/write operations is known as an access transistor as shown in **Figure 1.16**. This transistor limits the current during read operations and isolates the MTJ during standby.

1.9.3. Challenges in designing the access transistors for a 1-bit STT-MRAM cell

The access transistor in a 1T-1MTJ (one-transistor, one-magnetic tunnel junction) STT-MRAM cell plays a pivotal role in controlling read/write operations by regulating the current flow through the MTJ. One of the critical challenges in STT-MRAM design is the asymmetric current requirement for switching the MTJ from the parallel (P) to the antiparallel (AP) state and vice versa. This asymmetry arises due to the different energy barriers and spin-

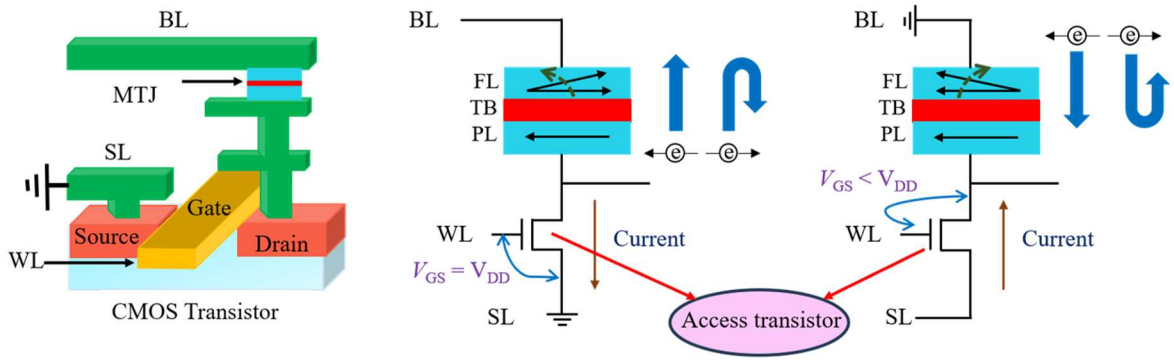

Figure 1.16 (a) 3-D Schematic of a 1-bit STT-MRAM cell. The MTJ is integrated with an access transistor in a 1T-1MTJ configuration (b) Standard connected STT-MRAM bit-cell.

torque efficiencies associated with the two switching directions. Switching from the P→AP state requires a higher current ($I_{P\rightarrow AP}$) due to a larger energy barrier, while the reverse transition (AP→P) demands a lower current ($I_{AP\rightarrow P}$). Conventional symmetric access transistors, designed to handle the worst-case current ($I_{P\rightarrow AP}$), lead to overdesign, energy inefficiency, and excessive power consumption.

To address this, asymmetric access transistors have been proposed. By using asymmetric devices in the access transistors, we can reduce the excess current that flows during the change in the magnetic state of the MTJ from AP→P. Further, asymmetric devices have also been used to enhance the performance of SRAM [113],[114]. This section reviews the literature on asymmetric access transistors, highlighting their advantages and key challenges.

1.10 Recent Progress in Circuit and Device Techniques for Asymmetric Write Current Management in 1-bit STT-MRAM Cell

In recent years, researchers have made significant strides in addressing the challenge of asymmetric write current requirements through various innovative approaches at both the device and circuit levels [115],[116],[117],[118],[119],[120]. These advancements include the development of circuit design techniques and novel device architectures aimed at

balancing and optimizing write current demands. Kim *et al.* [120] investigated circuit-based solutions to tackle the issue of asymmetric write current in STT-MRAM cells. Their proposed methods include bit-line voltage clamping through a pass transistor and the 2T-1R dual source-line (SL) technique. While these approaches effectively address the write current imbalance, they come with a notable drawback: both techniques require the integration of an extra transistor. This additional component substantially increases the overall area of the STT-MRAM bit-cell, posing a challenge for achieving higher memory density and scalability. Further, at the device level, researchers have explored the use of asymmetrically doped (AD) access devices to optimize write current in STT-MRAM bit cells, as demonstrated in [118],[119], and [121]. In AD devices, the source/drain region is lightly doped with respect to others to introduce asymmetry in drive current during forward and reverse conduction. Additionally, the concept of asymmetric spacer (AS) devices has been proposed in [122], where asymmetry is achieved by employing different spacer materials. Extensions of this idea, such as AS FinFET devices, have also been reported in [123] and [124]. However, the fabrication of AS FinFET devices presents significant challenges, particularly in creating an asymmetric dielectric spacer while maintaining symmetrical underlap regions (areas beneath the spacers) on both sides. Both AD and AS devices necessitate an additional mask to introduce the required asymmetry, significantly increasing fabrication complexity and cost and making their integration into standard CMOS processes less economically viable. These challenges highlight the trade-offs between performance optimization and manufacturability in advanced memory technologies. In this thesis, we have focused on a novel FinFET device architecture with an asymmetric drive current that meets the requirements of asymmetric write current in an STT-MRAM 1-bit memory cell.

1.11 Asymmetric Transistors

The concept of planar asymmetric field-effect transistors was explored in the early 2000s by Wheeler *et al*. [125]. Recently, FinFET devices have been used commercially with faster switching times and higher current density than planar CMOS technology. The idea of introducing asymmetry in transistor structures was initially motivated by the need to optimize drive current, power efficiency, and switching speed in logic and conventional memory circuits, e.g. SRAM. The use of asymmetric transistors in NVM, particularly STT-MRAM performance enhancement, has started gaining attention. The idea has been to exploit asymmetric drive currents to match the non-uniform switching characteristics of MTJ in STT-MRAM. Asymmetric transistors have emerged as a promising solution for optimizing the performance of STT-MRAM memory cells [118],[119],[122] . These transistors are designed to exhibit different drive currents in forward and reverse conduction, effectively addressing the challenges posed by asymmetric write current requirements in STT-MRAM cells.

1.11.1. Existing designs of asymmetric transistors for access devices in STT-MRAM cells

Some asymmetric FinFET devices have also been reported in [118],[119],[122],[124] and [121] are used to enhance the performance of the STT-MRAM bit cell. In [118] and [119], the asymmetry is due to the different doping concentrations used in the source and drain regions. In references [122] and [124], the asymmetry is due to the different materials of the spacer at the source and drain side. Herein, the major fabrication challenge associated with these asymmetric devices is to form asymmetric dielectric spacers, along with symmetrical underlap regions (regions below the spacers) on both sides. Furthermore, in the patent [90], the asymmetry is due to the use of the asymmetric distance between consecutive fins with

different gate work functions. As a result, the architecture of the asymmetric FinFET device in [118][119],[122],[124], and [121] is quite challenging from a fabrication point of view because they require several extra masks to create asymmetry in the device, which makes them very costly to be accommodated in a pristine FinFET process flow.

To address these fabrication challenges, this thesis proposes a novel process flow, which is discussed in Chapter 3, that is compatible with the pristine FinFET process flow. Further, the proposed architecture is better in terms of drive current, asymmetricity ratio, gate capacitance, and robustness as compared to the asymmetric device proposed in [118][119],[122],[124], and patent [121] for write-optimized STT-MRAM applications. Low gate capacitance provided by the proposed structure further highlights the advancement achieved in this work that can translate into a low write line capacitance in STT-MRAM bit-cell. The detailed comparison of our proposed asymmetric device with the existing asymmetric device is shown in **Table 1.1**.

1.11.2. Design aspects of asymmetric transistors

The design of asymmetric transistors involves several key considerations to achieve the desired electrical behavior, which can be realized through multiple design techniques. The primary design approaches include:

1. **Asymmetrically doped (AD) transistors:** AD transistors achieve asymmetry by selectively doping the source and drain terminals. In these devices, one terminal is lightly doped while the other remains heavily doped.
2. **Asymmetric spacer (AS) transistors:** AS transistors employ different dielectric material on either side of the gate to create asymmetry in the electric field distribution. This variation in dielectric materials influences carrier transport, resulting in

asymmetry in drive currents during forward and reverse conduction.

Table 1.1 Comparison of existing asymmetric transistor

Reference	Reason of asymmetricity	Additional mask requirements	Shifting of mask	Gate capacitance
[121]	Asymmetric distance between consecutive fins with different gate work functions.	Yes	No	High
[126]	1. Use of two opposite types of dopants in the S/D regions. 2. Asymmetric width and different liner materials are used as contact at the S/D region.	Yes	No	High
[122]	Different materials of the spacer at the S/D side.	Yes	No	High
[124]	Different materials of the spacer at the S/D side.	Yes	No	High
[118]	Different doping concentrations are used in the S/D regions. *i.e*, one is lightly doped in comparison to other regions.	Yes	No	High
[119]	Different doping concentrations are used in the S/D regions. *i.e*, one is lightly doped in comparison to other regions.	Yes	No	High

In this thesis, we have introduced a novel design that involves trimming the channel region of the transistor to create asymmetry in the drive current, which is discussed in detail in Chapter 3. Further, a selective fin-trimming step that is executed during the replacement of the metal gate process, along with a dielectric deposition in the trimmed fin regions, is the advancement done in process flow which has been demonstrated through process emulation in Sentaurus TCAD software.

1.12 Problem Statement

This thesis examined device-circuit co-design for FeFET and MTJ-based non-volatile memory, building on insights gained from an extensive literature review presented in the preceding sections. Section 1.3 discusses the role of synaptic devices in neuromorphic computing and explores various emerging non-volatile memory technologies that function as artificial synapses, facilitating connections between neurons. Among these technologies, ferroelectric-based NVM was chosen for synaptic devices due to its three-terminal structure, which offered higher conductance compared to other NVM options. The fundamental requirements of ferroelectricity in materials, structural considerations, and the underlying physics of ferroelectric materials were elaborated in Section 1.4. Furthermore, Section 1.6 provided an in-depth discussion of different types of ferroelectric field-effect transistors designed using FinFET-based architectures. Existing FeFET-based synapses were reviewed in Section 1.7, where it was observed that some synaptic devices employed planar architectures and utilized the back-end-of-line fabrication process. However, these structures exhibited low conductance at high operating voltages. To address these limitations, a novel architecture can be proposed that achieved high conductance at low voltage while utilizing the front-end-of-line fabrication process. The literature survey in Section 1.8 examined various FeFinFET-

based memory cell architectures, with a particular focus on the commonly used 2T memory cell architecture in memory crossbar arrays and neuromorphic computing applications. Among existing 2T memory cells, some suffered from destructive readout and separate read/write paths, while others supported non-destructive readout but required an additional signal for reading stored information. Consequently, there was a need for a novel one-transistor, one-resistor (1T-1R) architecture that eliminated these constraints. Additionally, Section 1.9 explored the structure of an MTJ-based 1-bit STT-MRAM cell and discussed the role of the access transistor in enhancing its performance. Section 1.10 reviewed existing methods for improving STT-MRAM cell efficiency, identifying the design of an asymmetric transistor as the most effective approach. This asymmetric transistor provided an imbalanced drive current to the MTJ, improving overall device performance. However, a critical analysis of the existing literature on asymmetric transistors revealed the need for further design optimizations and a reduction in fabrication complexity to enhance their practicality. Based on the insights gained from the literature review, the key challenges identified in this thesis were systematically structured into distinct chapters as outlined below:

(i) In ***Chapter 2,*** we introduce an SOI-based JAM ferroelectric FinFET designed to function as a synaptic weight device for neuromorphic computing architectures. The proposed device enhances the non-volatile conductance range in the ON-state compared to conventional junctionless and ferroelectric FinFETs, thereby improving synaptic weight modulation. Our simulation results demonstrate that the device offers continuous, linear conductance variation and symmetric switching characteristics, which are crucial for synaptic weight applications. Furthermore, we have shown the experimental and process feasibility of this novel synaptic weight device through process emulation using Sentaurus TCAD. The proposed

design introduces zero process overhead and is fully compatible with standard FinFET fabrication flows, making it a promising candidate for integration into advanced neuromorphic systems.

(ii) ***Chapter 3***, deals with a 1T-1R memory cell that leverages a memristive variant of ferroelectric field-effect transistor for data storage. The proposed 1T-1Memristive FeFinFET (1T-1MFeFET) memory architecture has distinct write and read paths. Using experimentally calibrated models and TCAD-based mixed-mode simulations, the proposed MFeFET-based memory cell is shown to enable non-destructive read operations while achieving higher read currents at lower operating voltages. Additionally, this novel memory architecture offers lower read latency compared to conventional STT-MRAM technologies.

(iii) In ***Chapter 4***, we propose a novel asymmetric FinFET designed to have different drive currents from drain to source and source to drain. This device is specifically designed to enhance the performance of STT-MRAM cells, which utilize an MTJ for data storage. The MTJ has an asymmetric bidirectional write current, which can be exploited to achieve power savings by using an asymmetric select/access device in the STT-MRAM bit-cell. Furthermore, the simulation and process emulation conducted in this chapter shows that the proposed device provides better asymmetry and easy compatibility with the existing FinFET fabrication flow, respectively. An additional advantage of this design is its lower gate capacitance compared to existing symmetric and asymmetric FinFET architectures. The reduced gate capacitance further contributes to lowering the write-line capacitance in STT-MRAM cells, thereby enhancing overall performance and energy efficiency.