Chapter: 2

Expandable L_nC_{2n-2} Impedance Network Based DC-DC Converter

2.1. Introduction

As discussed earlier, renewable energy resources are gaining popularity due to their potential to provide green and cost-effective solutions to the global power crisis. However, the low voltage output of these energy sources remains a significant challenge. To align their voltage levels with utility requirements, power electronic converters such as DC-DC, DC-AC, or hybrid converters are essential. Despite advancements, there is still room for improvement in terms of cost, size, voltage gain, and overall performance.

DC-DC converters play a vital role in stepping up the low voltage output of renewable sources to the required levels while enabling MPP tracking. Traditional DC-DC converters face challenges like low voltage gain and efficiency losses. While isolated converters provide flexible voltage gain through transformer-based designs, they suffer from bulkiness, high cost, and lower efficiency. Non-isolated converters, on the other hand, often require additional components to achieve high voltage gain, leading to increased losses and complexity.

To address these challenges, a step-up inductor-capacitor-based expandable DC-DC converter is proposed. This *n*-stage expandable design enhances voltage gain and reliability by allowing faulty modules to be bypassed without interrupting operation. Despite increased device count, the expandable architecture ensures robustness and ease of maintenance. The proposed L_nC_{2n-2} topology offers high voltage gain with a minimal number of components and scalable stages, making it well-suited for renewable energy applications, particularly solar PV systems.

2.2. Expandable L_nC_{2n-2} Network-based Converter

The proposed L_nC_{2n-2} expandable topology is designed as an expandable multi-stage DC-DC converter consisting of n stages. At each stage, denoted as the Kth stage, incrementally enhances the voltage gain of the system. As depicted in Fig. 2.1, adding each new stage leads to the introduction of each cell, which modifies the voltage gain by a factor of $1/(1-nd)$, where d represents the duty cycle. This systematic gain adjustment makes the topology highly adaptable for high-voltage applications.

Each K^{th} stage in the topology comprises a simple yet effective configuration of one inductor, two capacitors, and one diode. The total component count for the entire topology is determined by the number of stages (n) and follows this generalized formula for the proposed expandable topology:

- Inductors: n
- Diodes: n
- Capacitors: $(2n-2) + 1$
- Switches: 1

For a clearer understanding, n=3 is considered, i.e., the L_3C_4 expandable topology. This configuration includes three inductors, three diodes, six capacitors, and one switch, as shown in Fig. 2.2. The expandable approach not only simplifies the design but also ensures scalability and ease of maintenance.

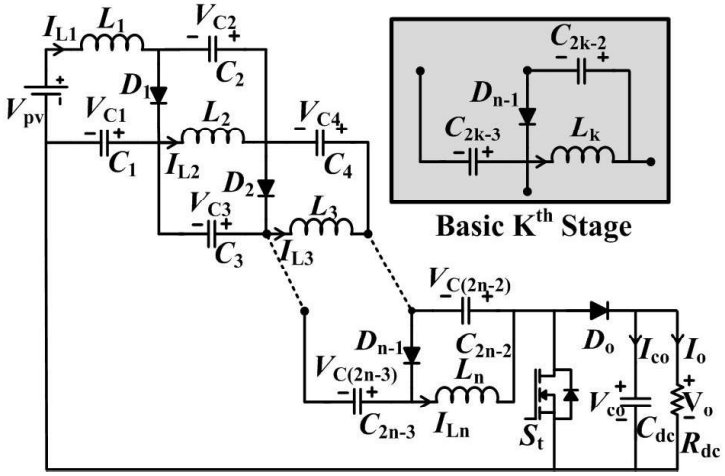


Fig. 2.1 Proposed L_nC_{2n-2} expandable network-based converter.

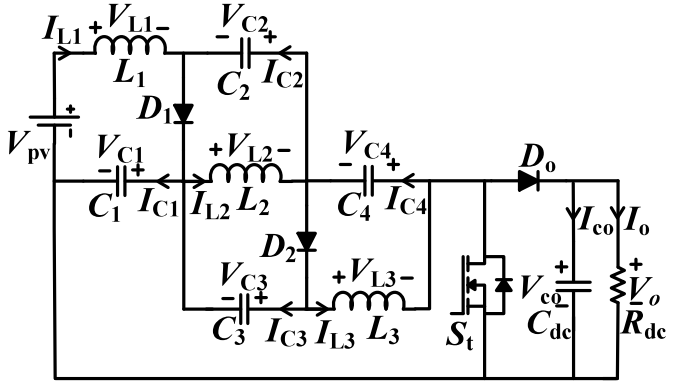


Fig. 2.2 Proposed L_3C_4 expandable network-based converter for n=3.

2.3. Operating Modes

The operating modes of the proposed converter are classified into two primary categories: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). Each mode offers distinct advantages and operational characteristics, making the topology versatile for various renewable energy applications.

2.3.1. Continuous Conduction Mode of Operation

The Continuous Conduction Mode (CCM) operation defines the period when the inductor current remains continuous without fully discharging, ensuring stable energy transfer and reduced current ripple. Within one switching cycle (T_s) and a duty ratio of d, the CCM mode consists of two distinct switching states: the dT_s switching state, where the switch remains on and the inductors charge, and the $(1\text{-}d)T_s$ switching state, where the switch is off and the inductors discharge. These states are critical in shaping the converter's performance and voltage gain characteristics, as detailed below.

DTs Switching State: As illustrated in Fig. 2.3(a), when the switch S_t is turned on for a duration of dT_s, all diodes become reverse-biased, preventing current flow through them. During this interval, inductor L_1 is charged via the path formed by the input voltage V_{pv}, capacitor C_2, and capacitor C_4. Similarly, inductor L_2 is charged through capacitors C_1 and C_4, while the combination of inductor L_3 and capacitor C_4 is charged through C_1 and C_3. The equations governing the dT_s state are provided in equation (2.1), and the corresponding waveform is depicted in Fig. 2.4.

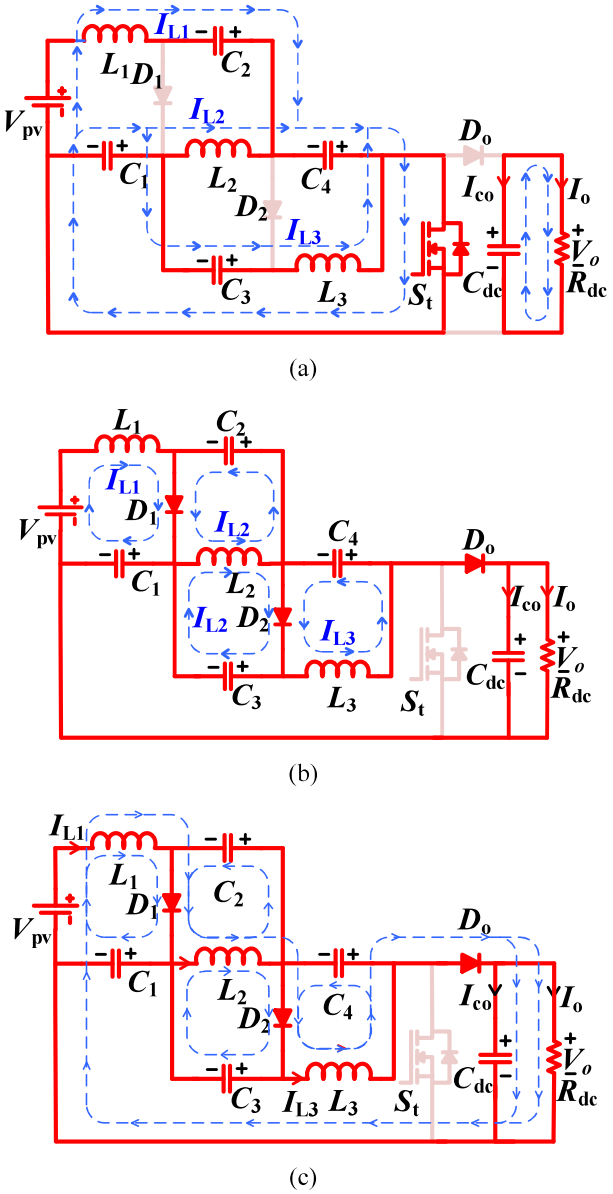


Fig 2.3. Operating Modes of Proposed L_3C_4 expandable DC-DC converter. (b) dT_s switching state of CCM (c) T_{buffer} state of CCM.

(1-*d*)T_s Switching State: When the switch S_t turns off for the (1-*d*)T_s interval, all diodes become forward-biased. There is a brief transient period, which is negligible, during

$$\left.\begin{aligned} V_{L1} &= V_{PV} + V_{C2} + V_{C4} \\ V_{L2} &= V_{C1} + V_{C4} \\ V_{L3} &= V_{C1} + V_{C3} \\ I_{C1} &= I_{L2} + I_{L3} \\ I_{C2} &= -(I_{L2} + I_{L3}) \\ I_{C3} &= -I_{L3} \\ I_{C4} &= -(I_{L1} + I_{L3}) \\ I_{Cdc} &= -I_0 \end{aligned}\right\} \quad (2.1)$$

$$\left.\begin{aligned} V_{L1} &= V_{PV} - V_{C1} \\ V_{L2} &= -V_{C2} = V_{C3} \\ V_{L3} &= -V_{C4} \\ I_{C1} &= I_{D1} + I_{D2} - (I_{L2} + I_{L3}) \\ I_{C2} &= I_{D1} - I_{L1} \\ I_{C3} &= I_{D2} - I_{L3} \\ I_{C4} &= I_{D1} + I_{D2} - (I_{L1} + I_{L2}) \\ I_{Cdc} &= (I_{L1} + I_{L2} + I_{L3}) - (I_{D1} + I_{D2}) - I_0 \end{aligned}\right\} \quad (2.2)$$

which the discharged capacitors recharge, as illustrated in Fig. 2.3(b). For the remainder of this interval, all the inductors collectively supply power to the load, as depicted in Fig. 2.3(c). The equations governing the (1-d)T_s state are provided in equation (2.2), and the corresponding waveform is shown in Fig. 2.4.

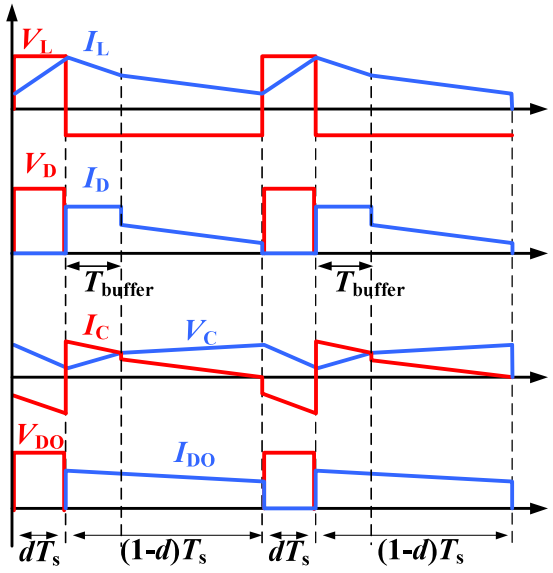


Fig. 2.4. Operating mode waveform for CCM.

The voltage across the capacitors in the L_3C_4 expandable topology is determined using the principle of volt-second balance over a complete switching period T_s. This balance is applied during the dT_s and (1-d)T_s intervals to derive the steady-state equations, which are expressed as follows:

$$V_{C1} = \frac{(1-2d)}{(1-3d)} V_{PV} = \frac{V_0 + 2V_{PV}}{3} \quad (2.3)$$

$$V_{C2} = V_{C3} = V_{C4} = \frac{dV_{PV}}{(1-3d)} = \frac{V_0 - V_{PV}}{3} \quad (2.4)$$

The peak dc-link voltage across the converter is:

$$V_O = V_{C1} + V_{C2} + V_{C4} = V_{C1} + V_{C3} + V_{C4} = \frac{1}{(1-3d)} V_{PV} \quad (2.5)$$

Therefore, the DC voltage gain for L_3C_4 expandable topology in CCM can be expressed as:

$$G_{CCM} = \frac{V_O}{V_{PV}} = \frac{1}{(1-3d)} \quad (2.6)$$

The maximum blocking voltage across the diodes and switches is:

$$V_{D1} = V_{D2} = V_{D0} = \frac{1}{(1-3D)} V_{PV} \quad (2.7)$$

$$V_{St} = \frac{1}{(1-3D)} V_{PV} \quad (2.8)$$

Similarly, by current second balance across the capacitors C_1, C_2, C_3, and C_4 the steady state current equations can be given by:

$$I_{L1} = I_{L2} = I_{L3} = I_{pv} \quad (2.9)$$

Further, by power balancing the input and output power:

$$I_{pv} = \frac{I_O}{(1-3d)} \quad (2.10)$$

2.3.2. Discontinuous Mode of Operation

Similar to the CCM, the L_3C_4 expandable topology contains an extra state other than that of the CCM operations. In this state (1-d), the T_s switching state is split into two states, i.e., the conducting state (d_1T_s) and the non-conducting state (d_2T_s). During the switching instant 0 to d_1T_s when the S_t is on, all three inductors get charged, and their current rises from zero to their peak value further during the switching instant d_1T_s to (1- d_1-d_2)T_s inductor's currents drops from its maximum value to zero, and for rest of the interval, i.e., d_2T_s inductor currents remains zero, diodes get reversed biased and capacitor C_{dc} supplies load. The circuit operation is shown in Fig. 2.5, and its waveform

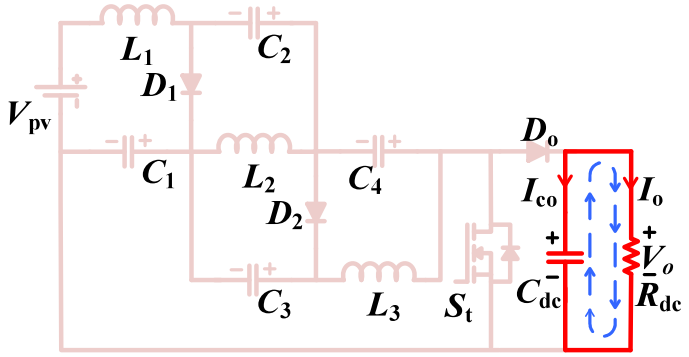


Fig. 2.5. Converters DCM Operation.

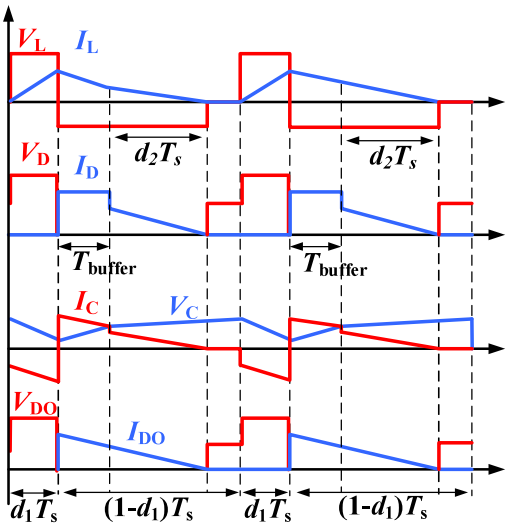


Fig. 2.6. Operating waveform under DCM.

is shown in Fig. 2.6. The average inductor current of the L_3C_4 expandable topology can be given as:

$$< I_L > = \frac{V_0^2}{RV_{PV}} = \frac{1}{2}\left[\frac{(V_{PV}+2V_{C2})(d_1(d_1+d_2))T_S}{L}\right] \tag{2.9}$$

By solving the above equations for the DCM voltage gain for L_3C_4 expandable topology can be given by:

$$G_{DCM} = \frac{V_O}{V_{PV}} = \frac{\left(1+\frac{2d_1^2}{K}\right)+\sqrt{\left(1+\frac{2d_1^2}{K}\right)^2+\frac{4d_1^2}{K}}}{2} \tag{2.10}$$

Where K is the inductor time constant, which is dependent on inductor L, load resistance R_{dc}, and time constant T_s and is given by:

$$K = \frac{2L}{R_{dc}\ T_S} \tag{2.11}$$

2.3.3. Critical Boundary Condition

Critical boundary condition represents the transition between continuous and discontinuous mode operations, with a subtle distinction — in this mode, the current through the inductor barely maintains conduction. The boundary condition for this state can be expressed as:

$$I_L = \frac{\Delta I_L}{2} \tag{2.12}$$

To solve this, the critical inductance (L_{Cr}) condition can be obtained as:

$$L_{Cr} = \frac{d_1*(1-d_1)*(1-3d_1)*R_{dc}*T_S}{2} \quad (2.13)$$

Further critical inductor time constant (K_{Cr}) is defined as:

$$K_{Cr} = d_1 * (1 - d_1) * (1 - 3d_1) \quad (2.14)$$

2.3.4. Generalised Formula for *n* Stages

Based on the structure of the proposed expandable topology for *n* stages. The following generalized equations for n cells can be obtained as:

$$V_{C1} = \frac{(1-(n-1)d)}{(1-nd)} V_{pv} \quad (2.15)$$

$$V_{C2} = V_{C3} \ldots\ldots\ldots\ldots = V_{C(2n-2)} = \frac{d}{(1-nd)} V_{pv} \quad (2.16)$$

$$V_{D0} = V_{D1} \ldots\ldots\ldots = V_{Dn} = \frac{1}{(1-nd)} V_{pv} \quad (2.17)$$

$$V_{St} = \frac{1}{(1-nd)} V_{pv} \quad (2.18)$$

$$G_{CCM} = \frac{V_O}{V_{PV}} = \frac{1}{(1-nd)} \quad (2.19)$$

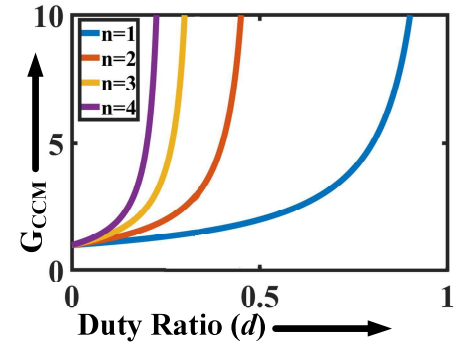
Additionally, Fig. 2.7(a) and Fig 2.7(b) illustrate the voltage gain characteristics for "*n*" basic cells for CCM and DCM, respectively. Where for DCM "K=0.028", and the output voltage gain for the DCM can be expressed as:

$$G_{DCM} = \frac{\left(1 + \frac{(n-1)d_1^2}{K}\right) + \sqrt{\left(1 + \frac{(n-1)d_1^2}{K}\right)^2 + \frac{4d_1^2}{K}}}{2} \quad (2.20)$$

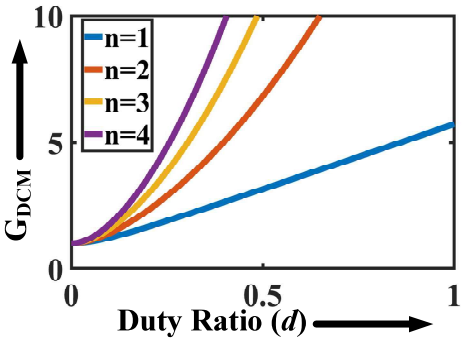
Similarly, The L_{Cr} and K_{Cr} for *n* basic cells are given below, and for different values of n, the CCM-DCM region along with *K* and *d* is expressed in Fig. 2.8. Where the inside region represents the DCM operation for different values of *n*. On the other hand, the outer region represents the CCM operation, corresponding to different values of *n* and is represented as:

$$L_{Cr} = \frac{d_1(1-d_1)(1-nd_1)R_{dc}T_S}{2} \quad (2.21)$$

$$K_{Cr} = d_1(1 - d_1)(1 - nd_1) \quad (2.22)$$



(a)



(b)

Fig. 2.7 Voltage gain of expandable DC-DC converter for different *n* (a) CCM (b) DCM.

2.4. Design of Passive Components

The proposed expandable DC-DC converter is composed of a L_nC_{2n-2} network, as discussed earlier. The converter is verified for n=3 i.e., L_3C_4 network. Thus, the total converter is composed of three inductors, four capacitors, and one filter capacitance.

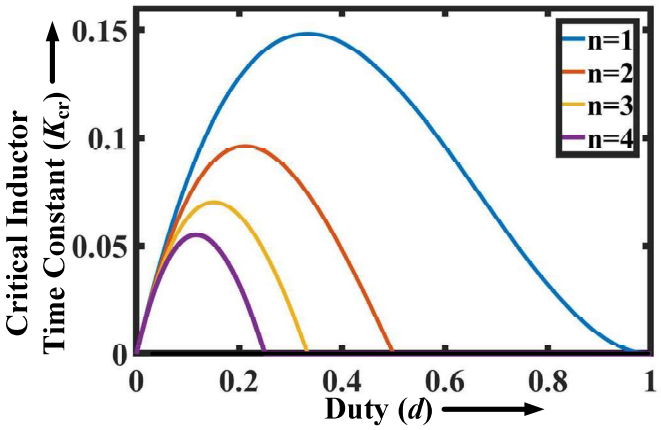


Fig.2.8 Critical boundary condition between CCM and DCM.

For n = 3 stages, since the current through each inductor remains constant, the design of the inductors is based on the ripple factor (%RF), duty (d), switching frequency (f_s), and the current through the inductor (I_{Ln}). The detailed design for this configuration is as follows:

$$L_1 = L_2 = L_3 = \frac{d(1-d)V_{pv}}{f_s(1-3d)(\%RF)I_{L1}} \tag{2.23}$$

Similarly, the inductor for n stage expandable converter can be calculated by:

$$L_1 = L_2 \ldots\ldots\ldots = L_n = \frac{d(1-d)V_{pv}}{f_s(1-nd)(\%RF)I_{L1}} \tag{2.23}$$

Capacitors of the L_nC_{2n-2} network are designed by considering the ripple factor. The average current flowing through the C_1, C_2, C_3, and C_4 in shoot-through interval I_{cn}. Considering the ripple factor of 1%, the C_1, C_2, C_3, and C_4 values of the converter can be designed using the equation:

$$I_{Cn} = C_n \frac{dV}{dt} \tag{2.24}$$

$$I_{Cn} = C_n \frac{dV}{d*T_s} = C_n \frac{dV*f_{sw}}{d} \tag{2.25}$$

Where d is the duty ratio, f_{sw} is the frequency, dV is the ripple voltage, and T_s is the switching time period.

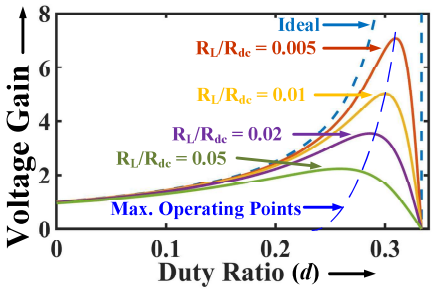
2.5. Analysis of Proposed Converter Considering Non-Ideality

P_{Cu} and P_L represent the conduction losses of the capacitors and inductors, respectively. Meanwhile, $P_{S,R}$ refers to the conduction loss attributed to S_t, while $P_{S,S}$ denotes the switching loss of S_t. $P_{D,R}$ accounts for the conduction loss of the diode, and $P_{D,F}$ pertains to the loss resulting from the diode's forward voltage drop.

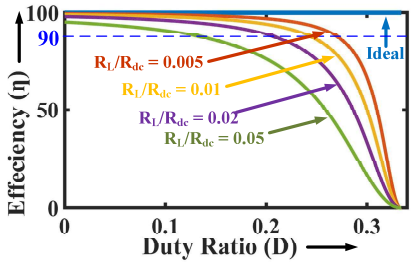
Fig. 2.9. Inductor with its parasitic value.

$$P_{LOSS} = P_L + P_{Cu} + P_{S,R} + P_{S,S} + P_{D,R} + P_{D,F} \tag{2.26}$$

After neglecting the switching losses of diodes and Mosfet and ESR of the capacitance, as it is very minimal, only the P_L is significant and is considered for Voltage gain. For the exact gain calculation of the gain, the parasitic resistance of each Inductance (R_L/n)



(a)



(b)

Fig. 2.10. Voltage and Efficiency curve (a) Variation of (G_{Real}) by considering R_{L}. (b) Variation of efficiency (η) by considering R_{L} with the variation of duty ratio (d).

shown in Fig. 2.9 is considered, which is responsible for the total voltage drop in the circuit, i.e., for n inductors, the total resistance would be R_{L}. By applying KVL to the circuit, the voltage gain of the proposed circuit (G_{Real}) can be expressed as (2.27) while taking into account the load resistance (R_{L}). Fig. 2.10(a) illustrates the voltage gain characteristics of the proposed circuit with varying d for different values of R_{L}. Based on Fig. 2.10(a) and Fig. 2.10(b), the maximum operating point can be determined for practical applications, aiding in the converter design.

$$(G_{Real})_3 = \frac{V_o}{V_{PV}} = \frac{1}{(1-3d)}\left(\frac{1}{1+\left(\frac{R_L}{(1-3d)^2 R_{dc}}\right)}\right) \tag{2.27}$$

Further, the G_{Real} for n cells can be extended as:

$$(G_{Real})_3 = \frac{V_o}{V_{PV}} = \frac{1}{(1-nd)}\left(\frac{1}{1+\left(\frac{R_L}{(1-nd)^2 R_{dc}}\right)}\right) \tag{2.28}$$

The efficiency for L_3C_4 expandable topology can be represented as (29), and its characteristics by considering the different values of R_{L} are shown in Fig. 2.8(b):

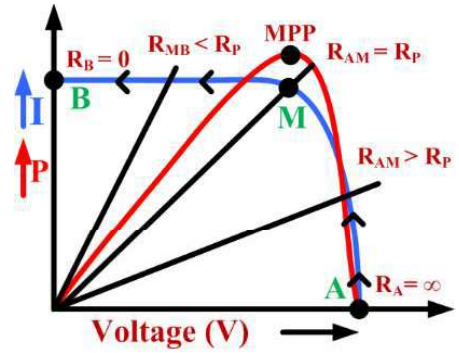
$$\eta_3 = \frac{1}{\left(1+\left(\frac{R_L}{(1-3d)^2 R_{dc}}\right)\right)} \quad (2.29)$$

Since we have n stages, the formula for losses with respect to n stages can be represented as:

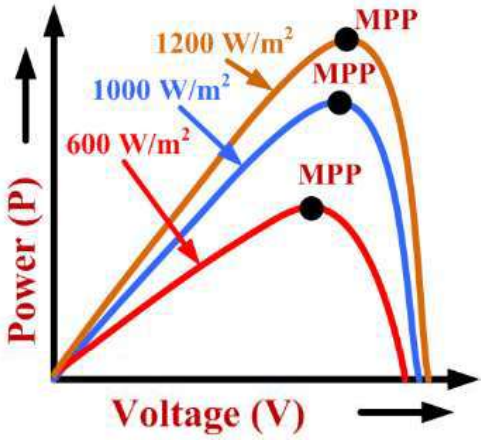
$$\eta_3 = \frac{1}{\left(1+\left(\frac{R_L}{(1-nd)^2 R_{dc}}\right)\right)} \quad (2.29)$$

2.6. MPPT Operation

The PV panel operates on the right-hand side of the MPP in the PV characteristics when load resistance (R_{dc}) is greater than the equivalent PV resistance at MPP (R_M). Similarly, the operating point is at the left when R_{dc} is less than R_M. In order to fully use the solar power from the PV panel, equivalent load resistance when referred to the PV side must be equal to R_M at a specific irradiance and temperature as shown in Fig. 2.11(a) by power balance, R_M for L_3C_4 expandable DC-DC converter be obtained as:



(a)



(b)

Fig. 2.11. Solar PV characteristics (a) Variation of equivalent PV resistance with PV and IVcurve (b) Variation of MPP with solar irradiance.

$$R_M = R_{dc}*(1-3d)^2 \quad (2.30)$$

Further, the formula can be extended for n stages as:

$$R_M = R_{dc}*(1-nd)^2 \quad (2.31)$$

With the variation of Irradiance and temperature, MPP changes its position, as shown in Fig. 2.11(b). Therefore, to track MPP, a traditional INC-based algorithm is used.

2.7. Comparative Analysis of Expandable DC-DC converters

The proposed L_3C_4 expandable topology has been compared with several existing modular converters based on various parameters, including gain characteristics, switch count, device count, voltage and current stress on devices and passive components, semiconductor device count, control algorithm, overall device count, efficiency, volume, and cost, as summarized in Table 2.1.

By examining Table 2.1 and comparing it with existing modular converters, It can be seen that the proposed topology uses a single input source, whereas [35] and [36] utilize 'n' input sources. The proposed topology and [34] both require only one controlled switch, meaning that only one gate driver is needed, which is the minimum among all

TABLE 2.1

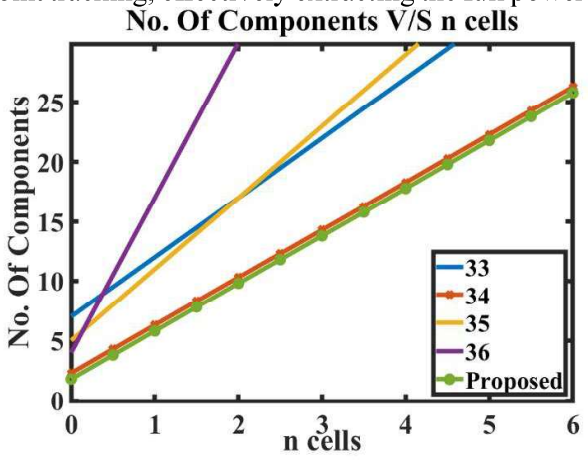
PERFORMANCE COMPARISON OF L_NC_{2N-2} NETWORK BASES DC-DC CONVERTER

Parameter	[33]	[34]	[35]	[36]	Proposed
Input Source	1	1	n	n	1
Switch	n+2	1	n+1	2n+2	1
Gate Driver	n+2	1	n+1	2n+2	1
Diode	2n	2(n-1)+1	n+1	2n-2	n
Capacitor	1	n	n+1	2n	2n-1
Inductor	n+2	n	n+1	2n	n
Control Algorithm	-	-	-	-	Incremental Conductance
Output/Input Voltage Ratio	$\frac{1+(n+1)D}{1-D}$	$\frac{1}{[1-D]^{n+2}}$	$\frac{n(1-D)+D}{[1-D]^2}$	$\frac{1+n-D}{[1-D]^2}$	$\frac{1}{1-nD}$
No. of Switches + Diodes	3n+2	2n	2n+2	4n	n+1
Total Number of Required Components	5n+8	4n+2	6n+5	11n+2	4n+2
Efficiency	94%	91%	-	88%	96%
Size/Volume	Moderate	Low	Moderate	High	Low
Cost	Moderate	Low	Moderate	High	Low

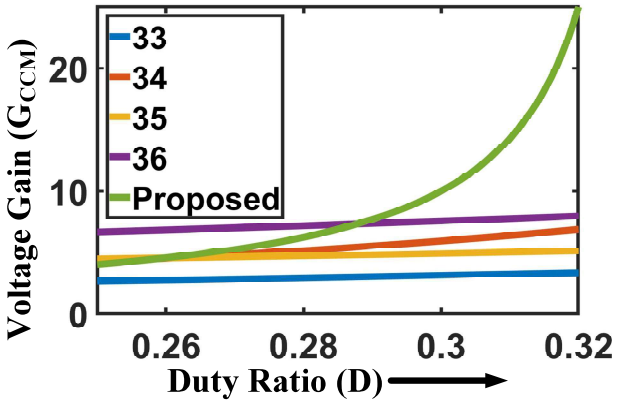
the topologies. The proposed topology also requires 'n' diodes and inductors, which are fewer than the other converters. The number of capacitors required in the proposed topology is '$2n$-1'.

The semiconductor device count as a function of the number of cells (n) is plotted, revealing that the proposed converter utilizes fewer semiconductor devices compared to other existing converters. Additionally, the total number of components as a function of n cells is illustrated in Fig. 2.12(a). Although the converter presented in [35] exhibits similar characteristics. however, the proposed topology not only maintains a lower device count but also offers higher gain, as illustrated in Fig. 2.12(b).

The proposed topology stands out as the only one tested for photovoltaic (PV) applications by implementing the incremental conductance algorithm to achieve maximum power point tracking, effectively extracting the full power from the PV panel.



(a)



(b)

Fig. 2.12. Comparative analysis (a) DC voltage gain comparison for L_3C_4 expandable topology. (b) total number of components with respect to n Cells.

In contrast, none of the existing modular converters have only been tested and realized for PV applications. Finally, the efficiency of the converter is calculated to be 92%, which is moderate compared to other topologies.

Thus, it can be stated that overall, the proposed topology uses the least number of components, making it more compact and cost-effective than another existing modular converter. The proposed converter achieves maximum gain at a lower duty cycle (d) while utilizing a minimum number of semiconductor devices and components.

2.8. Experimental Results

This section provides a comprehensive presentation of the experimental results obtained for the L_3C_4 expandable converter, developed and tested using a 300W laboratory prototype. The primary objective of these experiments was to thoroughly validate the converter's performance under different operating modes, including Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), and Maximum Power Point Tracking (MPPT) operation. By evaluating the converter's response in these distinct modes, the experimental analysis aims to establish its efficiency, stability, and overall suitability for practical solar PV applications.

The experimental setup was carefully designed to replicate real-world operating conditions and ensure precise performance assessment. A Chroma 62100H-600S solar

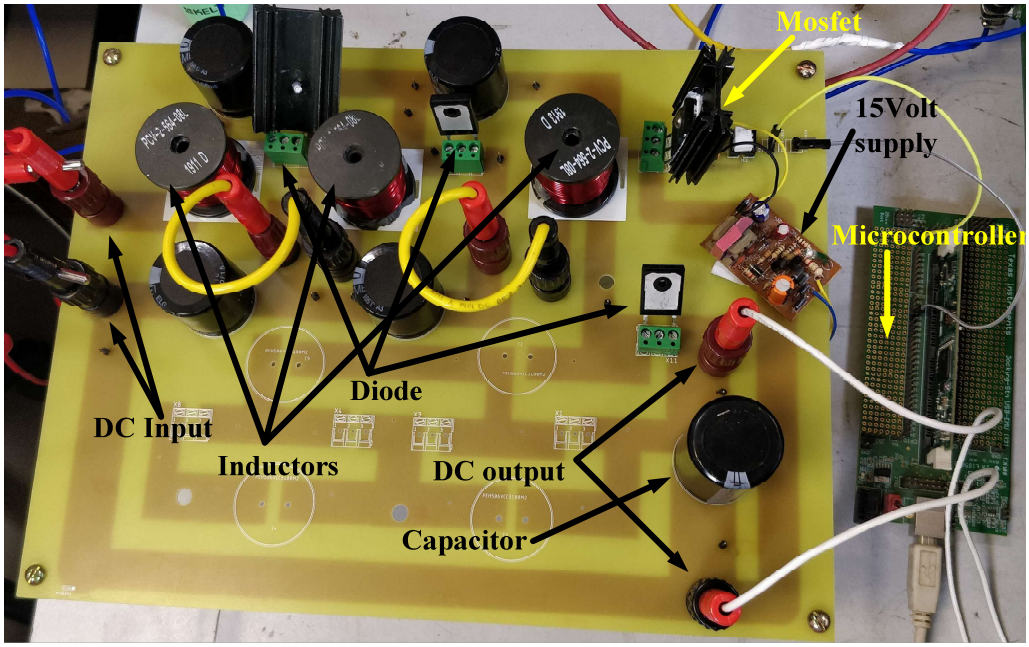


Fig. 2.13. Photograph of the hardware setup.

TABLE 2.2

DESIGN SPECIFICATION OF L_NC_{2N-2} NETWORK BASED DC-DC CONVERTER

Switch (S_t)	NTHL082N65S3F
Diode (D_0, D_1, D_2)	RURG8060
Capacitor (C_1, C_2, C_3, C_4)	180uF
Capacitor (C_o)	470uF
Inductor (L_1, L_2, L_3)	560 uH
Frequency (f)	50kHz
Gate Driver	FOD3184
Microcontroller	TMS320F28335

PV emulator was employed to simulate varying solar irradiation and temperature profiles, providing a highly controllable and realistic input source. The control of the system was facilitated using the Texas Instruments DSP F28335 Delfino Experimenter's Kit, known for its high-speed processing capabilities and suitability for real-time control applications in power electronics.

For a clearer understanding of the physical implementation, Fig. 2.13 presents a photograph of the 300W prototype used in the laboratory. This prototype was constructed with careful attention to component selection and layout, ensuring minimal parasitics and efficient thermal management. Additionally, the key parameters considered for validating the proposed converter topology, including component ratings, control specifications, and operating conditions, are systematically summarized in Table 2.2.

2.8.1. CCM Operation

Fig. 2.14(a) presents the input and output characteristics of the proposed system. With a DC input voltage of Vpv = 60V, a duty cycle d = 0.17, and a load resistance R_{dc} = 50 ohms, the input current I_{pv}, which is equal to the inductor current I_{L1}, is measured at 5A. This results in an output voltage of 120V and an output current of 2.4A. Furthermore, the inductor currents I_{L1} and I_{L2} both measure 5A, which is consistent with the theoretical predictions derived from Eq. (2.9), validating the proper operation of the system.

Fig. 2.14(b) illustrates the capacitor voltage distribution, where the voltages across capacitors C_1 and C_2 are measured as V_{C1} = 78V and V_{C2} = 22V, respectively. These

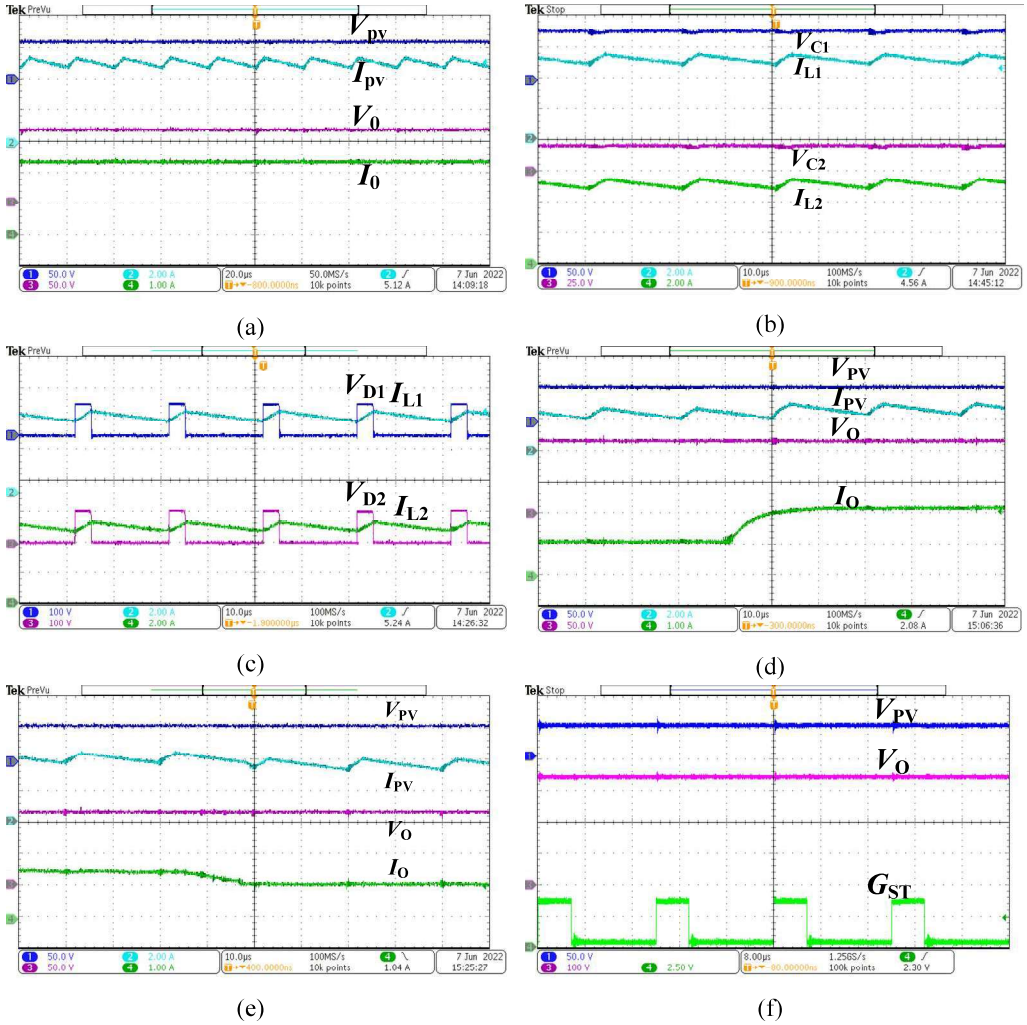


Fig. 2.12. Experimental result of L_3C_4 modular converter in CCM (a) Input and output voltage and current, (b) Charging and discharging of capacitor voltage and inductor current, (c) Stress across the diodes D_1 and D_2. (d) Dynamic load increase, (e) Dynamic load decrease. (f) High gain characteristic at D= 0.28.

values align closely with the calculations provided in Eq. (2.3) and Eq. (2.4), further confirming the accuracy of the proposed theoretical model.

Fig. 2.14(c) highlights the voltage stress experienced by the diodes D_1 and D_2. The maximum blocking voltage for both diodes reaches 120V, which corresponds exactly to the output voltage V_o. This behaviour is consistent with the predictions of Eq. (2.7), demonstrating the converter's expected performance in handling voltage stress.

Fig. 2.14(d), shows the system's dynamic response to increasing load is depicted. As the load increases, the output current Io rises proportionally. To maintain power balance within the system, the input current increases accordingly, ensuring consistent and

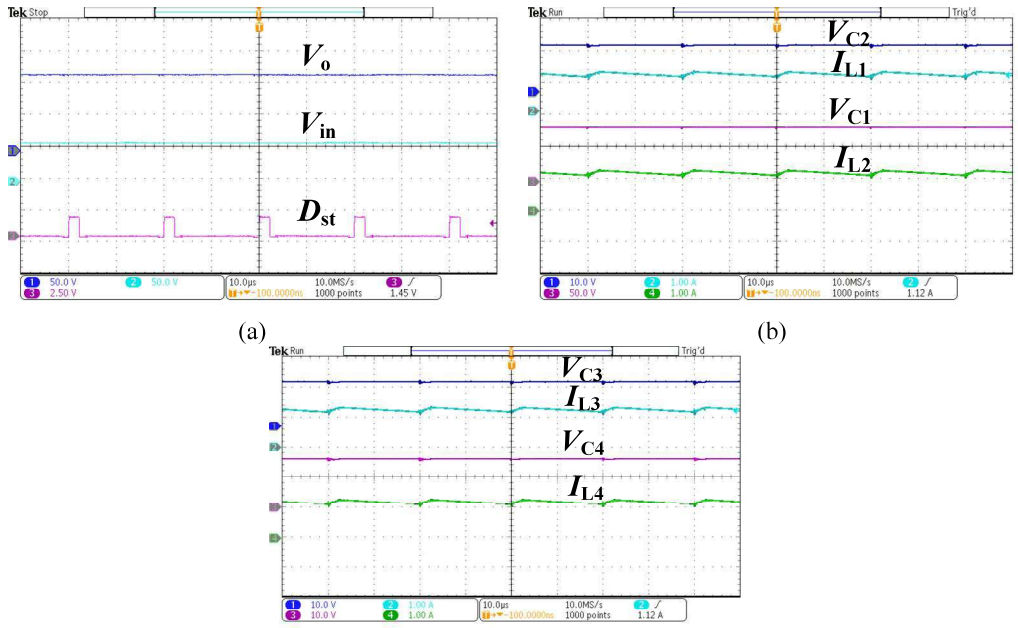


Fig. 2.15. Experimental result of L_4C_6 modular converter in CCM (a) Voltage gain for n=4 cells. (b) Voltage and current stress across I_{L1}, I_{L2}, V_{C1} and V_{C2} (c) Voltage and current stress across I_{L3}, I_{L4}, V_{C3} and V_{C4}.

stable voltage regulation. Conversely, Fig. 2.14(e) shows the system's behaviour under decreasing load conditions. When the load reduces dynamically, the output current decreases gradually due to the presence of a large filter capacitance, which helps in stabilizing the voltage output. Despite the reduction in current, the output voltage remains stable, and the input current decreases slowly to maintain power balance, demonstrating the system's robustness in load regulation.

Fig. 2.14(f) showcases the system's high voltage gain capability. With a small duty cycle of 0.28, the L_3C_4 modular topology achieves an impressive voltage gain of 6.25 times the input voltage. This significant boost in voltage output highlights the efficiency and effectiveness of the proposed converter design.

Moreover, to validate the scalability and versatility of the proposed converter, the results for an extended configuration with n=4 cells are presented in Fig. 2.15(a), 2.15(b), and 2.15(c). In Fig. 2.15(a), the L_4C_6 network-based converter achieves an output voltage of 120V with a reduced duty cycle of 0.125, demonstrating efficient voltage boosting even with an increased number of cells.

Fig. 2.15(b) depicts the voltage distribution across the capacitors for the n=4 configuration. The voltage across capacitor C_1 is measured at V_{C1} = 75V, while the

voltages across capacitors C_2, C_3, and C_4 are uniform, with $V_{C2} = V_{C3} = V_{C4} = 15V$. These results are consistent with the theoretical values predicted by Eq. (2.15) and Eq. (2.16), as further illustrated in Fig. 2.15(b) and 2.15(c). Finally, the inductor currents in the L_4C_6 network exhibit uniformity, with $I_{L1} = I_{L2} = I_{L3} = I_{L4} = 1.2A$. This equal current distribution across the inductors ensures balanced operation and efficient energy transfer, minimizing potential losses and confirming the reliability of the proposed converter design even with higher cell counts. These results collectively demonstrate the scalability, efficiency, and robustness of the proposed system.

2.8.2. DCM Operation

When the load decreases, the current flowing through the converter becomes discontinuous, causing the system to enter Discontinuous Conduction Mode (DCM). Under these conditions, with the photovoltaic input voltage (V_{pv}) set at 55V, a duty cycle (d) of 0.17, and a load resistance (R_{dc}) of 2000 ohms, the converter draws a peak input current of 1.1A. This particular configuration results in an output voltage (V_O) of 185V, which aligns closely with the theoretical prediction provided in Equation (2.20) and is clearly depicted in Fig. 2.16(a).

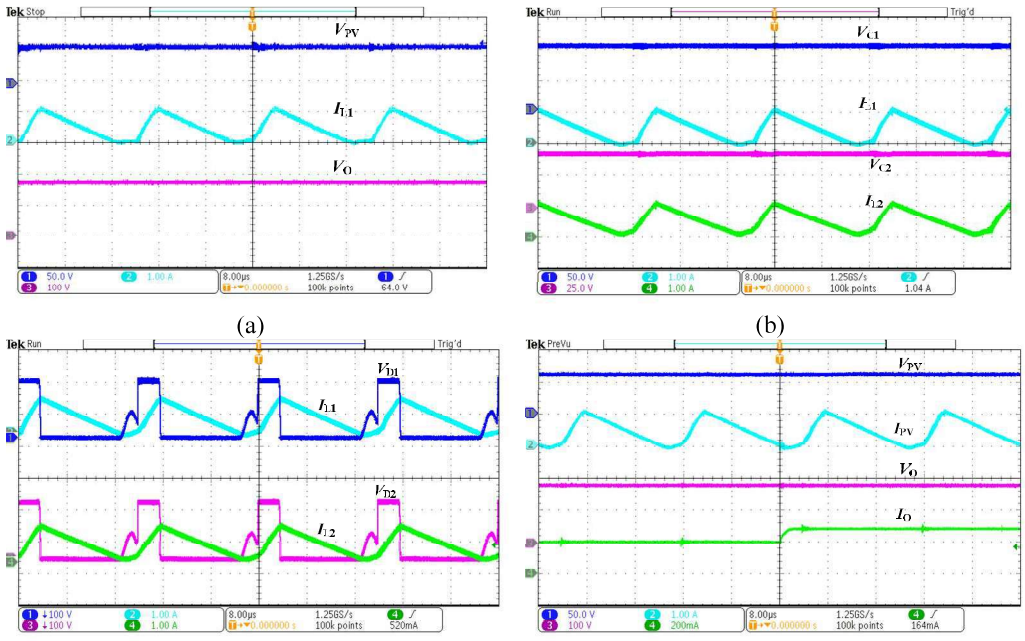


Fig. 2.16. Experimental result of L_3C_4 modular converter in DCM, (a) Input and output voltage and current. (b) Charging and discharging of capacitor voltage and inductor current. (c) Stress across the diodes D_1 and D_2. (d) Dynamic load increase.

Fig. 2.16(b) provides a closer look at the voltage behaviour across capacitors V_{C1} and V_{C2}, along with the current waveforms of inductors I_{L1} and I_{L2}. These waveforms reveal how the reduced load directly impacts the capacitor voltages and inductor currents, offering a clear illustration of the system's behaviour when operating under DCM conditions.

In Fig. 2.16(c), the maximum blocking voltages across diodes D_1 and D_2 are shown alongside the inductor currents I_{L1} and I_{L2}. Despite the converter's operation in DCM, the blocking voltages across the diodes remain stable. This stability ensures that the diodes can withstand voltage stresses without any performance degradation, as demonstrated by the behaviour seen in curve 2.6.

Finally, Fig. 2.16(d) captures the converter's dynamic response to a slight increase in load while still in DCM. Since this load variation is minimal—only in the range of milliamperes—the output voltage remains nearly unchanged, maintaining excellent stability. Moreover, the converter's voltage gain in DCM is significantly higher compared to its performance in Continuous Conduction Mode (CCM), as evidenced by the trend illustrated in Fig. 2.7.

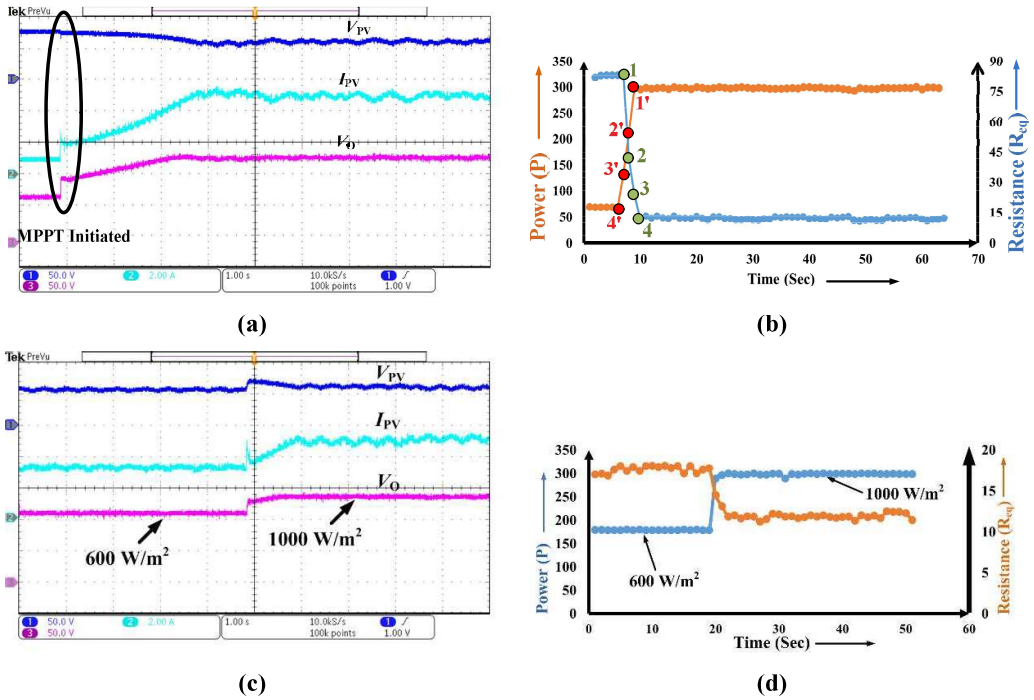


Fig. 2.17. Variation of R_{eq} with MPPT tracking (c) MPPT tracking with the variation of irradiance (d) Variation and tracking of R_{eq} with the change of irradiance.

2.8.3. MPPT Operation

The effectiveness of the MPPT operation is clearly demonstrated in Fig. 2.17(a), where the converter swiftly tracks the Maximum Power Point (MPP) within just 3 seconds. This rapid response highlights the efficiency of the incremental conductance algorithm, which quickly adjusts the operating point to ensure maximum power extraction from the photovoltaic (PV) system. Such fast-tracking capability is crucial for maintaining optimal performance, especially under varying environmental conditions.

Further insights come from the experimental tracking data gathered from the soft panel, as depicted in Fig. 2.17(b). This data reveals an important system behaviour: as soon as the MPP is reached, the equivalent resistance (R_{eq}) drops and aligns with the resistance at the MPP. This dynamic adjustment of parameters ensures that the system continuously operates at peak efficiency, confirming the theoretical expectations discussed earlier in Fig. 2.9(a).

The system's ability to maintain efficient tracking even under changing solar conditions is illustrated in Fig. 2.17(c). Here, as the solar irradiance increases from 600 W/m² to 1000 W/m², the converter adapts in real-time, maintaining its ability to track the MPP without delay. This adaptability is crucial for real-world PV applications, where irradiance levels often fluctuate.

Additionally, Fig. 2.17(d) sheds light on the interplay between power, equivalent resistance ($R_{eq)}$, and solar irradiance. As irradiance changes, the resistance associated with the MPP (R_M) also shifts, a relationship previously explained in Fig. 2.9(b). Despite these variations, the converter swiftly responds, achieving the new MPP within just 2 seconds, as illustrated in Fig. 2.17(c) and 2.17(d). This quick adaptation underscores the robustness and reliability of the system, ensuring that maximum power is consistently harnessed from the solar panels even under dynamic environmental conditions.

2.9. Summary

In this chapter, the development of a novel L_nC_{2n-2} network-based DC-DC converter, designed specifically for the efficient integration of low-voltage photovoltaic (PV) panels. One of the key strengths of this converter lies in its impedance network, which is highly effective in boosting the low-voltage input from the PV panel to match the

required voltage level for downstream applications. This makes it particularly well-suited for renewable energy systems where voltage amplification is crucial.

A significant advantage of the proposed topology is its modular and scalable design. The impedance network can be expanded up to 'n' stages, allowing for flexibility in meeting varying power and voltage requirements. Despite its scalability, the converter achieves this with a minimal number of components compared to other existing topologies, which not only reduces cost but also simplifies the overall design and assembly process.

Another standout feature of this converter is its simple control mechanism. The entire topology can be effectively regulated using a single switch, making the control strategy straightforward and highly efficient. This reduces the complexity typically associated with multi-switch configurations and minimizes the potential for control-related errors.

The impedance network-based structure also brings inherent benefits, such as excellent electromagnetic interference (EMI) immunity. This ensures stable and reliable operation even in environments with significant electrical noise. Additionally, the modular nature of the design means that in the event of a fault, any defective cell can be easily replaced without disrupting the entire system, enhancing the converter's maintainability and longevity.

The performance and reliability of the proposed converter have been rigorously verified through extensive testing under different operational modes: continuous conduction mode (CCM), discontinuous conduction mode (DCM), and maximum power point tracking (MPPT) mode. These tests confirm the converter's capability to operate efficiently and adaptively across a range of conditions, further validating its suitability for PV integration and other renewable energy applications.

The proposed converter, while innovative, remains a DC-DC converter. However, the growing demand is for a more advanced multi-output hybrid converter — one that can deliver both AC and DC outputs simultaneously from a single power source. This crucial requirement is addressed in detail in the next chapter.