DEVICE-CIRCUIT CO-DESIGN OF NOVEL FinFET-BASED DEVICES FOR NEUROMORPHIC COMPUTING AND NON-VOLATILE MEMORY APPLICATIONS

Thesis submitted in partial fulfillment
for the Award of Degree

DOCTOR OF PHILOSOPHY

BY

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Dedicated to Lord Shiva & Sankatmochana

For the Supremacy and to the Redeemer of My Soul

Dedicated to My Family

For their Endless Love, Support, and Encouragement

Dedicated to My Supervisors

For their Endless Motivation, Encouragement, and Teaching Skills

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It is certified that the work contained in the thesis entitled **"Device-circuit Co-design of Novel FinFET-based Devices for Neuromorphic Computing and Non-Volatile Memory Applications" by "*Roopesh Singh*"** has been carried out under my supervision and that this work has not been submitted elsewhere for a degree.

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Roopesh Singh

ROOPESH SINGH

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

Abbreviation	Details
CMOS	Complementary metal-oxide-semiconductor
SRAM	Static random-access memory
DRAM	Dynamic random-access memory
AI	Artificial intelligence
IOT	Internet of things
NVM	Non-volatile memory
FET	Field-effect transistor
FeFET	Ferroelectric field-effect transistor
FeFinFET	Ferroelectric fin field-effect transistor
MTJ	Magnetic Tunnel Junction
STT	Spin Transfer Torque
MRAM	Magneto-resistive random-access memory
JAM	Junctionless-accumulation-mode
MFeFET	Memristive ferroelectric field-effect transistor
RRAM	Resistive random-access memory
TCAD	Technology computer-aided design
PCM	Phase-change memory
PZT	Lead zirconate titanate
SBT	Strontium bismuth tantalate
AD	Asymmetrically doped
AS	Asymmetric spacers
HZO	Hafnium zirconium oxide
HKMG	High-*k* metal gate
ALD	Atomic layer deposition
FeRAM	Ferroelectric random-access memory
FeCap	Ferroelectric capacitor
BOX	Buried oxide
SOI	Silicon-on-insulator
MFIS	Metal-ferroelectric-insulator-semiconductor
p	Parallel
AP	Anti-Parallel
JL	Junctionless
JAM	Junctionless accumulation-mode field-effect transistors
DNN	Deep neural network
AM	Accumulation-mode
IM	Inversion-mode
PCRAM	Phase-change random-access memory
STDP	Spike-timing-dependent plasticity

LTD	Long-term depression
LTP	Long-term potentiation
BEOL	Back-end-of-line
FEOL	Fack-end-of-line
S/D	Source/Drain
BTBT	Band-to-band tunneling
SRH	Shockley–read–hall recombination
IALMob	Inversion and accumulation layer mobility
PhuMob	Philips unified mobility model
TAT	Trap assisted tunneling
LiM	Logic-in-Memory
PL	Pinned Layer
FL	Free Layer
CiM	Compute-in-memory
SOT	Spin-orbit Torque
RMG	Replacement metal gate
MLCS	Multilevel cells
RL	Read line
WL	Write line
SL	Select line
BL	Bit line
RC	Reverse connected
SC	Standard connected

LIST OF SYMBOLS

Symbol	Abbreviation
V_{th}	Threshold voltage
T_C	Curie temperature
E	Electric field
P	Polarization
P_r	Remnant polarization
P_S	Saturation polarization
E_C	Coercive field
G	Gibs free energy
P	Parallel
AP	Anti-parallel
R_T	Total resistance
R_{slcd}	Silicide resistance
R_{Plug}	Plug resistance
R_S	Source resistance
R_D	Drain resistance
V_{GG}	Gate voltage
V_{DS}	Drain to source voltage
T_{BOX}	Buried oxide thickness
V_{GS}	Gate to source voltage
V_{thH}	High threshold voltage
V_{thL}	Low threshold voltage
I_D	Drain current
W_{fin}	Fin width
H_{fin}	Fin height
I_{OFF}	OFF current
I_{ON}	ON current
C_{gg}	Gate capacitance