Chapter 4

Impact of Gate Oxide Stacking on the Performance of Source Pocket Engineered GaSb/Si Heterojunction Vertical TFET Based 8T SRAM Cell

4.1 Introduction

Low-power memory circuits are essential for all Internet of Things (IoT) and Artificial Intelligence (AI) enabled processors and sensors. Thus, the inherently low-power dissipation feature of the TFETs can be used for designing the static random-access memory (SRAM) circuits for low-power electronic gadgets and processor applications. We have already observed in Chapter-3 that the lateral/vertical HfO_2/Al_2O_3 gate stacking in the source pocket engineered (SPE) GaSb/Si heterojunction (HJ) vertical TFETs (VTFETs) [70],[118],[127],[132],[138] improves both the ON-current and subthreshold swing (SS) characteristics over the conventional SPE GaSb/Si HJ VTFETs with only Al_2O_3 as gate oxide (without gate oxide stacking). Thus, this chapter is devoted to investigate the effects of gate-oxide stacking on the performance of 8T SRAM circuits designed by SPE GaSb/Si HJ VTFETs which are considered in Chapter-3. The SRAM circuit has been chosen to demonstrate the circuit level application of the SPE GaSb/Si HJ VTFETs because of the increasing demand of low-power SRAMs [82],[98],[106],[133],[150],[151],[152] for IoTs enabled processor/sensors.

Conventional 6T (six transistor) SRAMs designed by TFETs comprise of two cross-coupled inverters and a pair of access transistors (ATs) which can either be connected in inward or outward directions thereby forming I-6T (inward access transistor based 6T

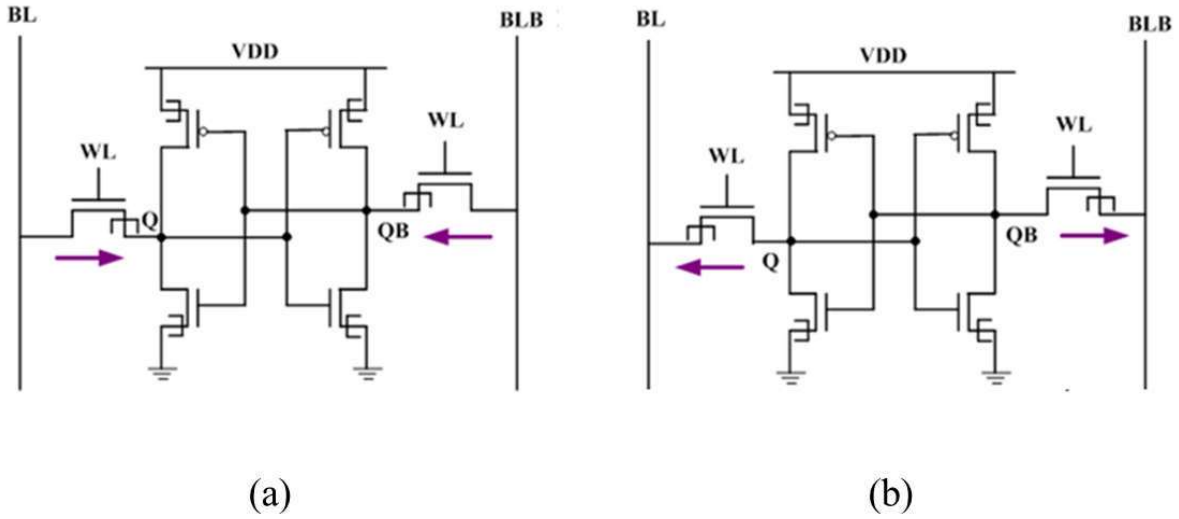

Fig. 4.1: Schematic of 6T SRAM cell designed with TFETs (a) inward access transistors (I-6T), and (b) outward access transistors (O-6T).

SRAM) or O-6T (outward access transistor based 6T SRAM) configuration as shown in Fig. 4.1(a) and (b) respectively [68],[75]. Unfortunately, both the read and write operations cannot be done successfully because of the unidirectional operation of TFETs [68],[75],[77],[82],[133]. In addition, read and write delays are higher for 6T SRAM configurations. In aforementioned configurations, only one AT out of two participates in the write operation which may lead to the single-ended operation. On the other hand, since the outward access transistors do not allow the BLs (bit lines) to discharge, the O-6T structure fails perform the read operation. This makes the TFETs based symmetric 6T SRAM cells unsuitable for memory related applications. To overcome the difficulty, the proposed 8T SRAM cell is designed using transmission gates instead of pass gates where both the pair of I-AT and O-AT are used to perform read and write operations successfully [82]. In 8T SRAM cell, a combination of both inward (I-AT) and outward (O-AT) access transistors are used to form a transmission gate like structure. In the proposed 8T SRAMs, the I-ATs are used for the read

operation of the SRAM cell while O-ATs take part in the write operation. The effect of the lateral/vertical gate-oxide stacking on the performance of SPE GaSb/Si HJ VTFETs based 8T SRAMs has been studied using CADENCE Virtuoso tool by virtue of Verilog A code after exporting the data related to I-V and C-V characteristics of the VTFETs presented for study in Chapter-2 from SILVACO ATLAS^{TM} 3-D TCAD tool. The layout of the present chapter is given as follows:

Section 4.2 deals with the simulation methodology where the device to circuit level framework has been discussed. The exported I-V and C-V characteristics data have been exported from SILVACO ATLAS^{TM} 3-D tool and 2-D look up table-based Verilog-A code has been formed to implement in Cadence Virtuoso tool. Finally, important results and discussions related to the effects of gate oxide stacking on the performance parameters like write margin, read margin, write delay and read delay of the proposed 8T SRAM circuits have been discussed in Sec. 4.3. Finally, Sec. 4.4 concludes the major observations of the present chapter.

4.2 Device to Circuit Level Framework for Implementation of 8T SRAM Using presented VTFETs

This section shows the schematic of 8T SRAM designed with the VTFETs which we have proposed in the Chapter-3 i.e., source pocket engineered GaSb/Si heterojunction vertical TFET structures with Al_2O_3 based homogeneous gate dielectric (SPE GaSb/Si HJ VTFET), source pocket engineered GaSb/Si heterojunction vertical TFET with vertical gate oxide stacking (SPE GaSb/Si HJ VTFET with VS), and laterally stacked heterogeneous gate dielectric (SPE GaSb/Si HJ VTFET with LS). The device design parameters of all presented VTFETs are same as that of the device

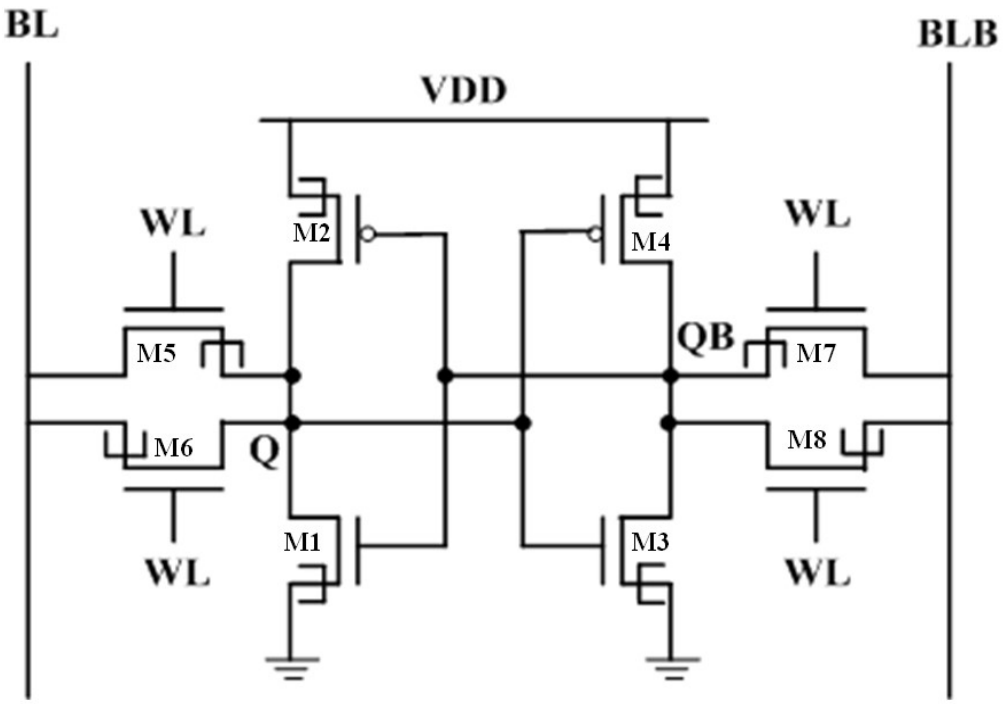

Fig. 4.2: Schematic of 8T SRAM designed with presented VTFETs.

presented in Chapter-3. In 8T SRAM cell, a combination of both inward (I-AT) and outward (O-AT) access transistors are used to form a transmission gate like structure. The I-ATs are used for the read operation of the SRAM cell while O-ATs take part in the write operation. The schematic of the 8T SRAM cell is shown in Fig. 4.2. The transistors M1, M2, M3 and M4 form the cross coupled inverter pair while the transistors M5, M6, M7 and M8 are a part of transmission gate structure on both sides. The transistors M5 and M7 are inward facing access transistors while the transistors M6 and M8 are outward facing access transistors. The write word line (WL) is connected to all of the four access transistors to control them simultaneously during read or write operation. The other two lines namely BL (bit line) and BLB (inverse of bit line) are connected to the access transistors (ATs) as shown in Fig. 4.2.

In order to test the feasibility of our device in circuit level applications, two sets of

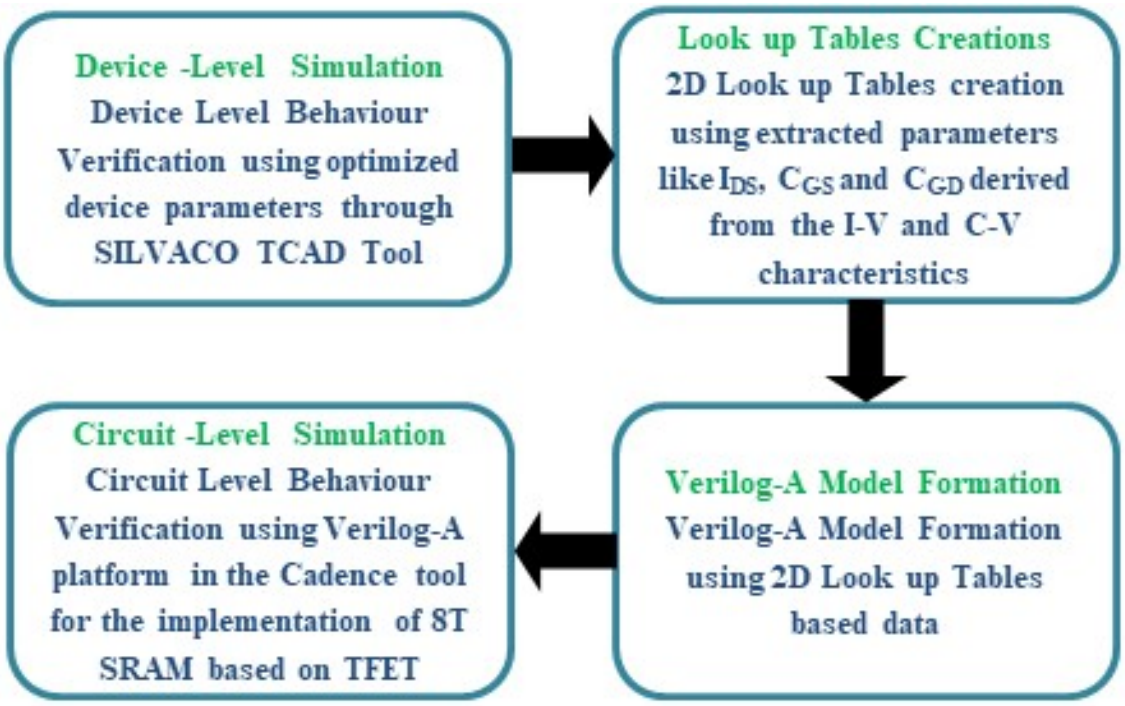

Fig. 4.3: Device (SILVACO ATLAS^{TM} 3-D TCAD tool) to circuit (CADENCE Virtuoso tool) simulation framework.

lookup tables of I-V (current-voltage) and C-V (capacitance-voltage) are constructed using the data exported from SILVACO ATLAS ^{TM} 3-D TCAD tool for the presented VTFETs. The lookup tables are then implemented in CADENCE Virtuoso tool with the help of Verilog-A model [106],[107] for implementing 8T SRAM. 2D look up table-based device-circuit simulation framework is pictorially shown in Fig. 4.3. The p-type VTFETs with and without gate oxide stacking structures are assumed to have symmetric I_D-V_G characteristics corresponding to their n-channel counterparts [107].

Calibration of I_D-V_G characteristics of SPE GaSb/Si HJ VTFET obtained from the CADENCE Virtuoso circuit simulator using 2-D look up table-based Verilog-A model is compared with the SILVACO ATLAS ^{TM} TCAD simulation data at V_{DS} = 1 V as shown in Fig. 4.4. Clearly a good match is observed between the two results validates the exported I-V and C-V data for circuit simulation.

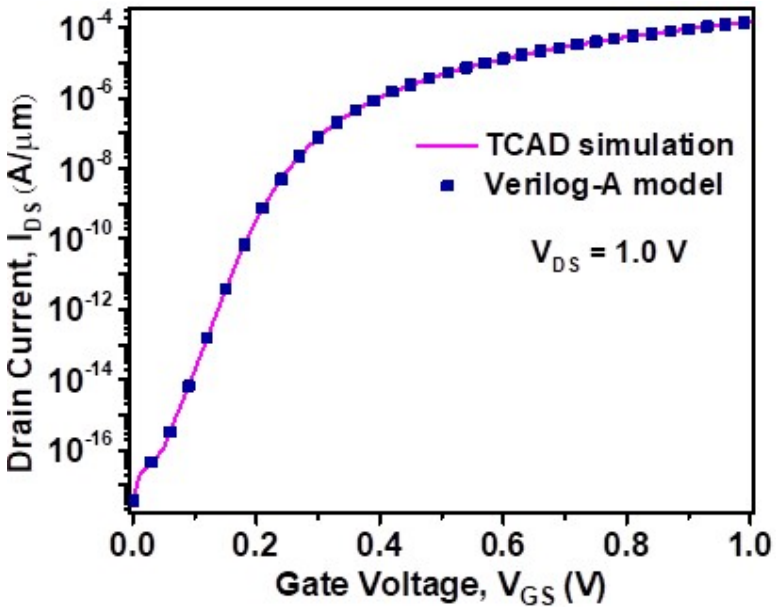

Fig. 4.4: Comparison of I_d-V_g characteristics of a source pocket engineered GaSb/Si heterojunction vertical TFET (SPE GaSb/Si HJ VTFET) between Verilog-A model prediction (symbol) and TCAD simulations (solid line) at V_{DS}= 1.0 V.

4.3 Results and Discussion

In this section, the performance parameters such as read margin, write margin, read delay and write delay of 8T SRAM designed with the presented VTFETs i.e SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS have been investigated considering the impact of lateral and vertical gate oxide stacking.

4.3.1 Read Stability

The read stability of a SRAM is calculated in terms of read static noise margin (RSNM) of the cross coupled inverter present in a SRAM. It is the measure of the highest noise value for which the value of the storage node remains constant [150][151]. The RSNM is calculated graphically from the butterfly curve obtained by transfer characteristics of

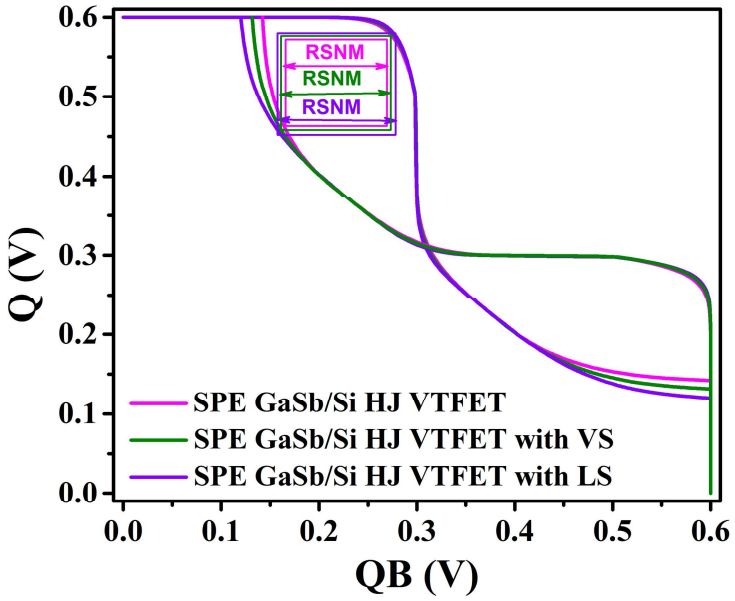

Fig. 4.5: Read static noise margin (RSNM) calculation for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, SPE GaSb/Si HJ VTFET with LS at 0.6 V supply voltage.

the cross coupled inverter under the operating condition BL= 'V_{DD}', BLB= 'V_{DD}' and WL= 'V_{DD}' and is equal to the side of the largest square that can be inscribed inside smaller lobe of butterfly curve. The voltage values of the storage node in 8T SRAM cell are affected by the bit line voltage due to the presence of inward access transistors (M5 and M7). Hence, the 8T based SRAM cells show low values of read static noise margin (RSNN) as compared to the O-AT 6T SRAM cell. The RSNMs values are calculated graphically as shown in Fig. 4.5 as the length of side of the largest square that can be inscribed inside the smaller lobe of the butterfly curve for a supply voltage of 0.6 volts. The RSNMs of 8T SRAM cell based on SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS are plotted in Fig. 4.6(a) for different values of supply voltage. The 8T SRAM cell based on SPE GaSb/Si HJ VTFET with LS shows higher RSNM value as compared to SRAMs using SPE GaSb/Si

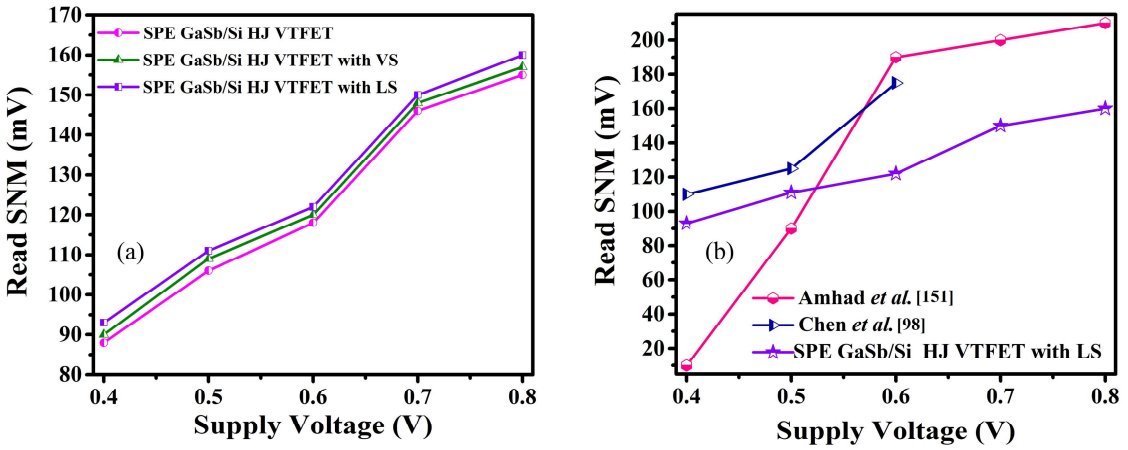

Fig. 4.6: (a) Comparative plot of read SNM (RSNM) for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS; and (b) Comparative plot for read SNM (RSNM) of SPE GaSb/Si HJ VTFET with LS with other reported 8T SRAM based on TFET.

HJ VTFET with VS, and SPE GaSb/Si HJ VTFET because of higher ON-current with lower average subthreshold swing of the former device than the later devices. The RSNM values are following a desired trend with respect to the increase in supply voltage i.e it is getting increased with increase in supply voltage. Fig. 4.6(b) shows the comparative plot of RSNM of the SPE GaSb/Si HJ VTFET with LS with other two reported 8T SRAM based TFET [98],[151]. We have only considered the best VTFET with highest RSNM i.e SPE GaSb/Si HJ VTFET with LS out of the three VTFETs for RSNM comparison with other reported results. From the aforesaid plot we can conclude that our proposed SPE GaSb/Si HJ VTFET with LS shows comparable value to that of other reported results.

4.3.2 Write Ability

The write stability is gauged in terms of write static noise margin (WSNM) or write

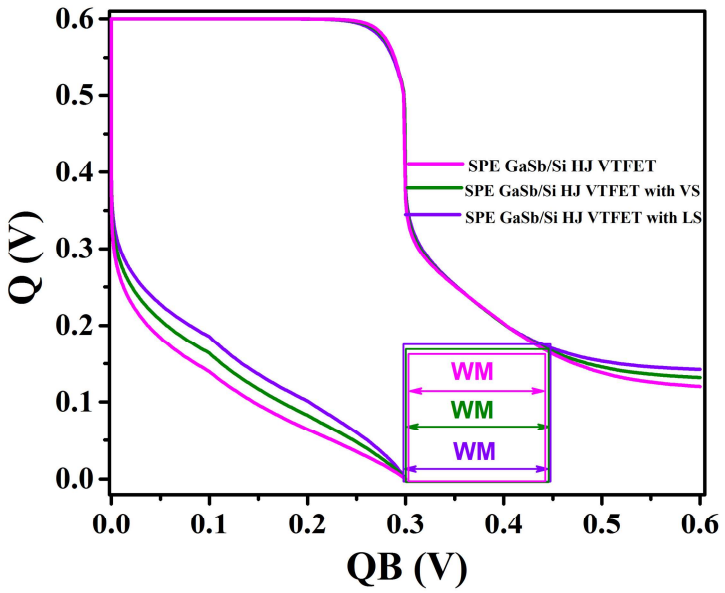

Fig. 4.7: Write margin (WM) calculation for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, SPE GaSb/Si HJ VTFET with LS at 0.6 V supply voltage.

margin (WM) of the SRAM cell. For WM calculations, the butterfly curve is plotted for the transfer characteristics of the cross coupled inverter at asymmetrical bit line condition i.e., BL= 'V_{DD}' ('0') and BLB= '0' ('V_{DD}') at WL= 'V_{DD}'. The WM is equal to the side of the smallest square that can be made touching both the VTCs. For successful write operation these VTCs should intersect at a single point [115]. As compared to the single-ended write operation in O-AT 6T SRAM due to the unidirectional conduction of the Outward facing access transistors, the write operation in 8T SRAM TFET is done by utilizing both inward (I-AT) and outward access transistors (O-AT) which are a part of the transmission gate type access path in it. The method of calculation of WM of the SRAM is shown in Fig. 4.7 for a supply voltage of 0.6 volts. Large write margin values are reported in 8T SRAM due to its bidirectional write operation which can be attributed to the presence of the transmission gate type access transistor path. Therefore, the WM of 8T SRAM shows a considerable

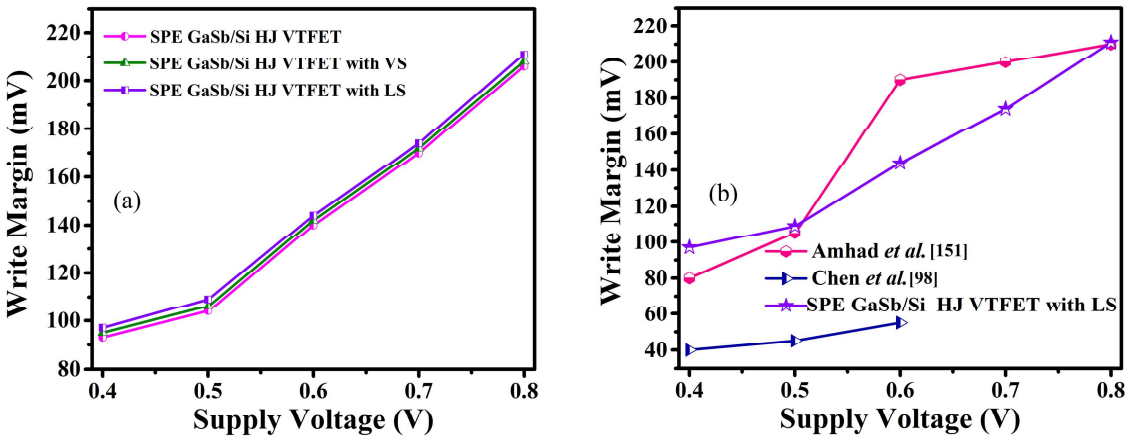

Fig. 4.8: (a) Comparative plot of write margin (WM) for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS; and (b) Comparative plot of write margin (WM) for SPE GaSb/Si HJ VTFET with LS with other reported 8T SRAM based on TFET.

improvement as compared to O-AT 6T SRAM configuration. The WM plot for different supply voltages of 8T SRAM based on SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS are shown in Fig. 4.8(a). Moreover, the 8T SRAM based on SPE GaSb/Si HJ VTFET with LS shows slightly higher WMs as compared to other two presented VTFETs. This can be attributed to improved current-voltage characteristics of SPE GaSb/Si HJ VTFET with LS due to the use of heterogeneous gate oxide in a lateral stacking manner. Figure 4.8(b) shows the comparative plot of WM of the SPE GaSb/Si HJ VTFET with LS with other two reported 8T SRAM cited earlier based on TFET. From the aforesaid plot we can conclude that our proposed SPE GaSb/Si HJ VTFET with LS is showing improved values compared to the other two reported results.

4.3.3 Read Delay

The read delay of the SRAM cell is a measure of the speed of its read operation. For

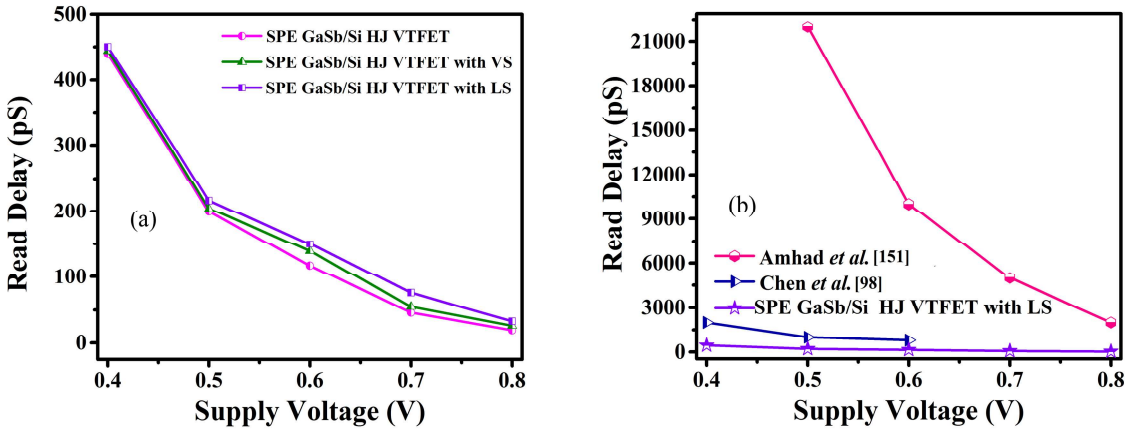

Fig. 4.9: (a) Comparison of read delay for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS; and (b) Comparison of read delay of SPE GaSb/Si HJ VTFET with LS with other reported 8T SRAM based on TFET.

faster read operation in SRAM, read delay should be as low as possible. The read delay is calculated by pre-charging the bit line capacitances to 'V_{DD}' value and is equal to the time required to obtain 10 % of V_{DD} difference between BL and BLB value after word line voltage is raised to V_{DD} [150],[151]. Fig. 4.9 shows the read delay comparison of 8T SRAM based on SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS for supply voltage range of 0.4 volts to 0.8 volts. The 8T SRAM cell shows improved values of read delays as compared to 6T SRAM design since there is a bi-directional current path in 8T SRAM cells employing a combination of both inward (I-AT) and outward transistors (O-AT) [82]. The 8T SRAM cells based on gate oxide stacked VTFETs i.e., SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS have higher values of the read delays because of the enhanced parasitic capacitances i.e due to higher C_{gd} as discussed in Chapter-3 compared to the VTFET without any gate oxide stacking (SPE GaSb/Si HJ VTFET). As low read delays are always preferred to have faster operation, the device without having any gate oxide

stacking is mostly preferable than gate oxide stacked TFETs. This is noted that the gate oxide stacked TFET based SRAM have the only disadvantage of having more read delays which makes a huddle for faster operation than SRAM based on TFET without having any oxide stacking. We have compared the read delays of SPE GaSb/Si HJ VTFET with LS with some reported results which show that our proposed SPE GaSb/Si HJ VTFET with LS shows low values of read delays compared to other two reported results [98],[151] based on 8T SRAM as shown in Fig. 4.9(b). That qualifies our 8T SRAM based on SPE GaSb/Si HJ VTFET with LS for fast switching and low power applications. Although, the VTFET without having gate oxide stacking (SPE GaSb/Si HJ VTFET) shows lower read delays than VTFET with gate oxide stacking (SPE GaSb/Si HJ VTFET with LS and SPE GaSb/Si HJ VTFET with VS), SPE GaSb/Si HJ VTFET with LS has been chosen for read delay comparison as shown in Fig. 4.9(b) to maintain uniformity in 8T SRAM performance comparison as considered earlier figures (Fig. 4.7(b), and Fig. 4.8(b))

4.3.4 Write Delay

The write delay of the SRAM cell is equal to the time required for charging or discharging of the storage node to 50 % of its initial value after the word line is activated (WL= 'V_{DD}') [150],[151]. The write delay variation of 8T SRAM employing SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS is given in Fig. 4.10(a). Since there is bi-directional accessing capability in 8T SRAM cell due to the presence of both I-AT and O-AT, smaller values of write delays are reported in it as compared to 6T SRAM based on TFET. The use of transmission gate in 8T SRAM cell leads to faster charging and discharging to the storage nodes Q and Q_B resulting in smaller write delay as shown in Fig. 4.2. SPE

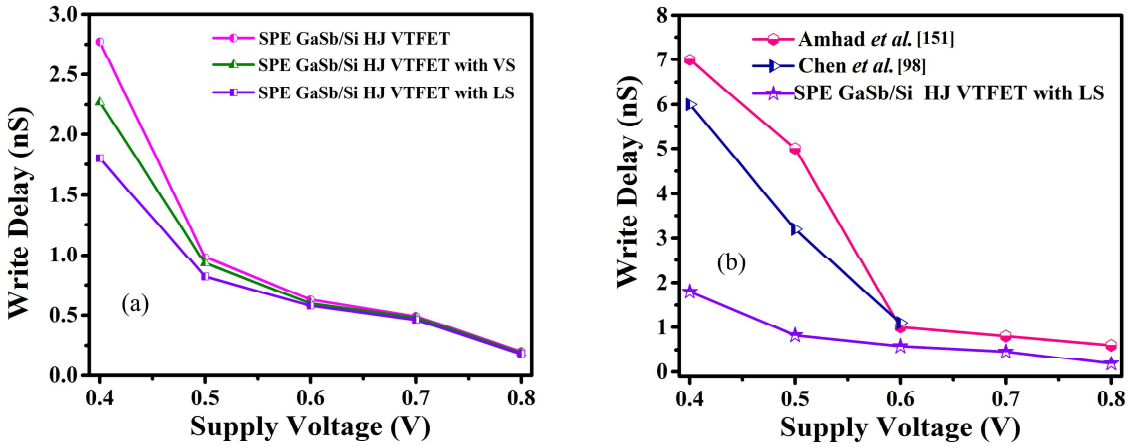

Fig. 4.10: (a) Comparative plot of write delay for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS; and (b) Comparative plot of write delay for SPE GaSb/Si HJ VTFET with LS with other reported 8T SRAM based on TFET.

GaSb/Si HJ VTFET with LS shows low value of write delay compared to SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET. This is because of higher ON-current of the former device compared to later ones causes faster charging and discharging of the storage nodes. This is important to note here that the VTFETs with gate oxide stacking (i.e., SPE GaSb/Si HJ VTFET with LS and SPE GaSb/Si HJ VTFET with VS) have higher ON-current with almost insignificant variation in OFF- state current making I_{ON}/I_{OFF} ratio higher for SPE GaSb/Si HJ VTFET with LS and SPE GaSb/Si HJ VTFET with VS than SPE GaSb/Si HJ VTFET. The important conclusion which can be derived here is that if I_{ON}/I_{OFF} ratio is high then write delays will be less. The comparative plot of write delays for different supply voltages are shown in Fig. 4.10(b) for the SPE GaSb/Si HJ VTFET with LS along with some other reported results based on 8T SRAM TFET. It clearly reveals that write delay of the SPE GaSb/Si HJ VTFET with LS is much less compared to the two [98],[151] reported results. Table-4.1 shows the

TABLE 4.1
COMPARISON OF DIFFERENT 8T SRAM PERFORMANCE PARAMETERS OF SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET WITH VS, AND SPE GaSb/Si HJ VTFET WITH LS

Supply Voltage	Parameters	SPE GaSb/Si HJ VTFET with LS	SPE GaSb/Si HJ VTFET with VS	SPE GaSb/Si HJ VTFET
0.4 V	RSNM (V)	88	90	93
	WRNM (V)	93	95	97
	Read Delay (ps)	439	444	450
	Write Delay (ns)	2.77	2.27	1.80
0.5 V	RSNM (V)	106	109	111
	WRNM (V)	104	106	109
	Read Delay (ps)	199	204	216
	Write Delay (ns)	0.98	0.93	0.82
0.6 V	RSNM (V)	118	120	122
	WRNM (V)	140	142	144
	Read Delay (ps)	117	139	150
	Write Delay (ns)	0.63	0.60	0.58
0.7 V	RSNM (V)	146	148	150
	WRNM (V)	170	172	174
	Read Delay (ps)	46	55	76
	Write Delay (ns)	0.49	0.48	0.46
0.8 V	RSNM (V)	155	157	160
	WRNM (V)	206	208	211
	Read Delay (ps)	19	26	33
	Write Delay (ns)	0.20	0.19	0.18

performance comparison of different SRAM performance parameters of the presented VTFETs i.e SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS and SPE

GaSb/Si HJ VTFET with LS. Although, SPE GaSb/Si HJ VTFET with LS shows higher read delays than other two VTFETs, other SRAM performance parameters are better for the SPE GaSb/Si HJ VTFET with LS makes it suitable for low power memory related applications.

4.4 Conclusion

In this chapter the impact of vertical and lateral gate oxide stacking on the 8T SRAM cell performance parameters based on SPE GaSb/Si HJ VTFETs (i.e SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET with LS) has been investigated. The performance parameters like write stability (write margin), read ability (RSNM), read delay and write delay are investigated for the 8T SRAM cell designed by SPE GaSb/Si HJ VTFET with LS, SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET. The SPE GaSb/Si HJ VTFET with LS based 8T SRAM shows higher read SNM, higher write margin, and lower write delay as compared to 8T SRAMs designed by SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET. However, the higher intrinsic capacitance in SPE GaSb/Si HJ VTFET with LS device leads to higher read delay in the SPE GaSb/Si HJ VTFET with LS based 8T SRAM than other two 8T SRAMs based on SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET as investigated in this chapter. Moreover, The SPE GaSb/Si HJ VTFET with LS with better device level performance as discussed in Chapter-3 shows better circuit level performance when investigated for 8T SRAM. In addition, the proposed VTFETs shows better performance compared to other reported 8T SRAM based on TFET. Thus, the proposed 8T SRAM cell based on SPE GaSb/Si HJ VTFETs suitable for low power IoT enabled processors.