Chapter 5

Quad-Operative Fractional Processor for Wide Battery Voltage EV Charging Applications

5.1 Introduction

Having established the benefits of FPP approach in previous chapters, this chapter broadens the operational capabilities of FPP based battery chargers for the more complex demand of EV charging. In previous chapters, two distinct FPP-based chargers were introduced one designed for voltage step-up operation and another serving multi-utility applications with step-down functionality. While these chargers demonstrated significant efficiency improvements and operational flexibility, they were limited to two-quadrant operation, restricting their output to only positive voltage. This constraint hinders their applicability in scenarios requiring bidirectional power flow across both positive and negative voltage domains.

To deal with the application requirements, the fractional power processors based on basic topologies often have to be designed for relatively large power levels, reducing their practical feasibility due to cost and complexity reasons. To extend the two-quadrant operation, [114] suggested employing either an unfolder circuit or bipolar switches to accommodate negative voltage. However, the use of bipolar switches to obtain four quadrant operation resulted in better performance compared to former approach. Moreover, using bipolar switches results in 50 % reduction in the active power processed through the converter compared to the only step-up or step-down FPP, improving the converter performance further for highly efficient charging.

However, several challenges arise in the design and implementation of quad-operative FPPs for EV charging. These include optimal component selection to minimize voltage and current stress, achieving seamless operation across a wide range of battery voltages, and implementing specific configuration to ensure soft switching and high efficiency.

Literature [118], [119] reported using bipolar switches based LC and CLLC resonant tank, however the former required three winding transformer and component matching in both bridges whereas the later required higher resonant component degrading converter power density. Further, in contrast to the earlier proposed voltage-fed step up/down chargers, the current derived converters offer superior performance in terms of reliability and soft-switching. The reported step-up/down converter in [121], [122] extends the operation to four quadrants, however, the converter requires dedicated PI controller to achieve a smooth current regulation.

To overcome these limitations, this chapter presents quad-operative fractional power processor that extends the operational range of the charger to four quadrants. This enables seamless handling of both charging and discharging modes, encompassing both step-up and step-down voltage conversion while maintaining the advantages of fractional power processing. The proposed topology not only enhances efficiency by minimizing processed power but also facilitates critical functionalities and smooth current control, thereby improving integration with modern EV infrastructure.

This chapter presents the quad-operative fractional power processor for wide range EV charging application. The subsequent sections of this chapter will discuss the specifics of the proposed FPP-based quad-operative converter topology. The details of the control strategy employed to achieve seamless and efficient bidirectional power flow is discussed. Further, comprehensive simulation results validating the converter's performance under various operating conditions, and the experimental validation of the proposed concept through a laboratory developed prototype is presented. Ultimately, this chapter aims to demonstrate the feasibility and potential of FPP-based quad operative charger to significantly enhance the efficiency, reduce the cost, and improve overall charging of EVs.

5.2 The Proposed Quad-Operative Fractional Processor for Wide Battery Voltage

The proposed quad-operative fractional power processor is shown in Fig. 5.1. The battery under charging represents the connected load. The proposed charger works in buck mode when the battery voltage is lower than the source voltage V_{dc} whereas, when the battery voltage under charging is higher than the source voltage, the fractional power processing

charger works in boost mode. However, it is notable that while covering the entire range of buck and boost voltage, the dc/dc converter still always works in buck mode with a gain $(V_{bat} - V_{dc})/V_{bat}$ simplifying the converter design and facilitating component optimization.

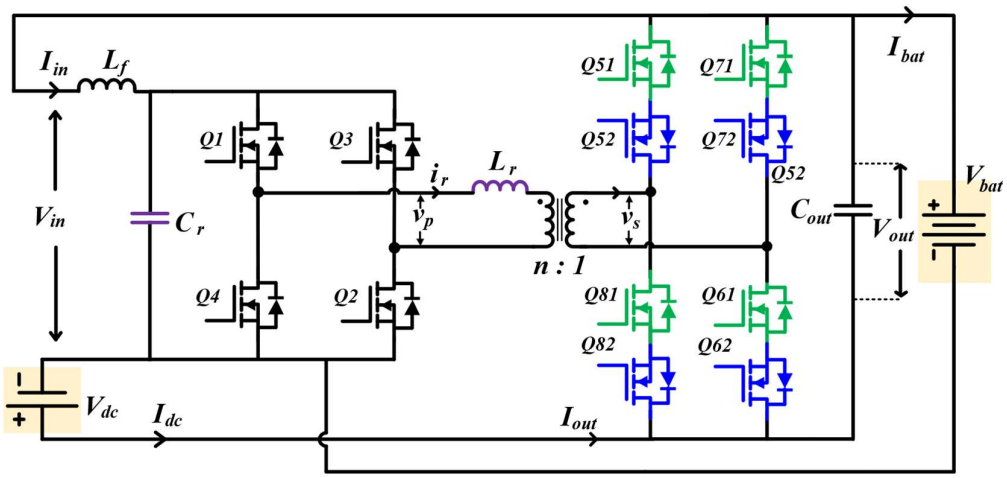


Fig. 5.1 The proposed quad-operative fractional power processor

Further, during the battery discharging operation, the converter works in boost mode and negative phase shift and similarly in buck mode negative phase shift to deliver power from battery to V_{dc} in for each quadrant respectively. The amalgamation of each mode of quad-operative fractional power processor is shown in Fig. 5.2.

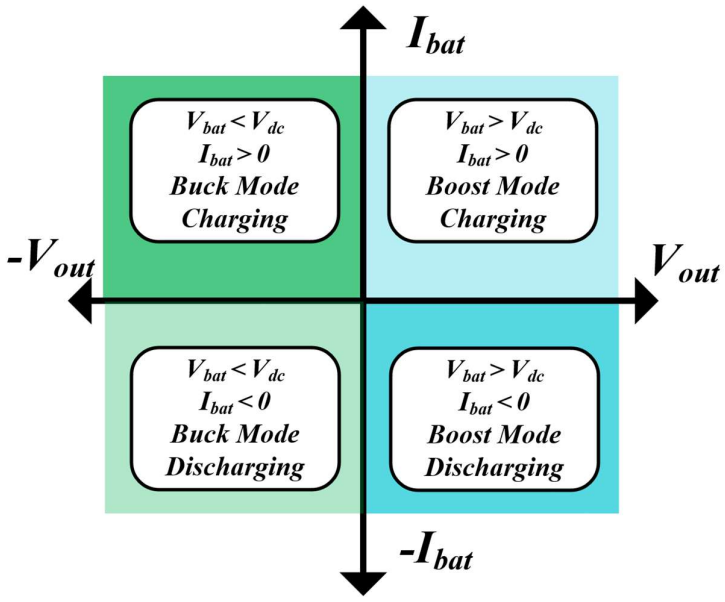


Fig. 5.2 Operation modes of proposed quad-operative fractional power processor.

5.2.1 Circuit Configuration

The fractional converter is connected in input parallel output series configuration. Due to parallel input, only the differential current enters the converter, i.e., the size of the inductor to achieve current source behavior can be greatly reduced. The H-bridge forms the high voltage port, connected in parallel with the resonant capacitor, followed by a high frequency transformer. The transformer is designed with turn ratio to optimize the voltage and current stress based on the desired battery voltage range. The input capacitor C_r forms a parallel resonant tank with the leakage inductance of the transformer.

The transformer secondary is connected to the bipolar MOSFET switch based H-bridge, also referred as full-bridge matrix stage, as shown in Fig. 5.1. This allows the converter to operate with both positive and negative output voltage as well as MOSFETs allow bidirectional current flow, enabling quad-operation. The secondary bridge is further connected in series with the DC source and battery. Due to the series connection at the output, the secondary bridge switches experience differential voltage. This provides the opportunity to obtain significantly reduced voltage stress allowing use of significantly low voltage rated switches. Further, the power processed by the converter in FPP depends on the difference voltage, which impacts the overall efficiency of the system. In the proposed input parallel output series configuration based fractional power processor supporting both buck and boost mode, the power processed is halved compared to step up or step-down FPP converter alone. This provides an opportunity to further optimize the converter rating.

5.3 Operation and Analysis of the Proposed EV Charger

5.3.1 Operation of Quad-Operational Charger in Buck Mode:

Quadrant II ($V_{bat} < V_{dc}, I_{bat} > 0$) and Quadrant III ($V_{bat} < V_{dc}, I_{bat} < 0$)

The quad-operative fractional power processor works in either of the four quadrant with seamless transition between each modes depending upon the polarity of differential voltage at the converter output and that of reference battery current. When the battery under charging is of lower voltage compared to the source voltage, the circuit configuration results in output voltage given by $V_{bat} - V_{dc}$ to be negative. This negative voltage at V_{out} which is sensed and accordingly PWM strategy is selected. The direction

(charging and the discharging) and the magnitude of reference current is achieved by setting the polarity and value of phase shift ensuring ease of control and seamless transition between all four operating modes.

The operation of the converter in buck mode during one switching cycle is divided into four switching intervals as shown in generalized current and voltage waveforms shown in Fig. 5.3.

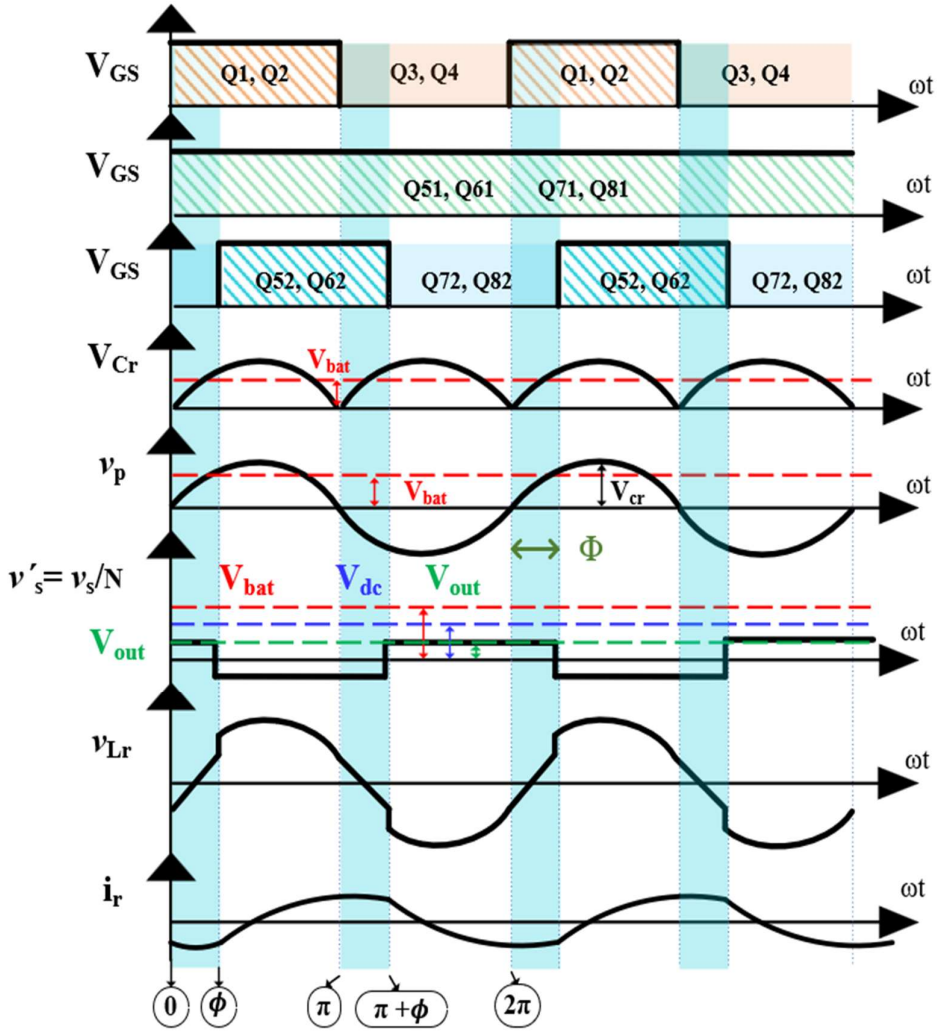
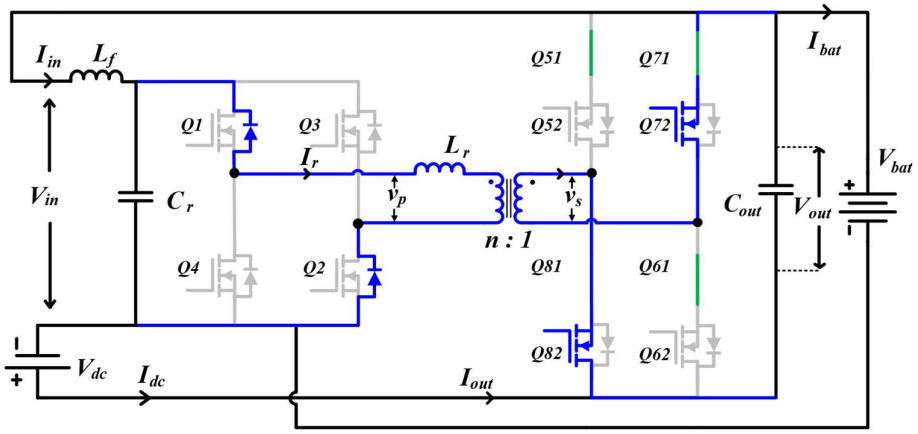


Fig. 5.3 Key waveforms of proposed quad-operational charger in buck mode, forward power flow.

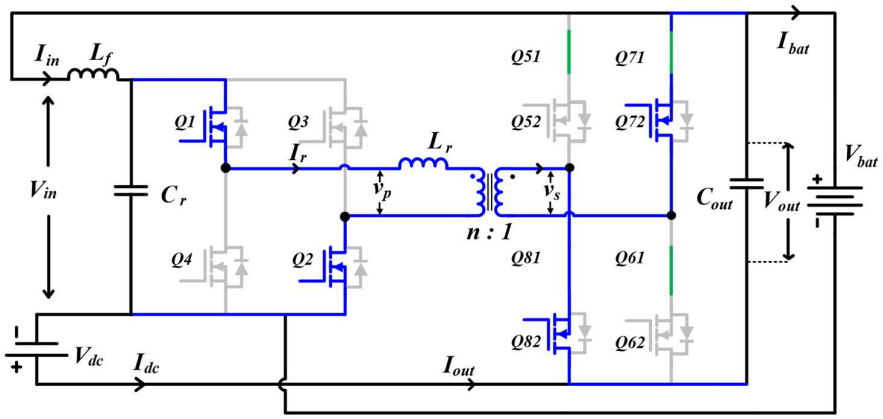
The charger circuit with active switches in each interval is shown in Fig. 5.4 and Fig. 5.5. Each of the bridge switches operate for 50% duty with a small deadtime. The phase between the primary bridge switch gate pulse V_{GSQ1} and secondary bridge switch gate pulse V_{GSQ51} (or V_{GSQ52}) is defined as the phase shift between primary and secondary bridge. In the buck mode, the upper switch Q51-81 of each leg of the secondary bridge

remains on during the entire cycle whereas, while Q52-82 are switched continuously with lagging phase shift to deliver power from source to load, in charging mode. Further, Q52-82 at a leading phase shift to deliver power from load to source in discharging mode. Switches Q72 Q82 are assumed to be already in conduction.

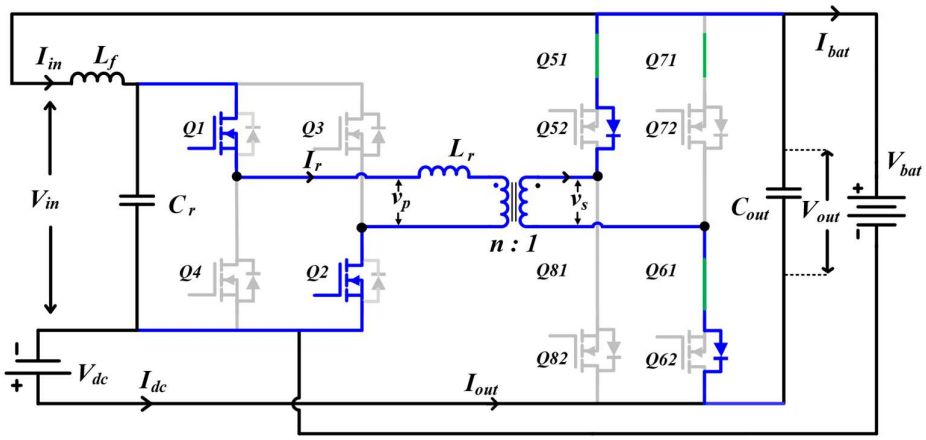
Fig. 5.4 (a). As the inductor voltage v_{Lr} changes from negative to positive, the current after decaying, begins to rise with a positive slope. This interval ends at phase shift ϕ when switches Q72 Q82 is turned off and Q52 Q62 is gated. This results in a negative voltage across transformer secondary as shown in Fig. 5.3, however due to the negative current the diode of Q52 Q62 conducts as is shown in Fig. 5.4 (b).



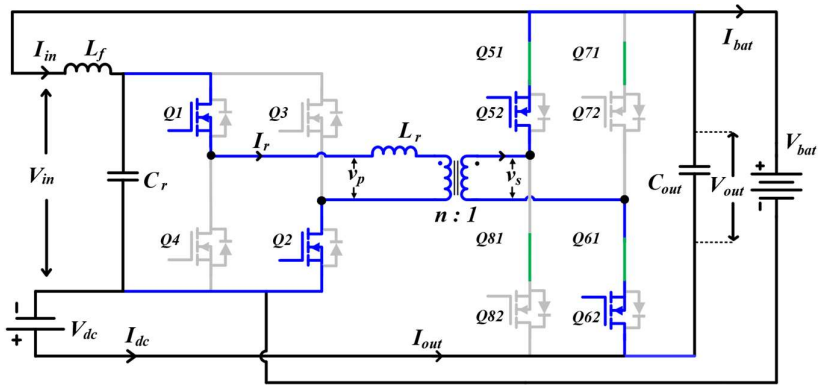
(a) Interval I: During deadband



(b) Interval I: $0 < \omega t \leq \phi$.



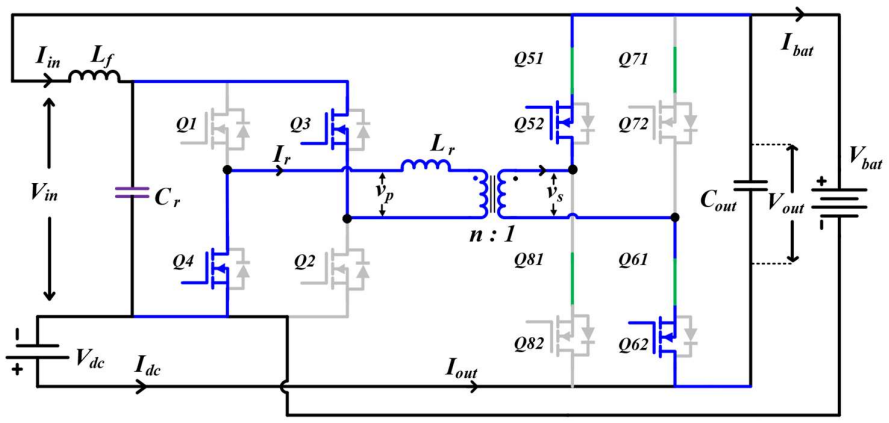
(c) Interval II: During deadband



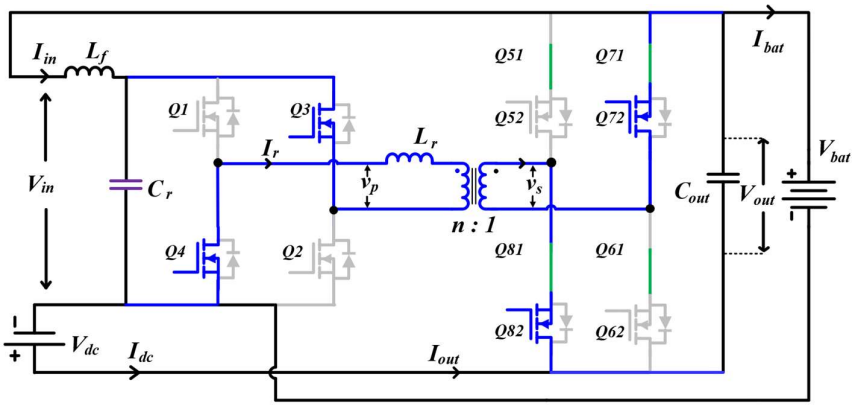
(d) Interval II: $\phi < \omega t \leq \pi$.

Fig. 5.4 Equivalent circuit of proposed charger during battery charging corresponding to operation in buck mode in (a) & (b) during deadband and Interval I, respectively (c) & (d) during deadband and Interval II.

The converter operation begins at $\omega t = 0$, with primary bridge switches Q3 Q4 turning off and Q1 Q2 being gated. As the current is of lagging nature, the current remains negative, i.e., flows through the anti-parallel diode of Q1 Q2, ensuring zero voltage during switch turn on, while switches Q72 Q82 remains in conduction as shown in Fig. 5.4. (b). It is important to note that the secondary bridge switches Q51-81 remains on during the entire buck mode operation. As no switching takes place a conduction channel is formed which allows the current to flow through it in both directions preventing body diode conduction. This ensures much lesser conduction losses compared to the literatures where diode is employed for bipolar voltage handling capability.



(a) Interval III: $\pi < \omega t \leq \pi + \phi$.



(b) Interval IV: $\pi + \phi < \omega t \leq 2\pi$.

Fig. 5.5 Equivalent circuit of proposed charger during battery charging corresponding to operation in buck mode in (a) Interval III (b) Interval IV.

The resonant inductor voltage is given by $v_p - nv_s = v_{cr} + nv_{out}$. Due to this positive voltage the current i_r continues to rise and crosses zero, resulting in switches turning on switches Q1 Q2 and Q52 Q62 at zero voltage, as in Fig. 5.4 (c). The operation in the negative half cycle of v_p is similar from π to 2π due to the symmetrical nature of the proposed topology and the equivalent circuit in each interval is represented in Fig. 5.5. It may be observed that only the difference between the battery voltage and the source voltage appears at the output significantly reducing the voltage stress at the secondary bridge switches.

5.3.1 Operation of Quad-Operational Charger in Boost Mode:

Quadrant I ($V_{bat} > V_{dc}, I_{bat} > 0$) and Quadrant IV ($V_{bat} > V_{dc}, I_{bat} < 0$)

In the boost mode of operation, i.e., when the battery voltage is higher than the dc source voltage, the output voltage V_{out} becomes positive. Based on the sensed voltage, the PWM strategy is such that the secondary bridge switches Q52-72 remains on for the entire cycle, whereas Q51-Q81 switches continuously. The key waveform of converter operation in boost mode is shown in Fig. 5.6.

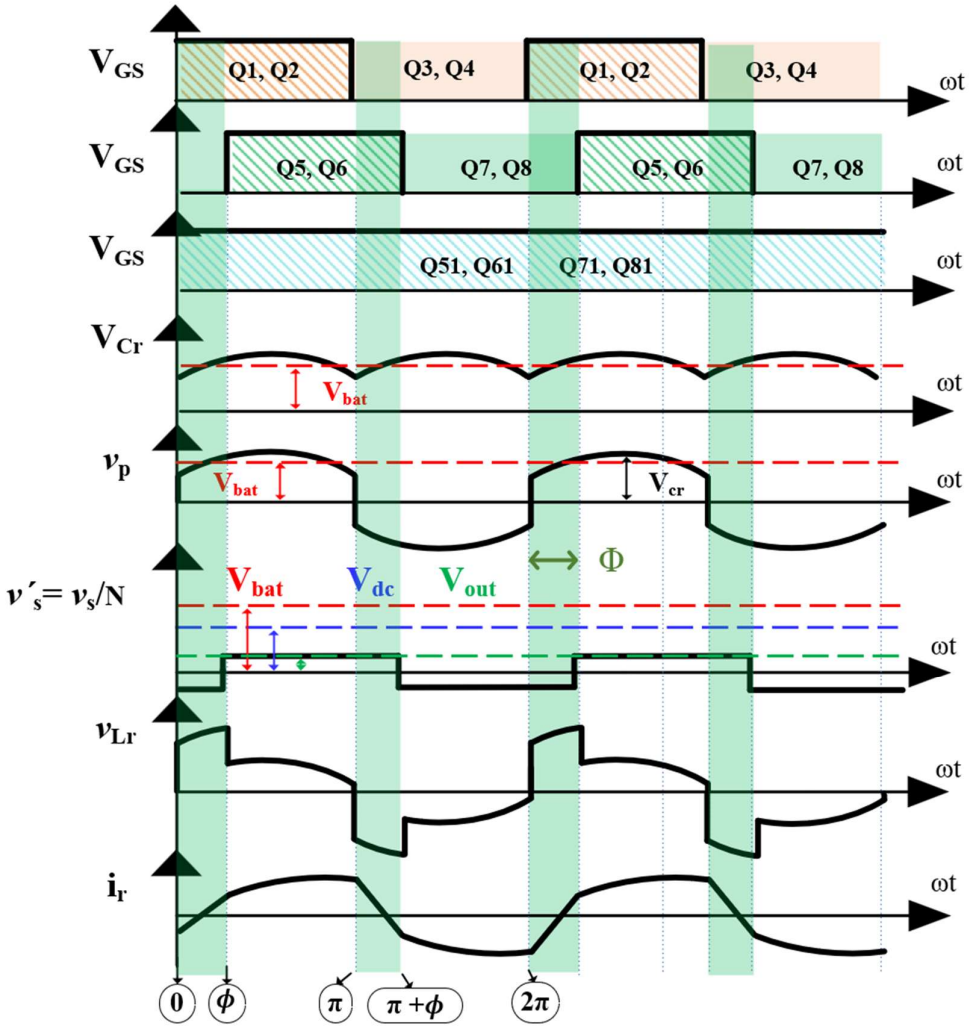


Fig. 5.6 Key waveforms of proposed quad-operational charger in boost mode, forward power flow.

For first quadrant operation, i.e., boost charging mode, the phase shift is set to be lagging secondary with respect to primary voltage. While for discharging mode quadrant IV operation the phase shift is set to be leading secondary with respect to primary voltage.

At the beginning of the cycle Q1 Q2 are turned on with Q71 Q81 already in conduction. The inductor current begins to rise with a positive slope. After a phase shift ϕ, the switches Q71 Q81 are tuned off. The current flows through the anti-parallel diode of the switch Q51 Q61 ensuring ZVS operation.

5.4 Verification

The operation and performance of the proposed quad-operative fractional power processor is verified for all four cases of operation. The performance critical to high power charging and discharging operation is verified through simulation and the results are presented in the following sections. With DC source voltage of 200 V and 350 V battery considered in case of boost mode whereas buck mode is analyzed by considering a 50 V battery. The converter parameters are listed in Table 5.1.

Table 5.1 Charger Design Parameters

Component	Value	Component	Value
Inductor, L_f	1.3 mH	Characteristic Impedance, Z_o	8.89 Ω
Capacitor, C_{in}	94 μF	Leakage Inductance, L_r	16 μH
Turn ratio, N	16:10	Resonant Capacitor, C_r	202 nF
Resonant Frequency, f_r	89 kHz	Switching Frequency, f_s	89 kHz
Source Voltage, V_{dc}	200 V	Battery Voltage, V_{bat}	200 ± 150 V

5.4.1 Operation in Boost Mode: Forward Power Flow

When the battery with its discharged SOC is connected at the load such that the terminal voltage is higher than the source voltage, and the reference battery current is positive, i.e., battery is to be charged, the upper switches of secondary (Q51-81) are supplied with positive phase shift pulses calculated based on the reference current. It may be observed from the results presented in Fig. 5.7 when the battery voltage is higher than V_{dc} the positive voltage appears across V_{out}. The magnitude of V_{out}, and subsequently secondary

bridge voltage v_s is much lower compared to the load voltage, which allows reduced voltage stress across secondary switches. From Fig. 5.7, it may be observed that only the difference current flows through input bridge offering about 50% reduction in the input current and primary bridge switch ratings.

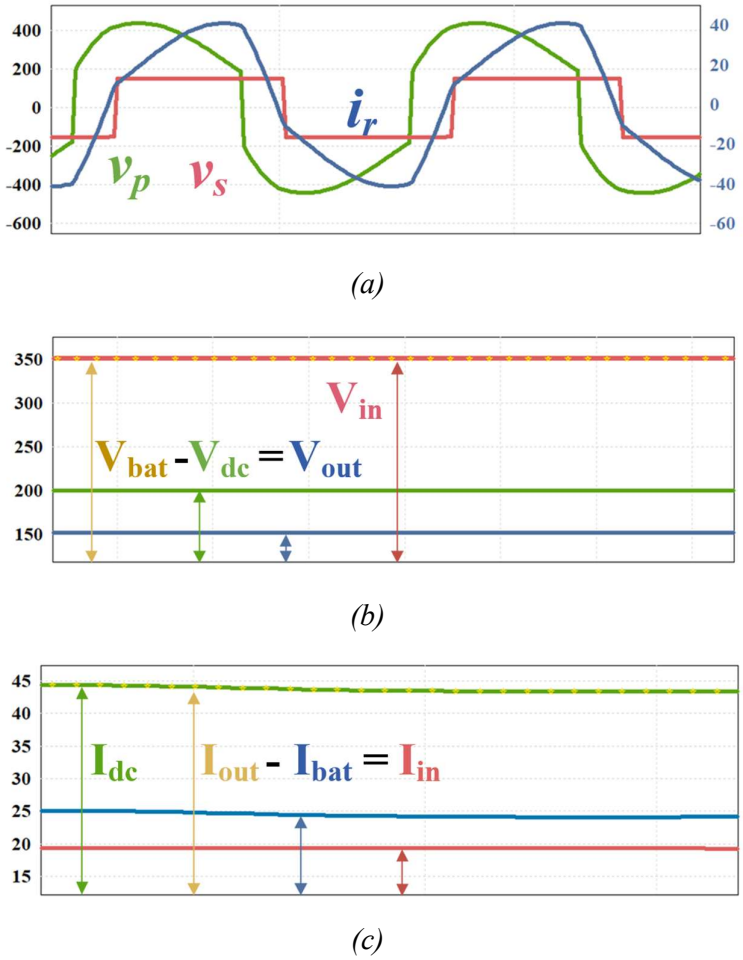


Fig. 5.7 Simulation results for charging operation in boost mode (a) Transformer primary secondary voltage and primary inductor current (b) Terminal Voltages at different ports (c) System and converter currents.

Fig. 5.8 and Fig. 5.9 shows the experimental waveform for converter operation in boost mode. In Fig. 5.8 a 48 V battery is being charged with 30 V dc source, the converter output voltage si positive. The inductor current demonstrates soft-switching operation. Fig. 5.9 shows a 120 V battery being charged from 65 V battery. In both the cases due to the differential voltage significant reduction in secondary voltage is achieved.

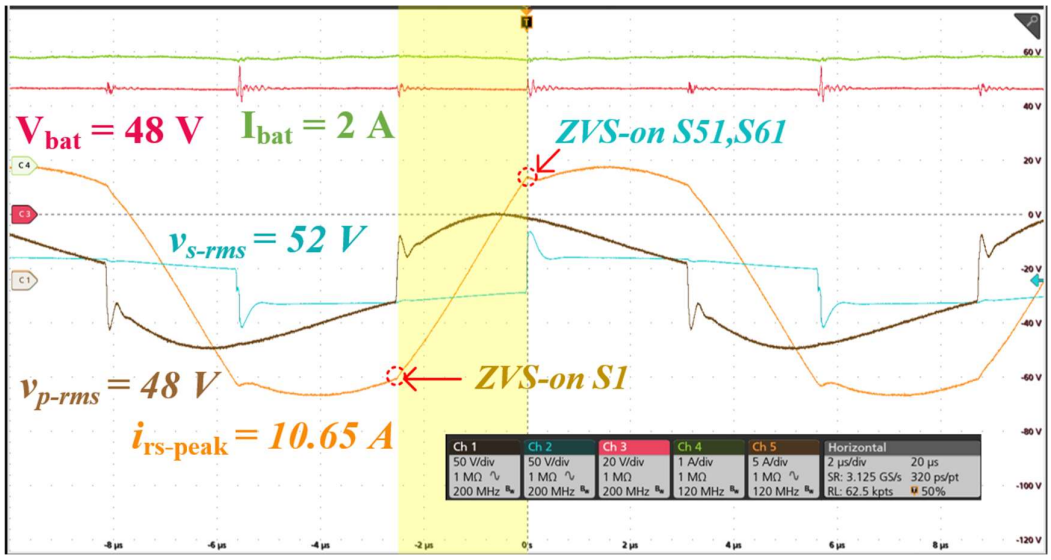


Fig. 5.8 Experimental results of the proposed quad-operative fractional power processor in boost charging mode with $V_{dc} = 30\ V$, $V_{bat} = 48\ V$, $\phi = 80°$.

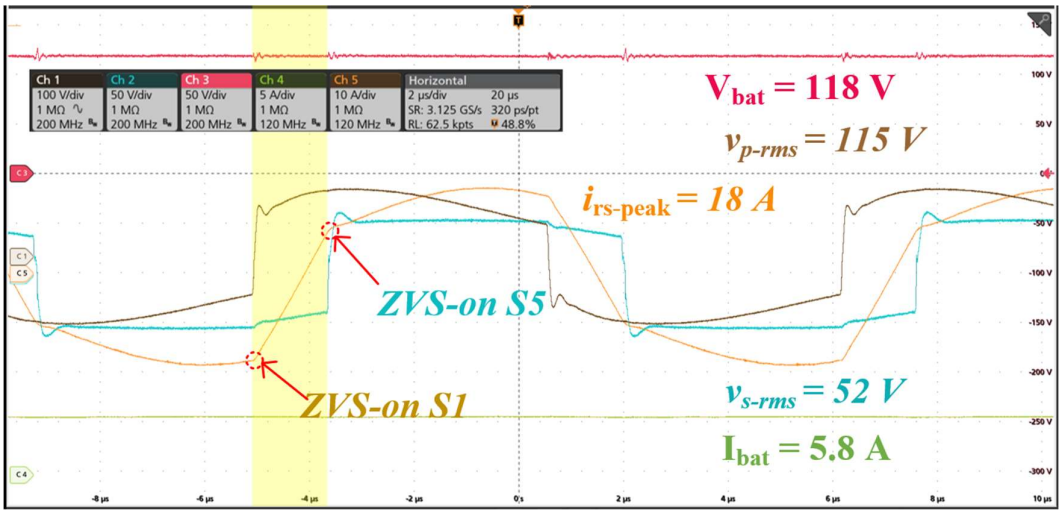
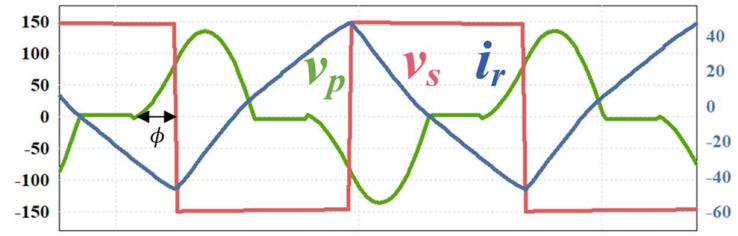


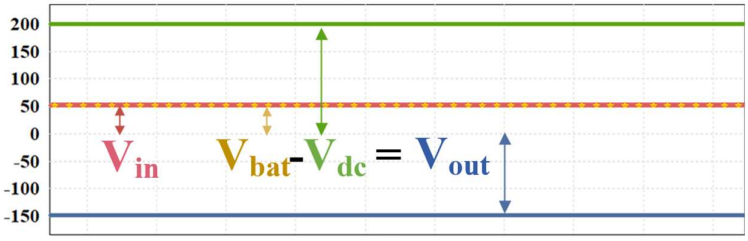
Fig. 5.9 Experimental results of proposed quad-operative fractional power processor in boost charging mode with $V_{dc} = 65\ V$, $V_{bat} = 120\ V$, $\phi = 45°$.

5.4.2 Operation in Buck Mode: Forward Power Flow

When the battery voltage is lower than the source voltage, the sensed output voltage is negative, the switching pulses are selected such that upper switches of secondary remains turned on while lower switches Q52-Q82 switches continuously.



(a)



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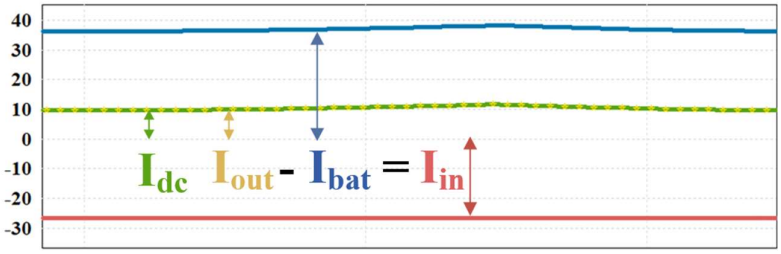
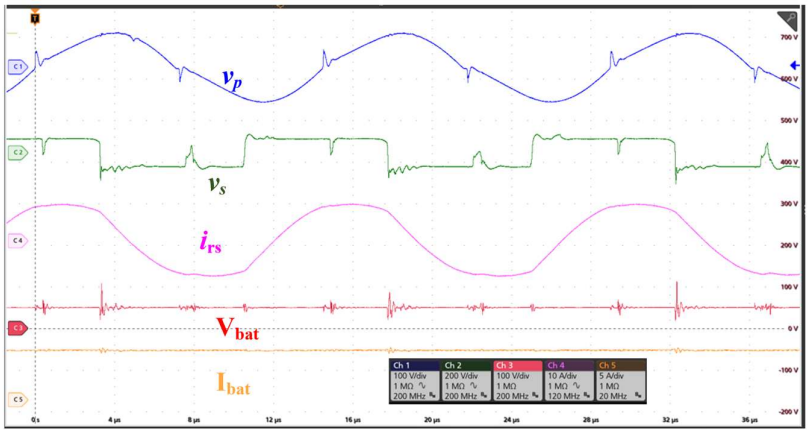


(c)



(d)

Fig. 5.10 Key waveforms for charging operation in buck mode (a) Transformer primary secondary and primary inductor current (b) Terminal Voltages at different ports (c) System and converter currents and (d) Experimental results for $V_{bat} = 50\,V$.

5.4.3 Operation in Boost Mode: Reverse Power Flow

To demonstrate the operation reverse mode operation in boost mode, the converter operates with leading phase shift for secondary voltage with respect to primary. The key waveforms in this mode are presented in Fig. 5.11.

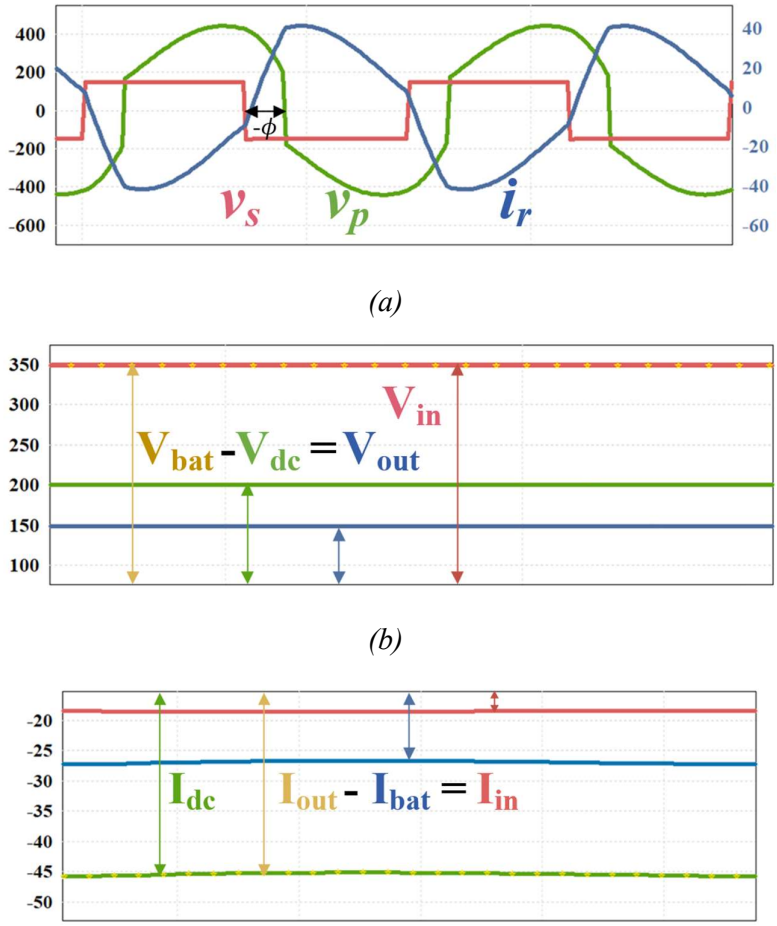


Fig. 5.11 Key waveforms for discharging operation in boost mode (a) Transformer primary secondary and primary inductor current (b) Terminal voltages at different ports (c) System and converter currents.

5.4.4 Operation in Buck Mode: Reverse Power Flow

To demonstrate the operation reverse mode operation in buck mode, the converter operates with leading phase shift for secondary voltage with respect to primary, however with negative output voltage, resulting in desired buck mode discharging. The key waveforms in this mode are presented in Fig. 5.12.

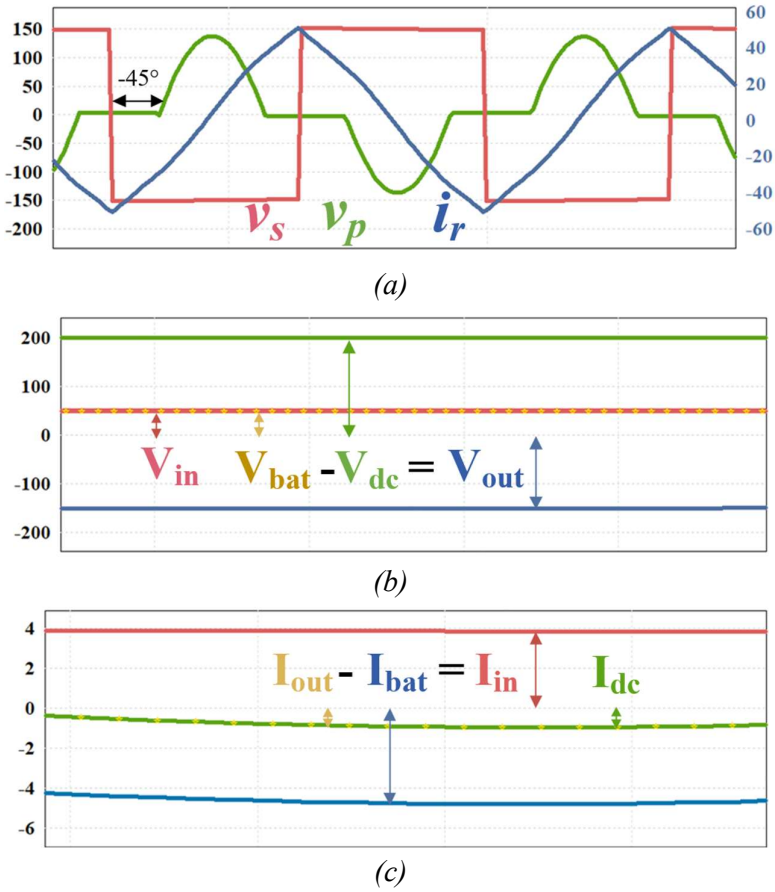


Fig. 5.12 Key waveforms for discharging operation in buck mode (a) Transformer primary secondary and primary inductor current (b) Terminal voltages at different ports (c) System and converter currents.

5.5 Conclusion

This fractional power processing concept is of significant importance in applications dealing with high power level. However, its implementation in practical EV landscape becomes challenging due to wide range of battery available in the market. The conventional approach to extend the available charging voltage range required converter design to be done for relatively large power, depreciating the benefits of FPP concept. To solve the above challenges the proposed issue of limited voltage range, the proposed quad-operative fractional power processor enables buck, boost operation in both charging and discharging mode, while also reducing the fractionality ratio by half. The proposed concept is verified through simulation results. Experimental validation of the proposed concept is presented using a scaled down laboratory prototype.