Chapter-1

Introduction and Organization of the Thesis

1.1 Introduction

1.1.1 Scaling and Power Challenges

Gordon Moore predicted in 1975 that the transistor count in a semiconductor-based integrated circuit will double every two years, popularly known as Moore's law [1]. Later, Dennard's scaling rules [2] guided the integrated circuit (IC) manufacturers to successfully implement Moore's law, augmented with an increase in the clock speed with every new technology node. However, the trend of increasing frequency eventually broke down in the mid-2000s. Clock speed enhancement was a source of annual increased performance. When clock speeds could no longer be improved, we switched to multi-core processors. As seen in Figure 1.1, adding more cores does not result in a similar improvement in total performance. Ever since the clock frequency of microprocessors has settled around 3-4 GHz due to the inability to further scale down the supply voltage (V_{DD}) [3]. In Figure 1.2 as the technology node changed from 1.4 µm to 65 nm, the supply voltage has been reduced to 20 percent of its initial value but the threshold voltage has been reduced to half of its initial value i.e., 50 %. The threshold voltage did not follow the Dennard scaling and was failing to achieve the desired value. There are two main reasons for this. First, difficulty in reducing the supply voltage, and secondly rise in leakage current. Static power depends on leakage current and in modern chips static power contributes a significant amount to power dissipation [3]-[5]. Scaling the supply voltage in accordance with device dimension is known as constant field scaling (voltage scaling) in MOSFET and was given by R. Dennard in 1975 [2]. The

scaling in MOSFET is done in such a way that the electric field remains unchanged inside the device. If the device dimensions are scaled by a factor of γ, then the supply voltage should decrease by a factor of γ, and doping of the source and drain region should increase by a factor of γ. These rules have been roughly followed ever since, until rather recently. The reason for which Dennard's scaling rules [1] no longer work as well as they did in the past can be seen in Figure 1.2, which shows the scaling trend from the 1.4 μm node to the 65 nm node. While the supply voltage V_{DD} decreased to about 20% of its original value, the threshold voltage V_T only went down to approximately half of its starting value. That threshold voltage decrease did not happen as a natural result of Dennard scaling. It had to come about in other ways, such as changing the doping of the channel region under the gate. Since the electric fields inside a MOSFET stay nearly constant when the scaling rules are followed correctly, the threshold voltage stays nearly constant (saturated) as well, unless other changes are made. So, to keep the electric field inside the device constant, the threshold voltage (saturation) does not decrease significantly, due to which overdrive voltage i.e. (V_{DD}-V_{TH} (sat.)) decreases as shown in Figure 1.2. The decrease in overdrive voltage leads to a low drive current (on-current) and hampers the performance of MOSFET and a low I_{ON}/I_{OFF} ratio. There are two possible solutions to overcome the problem of low drive current either V_{DD} can be kept high during constant field scaling or lower the V_{TH} value while using constant field scaling. Both the possible solutions along with the problems associated with them will be discussed further. When the scaling of supply voltage is done in accordance with the device dimensions to follow constant field scaling; the power density $I_{ON}V_{DD}/A$ (where A is the surface area of the device) of the device remains the same and therefore, the energy needed and the heat produced by the device remains unchanged [3]. V_{DD} scaling has been reduced dramatically to maintain appropriate levels of gate overdrive voltage.

When the supply voltage is reduced in step with the device size, the power density $I_{ON}V_{DD}/A$ (ON-current times supply voltage divided by surface area) remains constant, implying that the energy required to drive the chip and the heat produced by the chip remains constant [3]-[5]. This assumes that as the devices are scaled-down, chip size doesn't shrink rather, with each generation complexity and capability of the chip have been increased, and the chip size stays more or less constant. In order to overcome the reduction in power supply, another scaling theory namely the constant voltage theory was introduced in the literature [6]. According to these scaling rules, all the device dimensions are scaled down by the factor 'γ' with the increased doping concentration by the factor 'γ' similarly to those of constant electric field scaling rules except for the supply voltage kept constant in the former case. This scaling principle leads the speed of the device by a factor of 'γ^2' at the cost of increased power dissipation by a factor 'γ'. Thus, the constant field scaling is suitable for high-speed applications at the cost of increased power dissipation in the device. The effects of constant field and constant voltage scaling on various parameters of the device have been compared in Table 1.1. Note that the increased doping concentration by the factor of 'γ' in the scaling leads to the degradation of the mobility of the carriers due to increased impurity scattering [6] [7]. Further, the higher switching speed is achieved at the cost of increased power dissipation in the constant voltage scaling. Y. Taur and T. H. Ning have proposed a generalized hybrid scaling theory obtained by mixing the principles of the constant field and constant scaling rules for optimizing the device performance for high-speed and low-power applications [7].

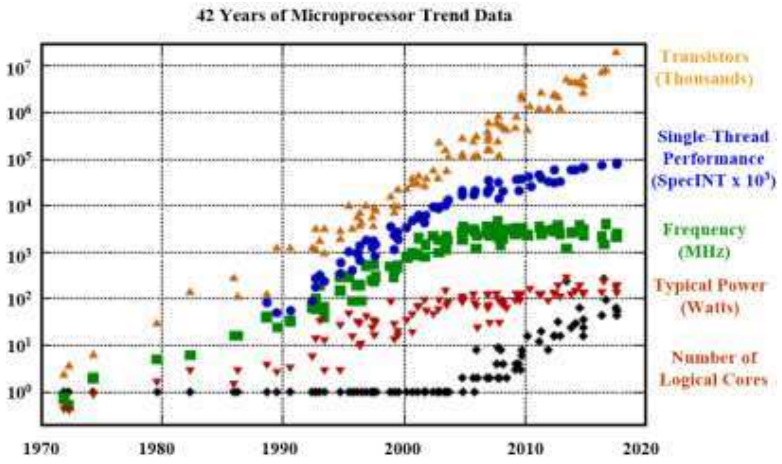

Figure 1.1 Microprocessor trends based on 42 years of experimental data [3].

Apart from the physical scaling outlined earlier in this chapter, application-dependent power dissipation becomes one of the key issues limiting the integration of scaled devices, limiting the utility of continued scaling [8] [9]. There are three types of power dissipation methods in VLSI circuits: dynamic or switching power, the short current produced power and static power dissipation.

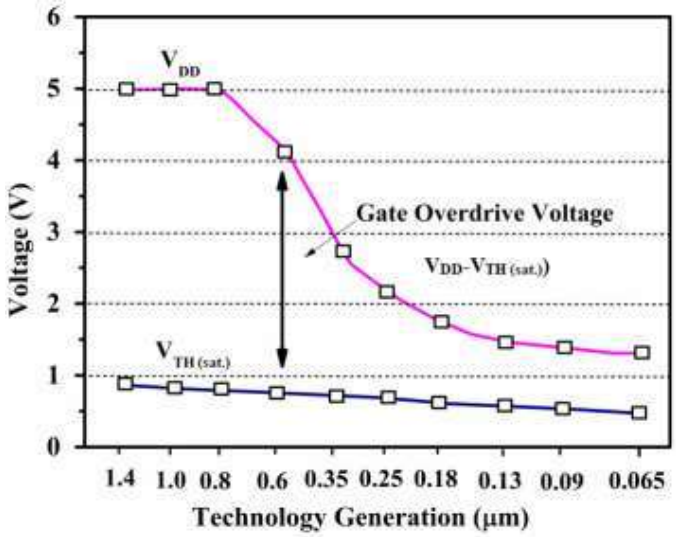

Figure 1.2 The trend of supply voltage and threshold voltage scaling vs. technology generation. V_{DD} decreases with device dimensions, but V_T does not. From [2].

The total power dissipation, P_T, of an integrated circuit is calculated as follows:

$$P_T = \sum (P_D, P_{sh}, P_{st}) \quad 1.1$$

When V_{DD} doesn't scale down, power density increases instead. For each MOSFET, the dynamic and static power consumption can be expressed as [8]

$$P_D = fC_L V_{DD}^2 \quad 1.2$$

where f is the operating frequency and C_L is the total load capacitance

$$P_{sh} = V_{DD}.I_{short} \quad 1.3$$

This is the power dissipation caused by short circuit currents. This is generally determined by the circuit's architecture. Typically, this is not the most important component of power dissipation. The static power expression is given by Eqn: 1.4.

$$P_{st} = I_{leakage}.V_{DD} \quad 1.4$$

where $I_{leakage}$ is the total leakage current in the off-state of the MOSFETs. So, it can be seen from the above equation that both the dynamic and the static power depend on the supply voltage (V_{DD}) and if we do not scale the supply voltage with the constant field scaling, that is if we increase $V_{DD,}$ power dissipation will increase.

In figure 1.3 it can be seen that in modern ICs or for lower technology nodes, the static power contributes a significant amount to the power dissipation. So, when we try to scale the threshold voltage aggressively, the leakage current will also increase. Subsequently, the static power dissipation will also increase. Figure 1.4 demonstrates that the proportion of the static power dissipation in 65 nm technology node circuits is higher than in prior technology nodes [8] [9]. The static power dissipation at the 45 nm technology node is expected to account for more than half of the total power consumption (see Figure 1.4). Beyond the 65 nm technology node, the ITRS requirement of maximum permissible power dissipation is also indicated in the graph and has been kept constant (P_T =198W).

For each technology generation, the experimental data in the bar graph corresponds to 30-meter-wide transistors [10].

TABLE 1.1 Scaling of the device dimensions and circuit parameters [10].

Device Parameters		**Multiplication Factor, $\gamma > 1$ Scaling parameter, α**			
		Constant Field Scaling	**Constant Voltage Scaling**	**Generalized Scaling**	
Primary Scaling	Device dimension (t_{ox} L, W)	$1/\gamma$	$1/\gamma$	$1/\gamma$	
	Doping concentration (N_s, N_a)	γ^2	γ^2	$\alpha\gamma$	
	Voltage (V)	$1/\gamma$	1	α/γ	
Derived Scaling Behavior of Transistor	Electric field (E)	1	γ	α	
	Depletion Layer width (W_d)	$1/\gamma$	$1/\gamma$	$1/\gamma$	
	Capacitance (C)	$1/\gamma$	$1/\gamma$	$1/\gamma$	
	Inversion/Layer charge density (Q_i)	1	γ	1	
				Long channel	**Velocity Saturation**
	Carrier velocity (v)	1	γ	α	1
	Drift current (I_{drift})	$1/\gamma$	γ	α^2/γ	α/γ
	Channel resistance (R_c)	1	$1/\gamma$	α^2/γ	α/γ
Derived Scaling Behavior Of Circuit	Circuit delay time	$1/\gamma$	$1/\gamma^2$	$1/\alpha\gamma$	$1/\gamma$
	Power dissipation per circuit	$1/\gamma^2$	γ	α^3	α^2/γ^2
	Power density	1	γ^3	α^3	α^2
	Power-delay product per circuit	$1/\gamma^3$	γ	α^2/γ^3	

As discussed earlier, the different components of the leakage currents are the key scaling limiting factors. All the three major tunneling leakage currents (gate oxide, source-to-drain, and band-to-band tunneling of electrons or holes) will contribute to the ever-increasing power density of VLSI circuits for high-performance devices. The reason for this is that high-performance devices have a greater power supply voltage than the low operating power (LOP) transistors. As a result, regulating leakage current in the individual devices and designing power-optimized VLSI circuit topologies remain the primary concerns for next-generation device research and development.

1.1.2 Limitation of MOSFETs

Continuous downscaling in device dimension to fulfill the demands of present semiconductor technology by introducing high speed and low power devices is pushing the CMOS technology to the ultimate nanoscale dimension [14]-[17]. Although scaling is adopted to meet the technological requirements, there are several issues in MOSFETs that need to be addressed as device dimensions have reduced over time [17]-[20]. This section presents an overview of such problems that exist. There is one important parameter that can't be scaled.

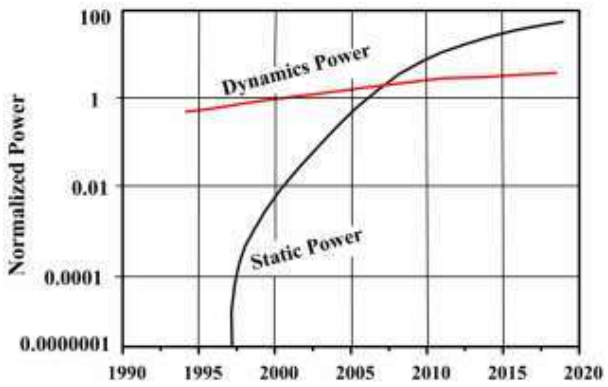

Figure 1.3 Trends of dynamic and static CMOS power, showing that static power [11].

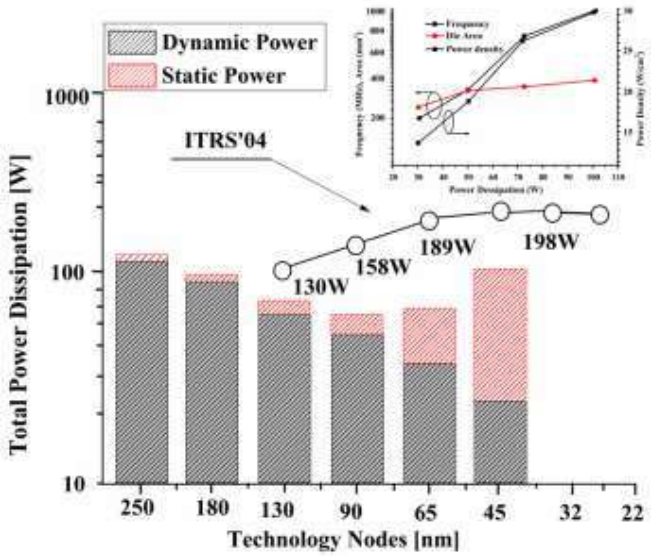

Figure 1.4 Total power dissipation as a function of technology node, including an illustration of how the static power dissipation increases when technology advances to 65nm and beyond due to the large increase in the off-state current [12] [13].

The subthreshold swing (SS) of a transistor is defined as the amount of gate voltage required to decrease the drain current by one order of magnitude [21]-[23]. It determines the quality of the switching action of a transistor and is mathematically expressed as [24]:

$$SS = \frac{dV_{GS}}{d\left(\log_{10} I_{DS}\right)} \approx 2.303 \frac{kT}{q}\left(1 + \frac{C_{ox}}{C_{dep}}\right) \tag{1.5}$$

where V_{GS}, I_{DS}, C_{OX}, and C_{dep} are gate voltage, drain current, oxide capacitance, and depletion capacitance, respectively.

Thermal Voltage, KT/q, is not scalable. Although the capacitance is scaled down by a factor γ (Table 1.1), their presence in a ratio eliminates any factor associated with the result. As a result, *SS* remains unchanged when the device is subjected to scaling. When the transistor dimensions and voltages are scaled-down, the SS in the scaled device from a higher percentage of the total voltage available to switch off the transistor as compared

to the case when the device dimensions and the voltages were not scaled. The non-scaling property of the subthreshold characteristics is of concern to the digital circuits.

Dennard *et al*. reported in their analysis that the threshold voltage also scales by the same factor as the dimensions in the constant field scaling principle. However, a drastic decrease in the threshold voltage means that the transfer characteristics shift to the left on the positive gate voltage axis. This increases the possibility of a higher OFF-state current in the scaled device. This, however, can be addressed in the generalized scaling principle by adjusting the two scaling factors, γ, and α.

From a perspective concerning the geometry of a conventional MOSFET, scaling reduces the length between its source and drain regions. When the junction's widths associated with the source and drain regions become comfortable with the channel length, the device is said to possess a short channel. Such devices exhibit non-ideal traits arising out of the presence of a significant longitudinal electric field (parallel to the direction of current flow) in addition to a transverse electric field (normal to the current flow) as compared to the dominant transverse electric field and negligible longitudinal field in long channel devices [23]-[26]. This longitudinal field is due to the source and drain regions which act like controlling electrodes similar to the gate in scaled devices. Due to this several adverse effects appear in MOSFETs, which cannot be predicted by the theory of long channel devices, and are collectively known as short channel effects. Threshold Voltage roll-off, drain-induced barrier lowering (DIBL), and mobility degradation are the most notable amongst them. Such effects have led to serious concern for MOSFET as the industry proceeds for smaller dimensions.

1.1.3 The Emergence of Alternative Devices

The inability of the MOSFETs to withstand downscaling has led the researchers and research groups to look for novel devices which may be considered as alternatives to the

MOSFETs. The 2015 edition of the ITRS, in its document, 'Beyond CMOS', presents a map of emerging devices considered as future replacements of the MOSFETs; the same is reproduced in Figure 1.5 [27]. These devices have been classified into conventional or novel structures or novel materials. This section discusses some of the most important devices of this map, relevant to this thesis, with more emphasis on conventional charge-based devices which are the closest counterparts of MOSFETs.

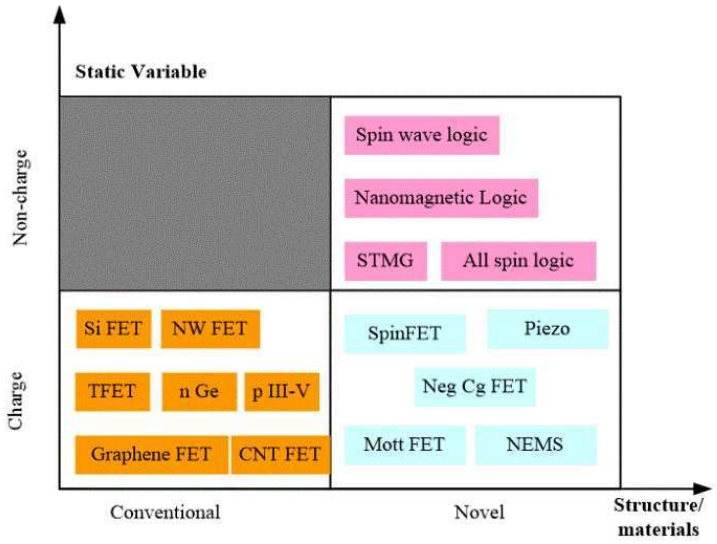

Figure 1.5 Taxonomy of options for emerging logic devices as mentioned in ITRS 2.0 2015 edition [27].

1.1.3.1 Carbon Nanotube FETs

A carbon nanotube FET (CNTFET) is a field-effect transistor that differs from typical MOSFET construction using a single carbon nanotube or an array of carbon nanotubes as the channel material, as shown in Figure 1.6. The carbon nanotube FET (CNT FETs) [28]-[29] have shown positive developments in applications and areas where other semiconductor devices have failed in sub-10 nm technology. This is attributed to the ultrathin dimensionality of carbon nanotube, the excellent energy bandgap of around 0.6 eV – 0.8 eV, and room temperature ballistic transport of charge carriers. The CNT FETs are primarily used as Schottky barrier transistors for both n- and p-mode of transport.

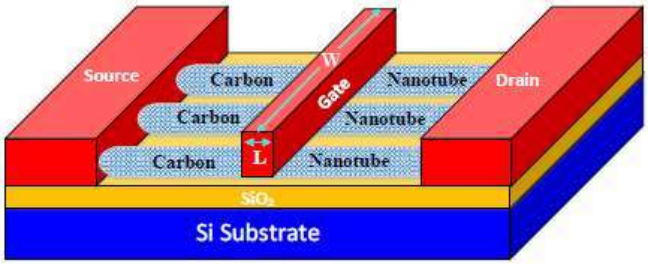

Figure 1.6 Schematic of a Carbon Nanotube Field Effect Transistor (CNTFET) [28].

1.1.3.2 Graphene FETs

Another material modification in conventional FET is Graphene FET (GFET) [30]-[32] which offers higher carrier mobility than carbon nanotubes. Graphene possesses zero bandgap which is the cause for extremely poor ratios of ON and OFF-state currents. Research is being carried out to develop methods to widen its bandgap. Graphene FETs are expected to be useful for RF applications. Figure 1.7 shows the Graphene FET (GFET) which is composed of a graphene channel between two electrodes with a gate contact to modulate the electronic response of the channel.

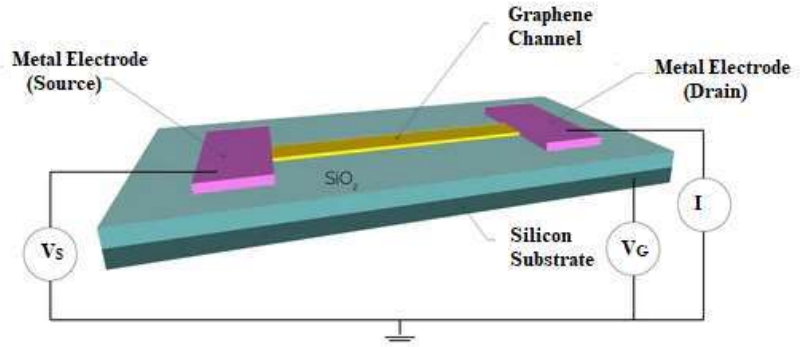

Figure 1.7 Schematic of a Carbon Nanotube Field Effect Transistor (CNTFET) [30].

1.1.3.3 Nanowire FETs

Figure 1.8 shows the schematic diagram of nanowire FETs (NWFETs) [33]-[35]. They are structures where the channel of a conventional MOSFET is replaced with semiconducting nanowires of a wide variety of materials: Group IV (Si, Ge), Group III-V

compound semiconductors (AlN, InN, GaP, InP), Group II-VI materials (CdSe, ZnSe, CdS), and semiconducting oxides (ZnO, TiO_2). As the diameter of these nanowires is reduced, they exhibit ballistic conduction. Subthreshold swing (SS) close to 60 mV/decade has been demonstrated for gate-all-around geometries. Many developments have been reported [28] till date on the use of nanowire FETs in several circuits. However, the commercialization of the devices is a major challenge.

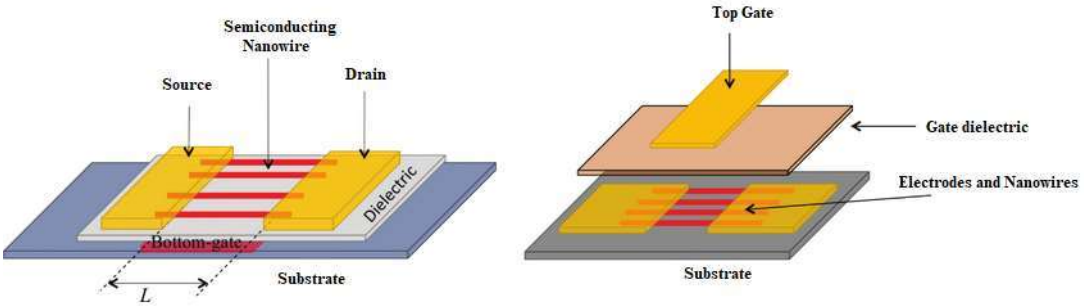

Figure 1.8 Schematic of a nanowire field-effect transistor (CNTFET) [35].

1.1.3.4 Negative Gate Capacitance FETs

The negative gate capacitance FETs [36]-[37] are another class of devices where ferromagnetic materials used as the gate dielectric in conventional charge-based devices may help to achieve amplification of gate voltage as shown in Figure 1.9. The most commonly used dielectric is the HfO_2 doped frequently with constituents like Zr, Al, or Si. These FETs are reported to have sub-60 mV/dec due to the possibility of low voltage operation. The chief advantage of this device is its geometrical similarity to the conventional devices.

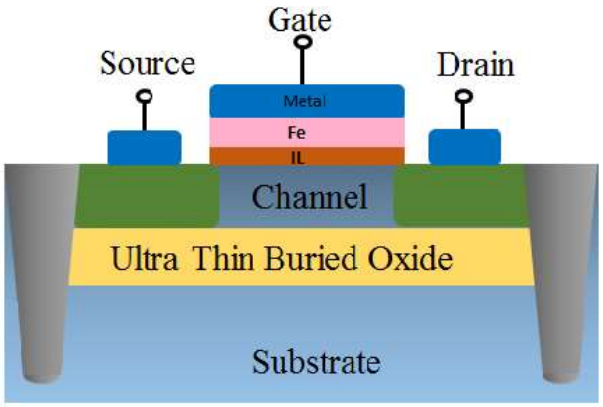

Figure 1.9 Schematic of a negative gate capacitance field effect transistor (NGC-TFET) [37].

1.1.3.5 Tunnel Field Effect Transistors (TFETs)

As the size of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) is reduced to the nanoscale, we have an electronic unit with more components. It consumes more energy, making power consumption a major issue [3] [4] [5]. However, lowering the supply voltage is extremely difficult due to the transport mechanism of typical MOSFETs, which is governed by carrier diffusion through a heat barrier [5] [6]. Even in the best-case scenario, MOSFET sub-threshold swing is limited by 60 mV/dec [21] [22] [24]. The tunnel field-effect transistor (TFET) is a form of transistor that has been used in research. Despite its structural similarities to a metal-oxide-semiconductor field-effect transistor (MOSFET), the fundamental switching mechanism is different [38] [39] [40]. Therefore, TFET is one of the counterparts of the MOSFET targeted for low power applications, and it is considered a promising solution because its transport mechanism is under quantum mechanics, unlike MOSFETs, which operated by the mechanism of thermionic emission (classical mechanics) as depicted in Figure 1.10. A conventional TFET geometry and its ON-state and OFF-state energy band diagram are shown in Figure 1.11 and Figure 1.12, respectively [38].

1.1.3.5.1 Physics and Operation of TFETs

The biasing conditions of p-type and n-type TFETs ate tabulated in Table 1.2. In n-TFET, the application of positive gate voltage suppresses the energy bands at the p+ source and i-channel junction causing the valence band of the source to line up with the conduction band of the channel. The tunnel barrier is approximated as a triangular barrier with reduced tunnel width [38]-[42]. The electrons from the valence band of the source tunnel through the barrier into the conduction band of the channel, and are finally collected by the n+ drain through a positive bias. The Band to Band Tunneling phenomenon provides an expression for carrier tunneling transmission and can be achieved by using the Wentzel Kramers Brillouin (WKB) approximation and considering the tunnel barrier as a triangle-shaped potential barrier, as shown in Figure 1.13.

TABLE 1.2: Modes of operation in TFET, convention of source and drain regions, and biasing condition [38].

Mode of Operation	Source	Drain	Biasing Condition
p-type TFET	n+	p+	$V_{GD} < 0$; $V_{SD} < 0$
n-type TFET	p+	n+	$V_{GS} > 0$; $V_{DS} > 0$

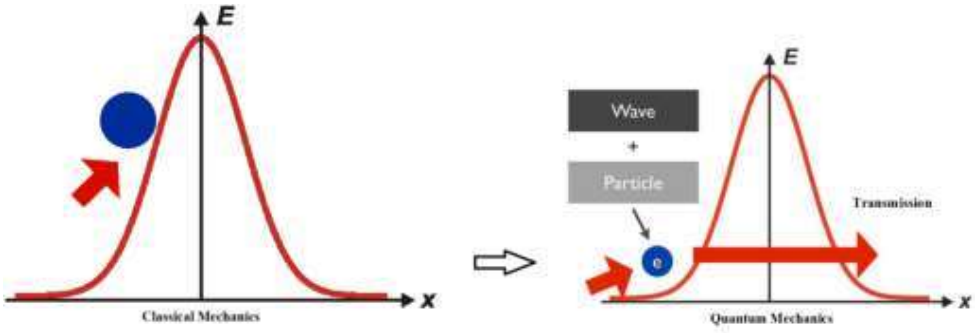

Figure 1.10 Plots of classical and quantum charge carrier transmission mechanism [43].

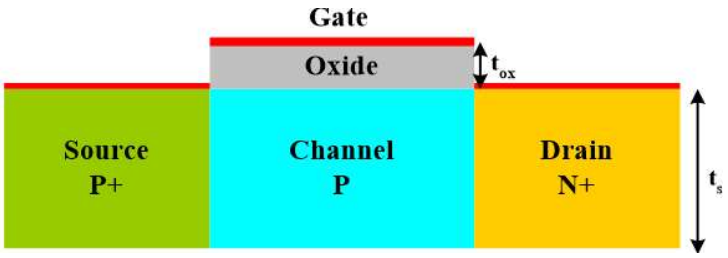

Figure 1.11 Schematic structure of conventional TFET [38].

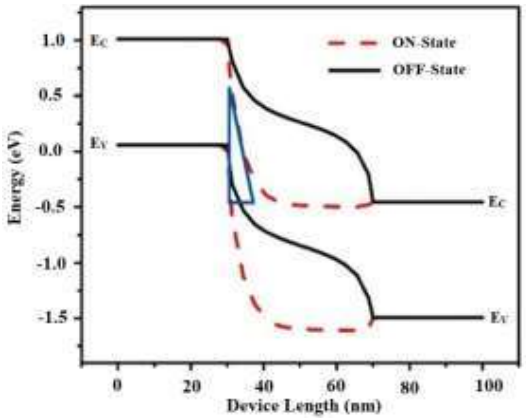

Figure 1. 1 Energy band diagram of conventional TFET in ON and OFF-state [38].

The Band to Band Tunneling transmission is given by the following expression using the WKB approximation.

$$T_t \approx exp\left[-2\int_{x_1}^{-x_2}\left|k(x)\right|\partial x\right] \tag{1.6}$$

where *k(x)* is the quantum wave vector of the electron inside the triangular barrier and given by

$$k(x) \approx \sqrt{\frac{2m^*}{h^2}(PE-E)} \tag{1.7}$$

where m^* is the electron effective mass and $\hbar$ is derived from Planck's constant.

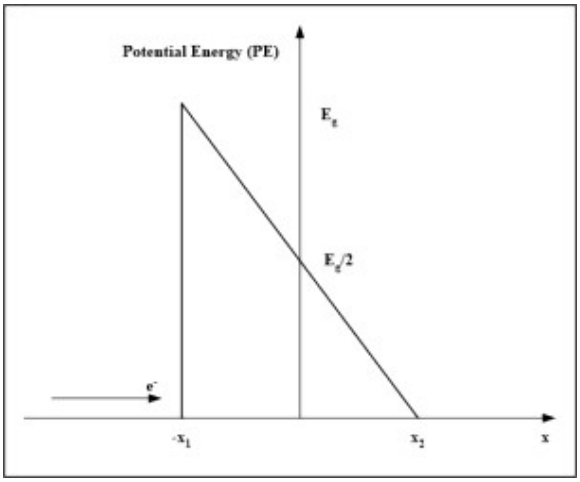

Figure 1.13 Shows the tunnel barrier as a triangular-shaped potential barrier [44].

Figure 1.13 shows the triangular energy barrier of electrons in a TFET. Along the device length, the PE of the electrons reduces from the energy bandgap at tunnel junction (E_g) to zero. At the width of the triangle, the term E is zero. The rate of reduction in PE can be expressed as $^{E_g}/_{2} - qF_x$, where E_g is the bandgap of the semiconductor material at the tunnel junction and F is the electric field measured in V/m (the new term (F) has the unit of eV/m), and therefore we must also cancel out an electron charge [45]. Hence, the approximate expression for PE is:

$$k(x) \approx \sqrt{\frac{2m^*}{h^2}\left(\frac{E_g}{2} - qF_x\right)} \tag{1.8}$$

Now, this expression can be used with Eqn: 1.6 to obtain the expression below:

$$T_t \approx exp\left[-2\int_{x_1}^{-x_2}\left(\frac{E_g}{2} - qF_x\right)\partial x\right] \tag{1.9}$$

Expanding the above equation gives:

$$T_t \approx exp\left[\frac{4}{3}\frac{\sqrt{2m^*}}{qEh}\left(\frac{E_g}{2}-qF_x\right)^{3/2}\right]\Bigg|_{-x_1}^{x_2} \tag{1.10}$$

Looking back at the triangular barrier, we know that at x = - x_1, ($\frac{E_g}{2}-qF_x$) = E_g, and that at x = x_2, ($\frac{E_g}{2}-qF_x$) = 0,

$$T_t \approx exp\left(-\frac{4\lambda}{3}\frac{\sqrt{2m^*}}{h(\Delta\phi+E_g)}\left(E_g\right)^{3/2}\right) \tag{1.11}$$

Eqn: 1.11 is a general expression for band-to-band tunneling transmission. This equation can be improved slightly by making it more specific to the tunneling transistors. In Figure 1.12, the height of the triangle along the y-axis is $\Delta\phi+E_g$, and a screening length λ refers to the spatial extent of the electric field [46]. $\Delta\phi$ is the energy range over which tunneling takes place. There are four important conditions for band-to-band tunneling to take place: (i) available states to tunnel from (ii) available states to tunnel to (iii) an energy barrier that is sufficiently narrow for tunneling to take place, (iv) conservation of momentum [44]. λ can be expressed in the terms of the gate oxide dielectric material (ε_{ox}), thicknesses of the gate dielectric (t_{ox}) and thickness of the body of the device (t_{si}), and gate geometry. λ is expressed in the following equation [47]:

$$\lambda = \sqrt{\frac{\varepsilon_{si}t_{si}t_{ox}}{2\varepsilon_{ox}}} \tag{1.12}$$

1.1.3.5.2 Subthreshold Swing (*SS*) in TFETs

The purpose of describing the above expression is to demonstrate that the subthreshold swing (*SS*) of a TFET differs from that of a MOSFET in terms of parameter dependency. To describe the expression for the subthreshold swing of a band-to-band tunneling device, consider the BTBT current given below [44], [48] for a reverse-biased p-n junction.

$$I = aV_{eff}E_e^{\frac{-b}{E}} \tag{1.13}$$

where

$$a = Aq^3\frac{\sqrt{\frac{2m^*}{E_g}}}{\pi^2 h^2} \tag{1.14}$$

where A is the device's cross-sectional area and

$$b = 4\sqrt{m^*}\frac{E_g^{3/2}}{3qh} \tag{1.15}$$

V_{eff} is the bias at the tunnel junction and E is the electric field at the tunnel junction [22]. Then from the Eqn: 1.13, the sub-threshold swing is calculated as $SS = \frac{\partial V_{GS}}{\partial(\log I_{ds})}$ this result [22] in

$$SS = ln(10)\left[\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{GS}} + \frac{E+b}{E^2}\frac{dE}{dV_{GS}}\right]^{-1} \tag{1.16}$$

There are two terms in the denominator of Eqn: 1.13, which can be maximized to achieve a low sub-threshold swing, and these terms are not limited by kT/q. According to the first term, TFET should be engineered so that the gate-source voltage directly controls the tunnel-junction bias V_{eff} and this depends on the TFET geometry with a thin and/or high dielectric gate material and an ultra-thin body to assure that the gate field directly modulates the channel. For an equivalent oxide thickness approaching 1 nm, $\frac{dV_{eff}}{dV_{gs}} \approx 1$ and the first term in the denominator of Eqn: 1.13, which is approximately inversely related to V_{gs}.

1.1.4 Evolution of Tunnel Field Effect Transistors (TFETs)

Stuetzer invented the first TFET in 1952, before the invention of Esaki tunnel diodes when he built a p-n junction and explained its operation under reverse bias conditions

[50]. He termed it as 'fieldistor.' He has discussed the effect of the control electrodeposition on device characteristics, demonstrating the presence of ambipolarity in the device. Quinn *et al*. proposed the concept of a surface tunnel junction in 1977 by replacing a MOSFET's degenerated n-type source with a highly degenerated p-type source [51]. The requirement of an abrupt junction and maximum band bending was reported in this work. The main focus of the work was subband splitting near the tunnel junction and the scope of experimentally determining the phenomenon. Banerjee *et al*. presented a three-terminal device in 1987 and reported the presence of Zener tunneling [52]. The authors calculated the tunneling current by approximating the tunnel barrier as of triangular shape, Takeda *et al*. proposed and characterized a band to band tunneling MOS device, and highlighted the negligible short channel effects associated with the 'Silicon quantum device' [53]. In 1992, Baba proposed the surface tunnel transistor (STT), an alternative version of Quinn's device where he commented on the use of a gate to control negative differential resistance (NDR) in the forward-biased state [54]. In 1995, Reddick and Amartunga proposed a gate-controlled p^+-p-n^+ structure of STT, and proposed experimental as well as simulation results to explain interband tunneling in STTs [55]. They have also presented the basic formula for barrier height at the tunnel junction, which finds its use in the analytical modeling of TFETs. In 1996, Uemura and Baba first demonstrated NDR in two planar-type surface tunnel transistors based on GaAs and InGaAs [56]. The gating of the vertical TFET was proposed by Hansch *et al.* in 2000 [57]. In 2004, the silicon on insulator TFET was first proposed by Aydin *et al*. [58]. The tunneling mechanism of transport in TFETs allows them to possess a subthreshold swing (SS) lesser than the thermal limit of 60 mV/dec in MOSFETs. The tunnel barrier act as a filter that prevents the passage of high and low-energy Fermi tails, whereas, in MOSFETs, thermionic emission allows the transmission of high energy Fermi tails.

TFETs also exhibit low off current due to their mechanism of carrier transport [59]. Short channel effects are minimized owing to the dependence of the total current on the tunnel current concentrated at the tunnel junction. The advantage of TFET is its compatibility with CMOS fabrication techniques. TFETs, however, are not free from disadvantages. Due to their reverse-biased geometries and mechanism of transport, they have a low ON-current [60]. Ambipolarity is another undesirable property of TFETs [60]. The most significant drawback in TFETs is the dominance of their gate-to-drain capacitances which contribute to Miller Capacitances in the digital circuits [61]-[62].

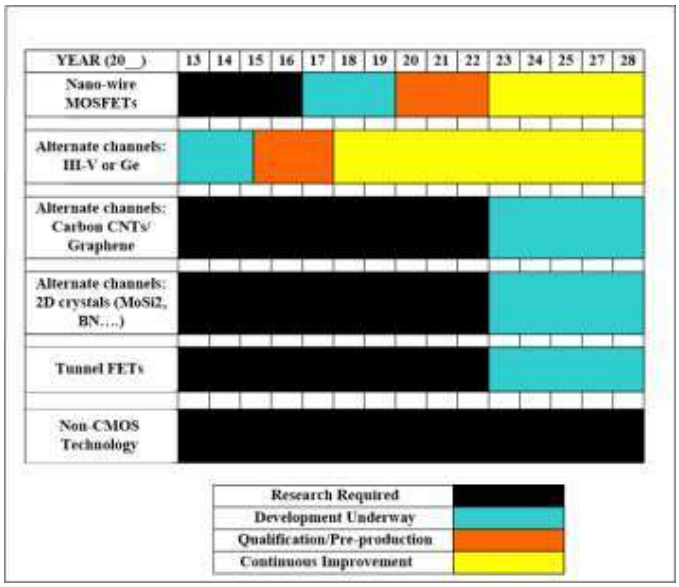

Figure 1.14 Mention of tunnel FET in process, integration, and devices section of ITRS Report, 2013 [63].

Figure 1.14 discusses the evolution of TFETs, showing research from the early period of TFETs to date. The discussion here is purely speculative, intending to improve the readability of the otherwise complex distribution of significant works of TFETs over time. The same is true for the other sections, which are divided chronologically according to the representative diagram shown in Figure 1.15.

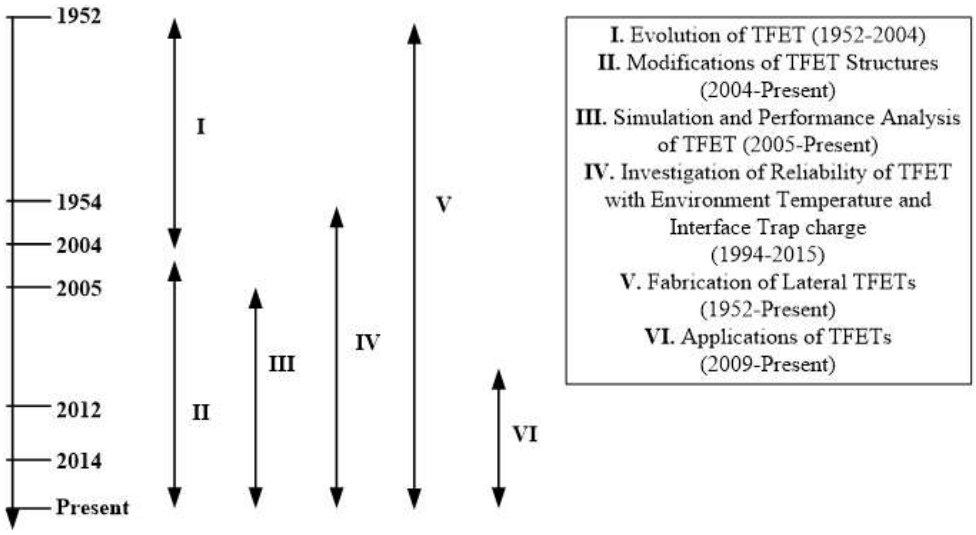

Figure 1.15 A chronological division of the literature survey taken under this chapter.

1.1.5 Adopted Technologies

There are different kinds of technologies (engineering) that have been adopted for designing the studied TFETs structures such as gate oxide engineering, source material engineering/heterojunction engineering, and substrate engineering (selective buried oxide (SELBOX) to improve the TFET performance. These engineering techniques have been discussed in the following subsections.

1.1.5.1 Gate Oxide Engineering

The gate oxide is a dielectric layer that separates the gate terminal from the underlying source and drains terminals, as well as the conductive channel that connects the source and drain regions when a transistor is turned on. By implementing certain modifications to the gate oxide, we can improve the performance of the TFET which is generally known as gate oxide engineering. Some gate oxide engineering is explained below in detail.

1.1.5.2 SiO_2/High-k Gate Stacked Engineering

Due to the reduction of the SiO2-based gate oxide thickness in bulk MOSFETs as a result of continuous scaling, the gate leakage current has been dramatically increasing. Thus as

per the demand for scaling the use of ultra-thin gate dielectrics (H. S Momose 1998) may lead to excessive static power dissipation in the MOS devices [64]. The gate leakage can be reduced by using high-k dielectric material as the gate oxide in the device. Note that the gate oxide capacitance per unit area is given by $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ where ε_{ox} and t_{ox} are the permittivity and thickness of the oxide layer respectively. For a fixed gate oxide capacitance, the physical thickness of high-k material is given by$t_{hk} = t_{ox}\left(\frac{\varepsilon_{SiO_2}}{\varepsilon_{hk}}\right)$, where ε_{SiO2} is the permittivity of silicon, ε_{hk} is the permittivity of high-k dielectric material and t_{ox} is the actual SiO_2 oxide thickness required to achieve the desired oxide capacitance in the bulk MOS device [65]. In recent years, material like Si_3N_4 (k = 7), HfO_2 (k = 25), ZrO_2 (k = 29), Ta_2O_3 (k = 26), $HfSiO_4$ (k = 27) and TiO_2 have come up as strong replacement of SiO_2 when channel length scaled down to sub 20 nm.

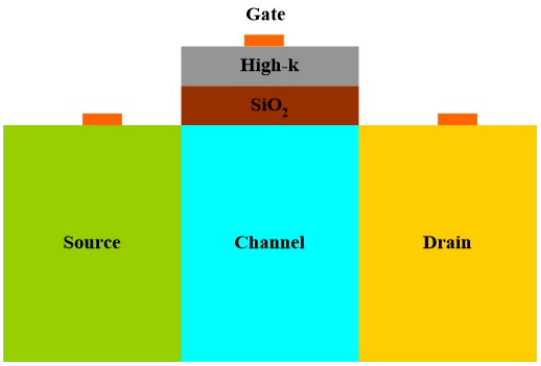

Figure 1.16 Schematic structure of conventional TFET with SiO_2/High-k gate stacked engineering.

For the improvement of the ON-state current and reduction of gate leakage current of the TFET vertical and gate stacking of SiO_2/high-k oxides are used, S. Kumar *et. al*. have proposed a double gate TFET with SiO_2/HfO_2 vertical gate stacked DGTFET structures [66]. In this thesis, we have adopted a vertical gate stacked (GS) SiO_2/high-k oxide structure technology for the designing of the proposed TFET structures as sown shown in Figure 1.16.

1.1.5.3 Ferroelectric Oxide Engineering

A ferroelectric FET incorporates a ferroelectric layer into the gate dielectric stack of a conventional metal-oxide-semiconductor field-effect transistor (MOSFET) [67]. Let's start by noting that the band-to-band tunneling rate in a TFET is strongly reliant on the gate capacitive coupling's control and the resulting barrier thinning. As a result, any further increase in the capacitance due to polarisation effects in a Fe material should affect the band-to-band tunneling conditions when increasing the gate voltage on the Fe gate stack of a TFET as shown in Figure 1.17 [68]. Due to its very low subthreshold current I_{off}, a Fe-TFET is projected to have much lower subthreshold power consumption than an existing Fe-MOSFET, allowing for far greater I_{on}/I_{off} [69]. The expected I_d–V_g characteristics of a Fe-TFET compared to a MOSFET and a TFET are shown in Figure 1.18; due to the band-to-band tunneling mechanisms, a very low I_{off} current, and a steep OFF-ON transition are expected, whereas hysteresis is expected due to the ferroelectric polarization. The abruptness of the OFF-ON transition can be even higher than that of a normal TFET at the same EOT because the electric field enhances polarization when the gate voltage is increased, enhancing capacitance coupling [69]. The *SS* of ferroelectric-related MOS devices is expressed as,

$$SS \approx \frac{\partial V_{GS}}{\partial(\log I_D)} = \underbrace{\frac{\partial V_{GS}}{\partial \psi_S}}_{m} \underbrace{\frac{\partial \psi_S}{\partial(\log I_D)}}_{n} = \left(1+\frac{C_s}{C_{ox}}\right)\frac{\partial \psi_s}{d\left(\log_{10} I_d\right)} \tag{1.17}$$

where, the gate oxide capacitance, channel-depletion capacitance, surface potential, and drain current are represented as C_{ox}, C_s, ψ_s, and I_d, respectively. The transistor body's factor, or factor m, is determined by the capacitance of the silicon body and the gate oxide capacitance. $m > 1$ for conventional oxide (i.e. SiO_2 and HfO_2), however, it can be lowered by replacing conventional oxide with the negative gate capacitance oxide.

MOSFET charge transport is completely dependent on factor *n*, which can be reduced by employing TFET because TFET carriers are transported by band-to-band tunneling rather than thermal excitation [69] [70] [71].

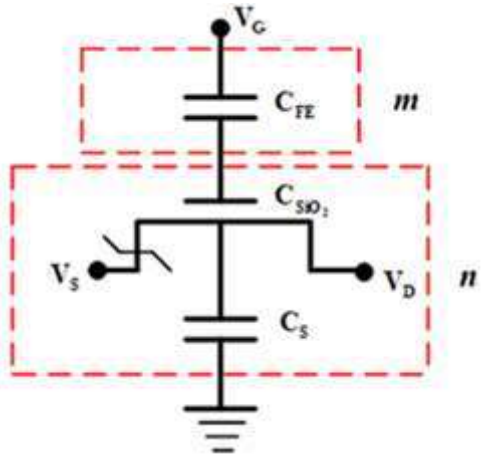

Figure 1.17 The Ferro dielectric TFET circuit diagram, which includes the TFET's C_{FE}, C_{SiO2}, and C_S [69].

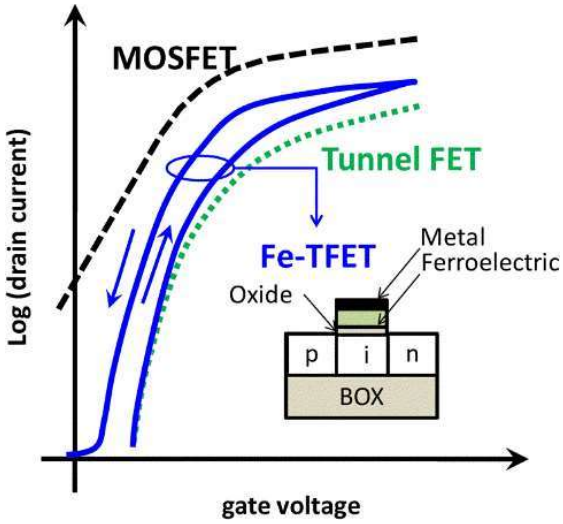

Figure 1.18 Log scaled drain current plots for different CMOS devices such as MOSFET, TFET, and Fe-TFET [69].

M. Ionescu *et al.* (2010) [68] demonstrated the manufacture and electrical characterization of ferroelectric tunnel FETs (Fe-TFETs). The low subthreshold power of band-to-band tunneling devices is combined with the retention features of Fe gate stacks

in this innovative family of hysteretic switches. M. H. Lee *et al*. (2014) [69] demonstrated an improvement in the swing range by extending the range of the steep subthreshold swing in tunnel field-effect transistors by 3.5 orders of magnitude using a ferroelectric PbZrTiO3 gate stack (by approximately double the slope).

1.1.5.4 Substrate Engineering

Due to the influence of the device's internal capacitance, the bulk transistor (Figure 1.19) has some constraints associated with relatively high power dissipation, short channel effects, and low speed. As a result, many techniques aimed at the device structure, such as fully-depleted SOI (FD-SOI) MOSFETs, have been proposed. This device benefits from an added isolation layer in the silicon substrate, as shown in Figure 1.19 (b), which can be built of silicon dioxide (SiO_2) and isolates the transistor active region from the substrate [72]-[74]. As a result, the parasitic capacitances (source/drain/gate parasitic capacitances) will be lowered, resulting in a faster operation speed. Vertical isolation is also a feature of SOI devices, which eliminates the leakage current. In addition, CMOS SOI's isolation from the substrate and adjacent devices minimizes the latch-up difficulties, which can result in shorting of the V_{DD} and GND lines and chip damage, and allows high device integration [73]. However, the self-heating and kink effect downsides of the FD SOI MOSFET cannot be overlooked. In both fully depleted (FD) and partially depleted SOI, the self-heating effect occurs. The kink effect, on the other hand, is exclusively seen in PD SOI MOSFETs. When the drain voltage is high, the kink effect occurs due to the high electric field near the drain. As a result, the body potential rises while the threshold voltage falls, resulting in a sudden increase in the drain current and device non-linearity [74].

As a result, the development of a novel device that combines the benefits of bulk transistors and SOI MOSFETs while also addressing their shortcomings has become a

need. The Selective-Buried Oxide (SELBOX) MOSFET is a novel device that works by placing a gap in the buried oxide isolation layer to minimize the body's potential OFF-state current [74] [75]. Figure 1.19 depicts the SELBOX MOSFET construction (c). Due to smaller internal capacitances, SELBOX MOSFETs have superior frequency characteristics, less short-channel effects, and faster operation speeds. Furthermore, the SELBOX MOSFET decreases the effect of self-heating [74]. Also, because of the SELBOX gap, thermal connection will be lowered because the gap acts as a parallel low resistance, lowering overall resistance. Furthermore, the gap reduces the kink effect by absorbing the holes created by the electric field, resulting in a lower body potential for the SELBOX MOSFETs than for the SOI MOSFETs [74] [75]. We believe that employing the SELBOX structure will reduce dynamic power dissipation because it reduces total device capacitance. On a selective buried oxide (SELBOX) substrate, D. Borah et al. (2019) present a new structure for the tunnel field-effect transistors [76]. The key characteristics of the suggested geometry of TFET on the SELBOX substrate and the conventional fully depleted silicon-on-insulator (FDSOI) TFETs were compared in a simulation study. It has been discovered that SELBOX can drastically reduce the device's OFF-state current while not affecting the device's ON-state current. The suggested work by S. Chaudhury et al. (2020) [77] combines the benefits of a hetero-stacked source and a selective buried oxide (SELBOX) structure in a single device. After analyzing crucial parameters, a performance comparison of the presented structure with existing structures was conducted. Drain current, sub-threshold swing, and capacitances are all investigated for the suggested structure.

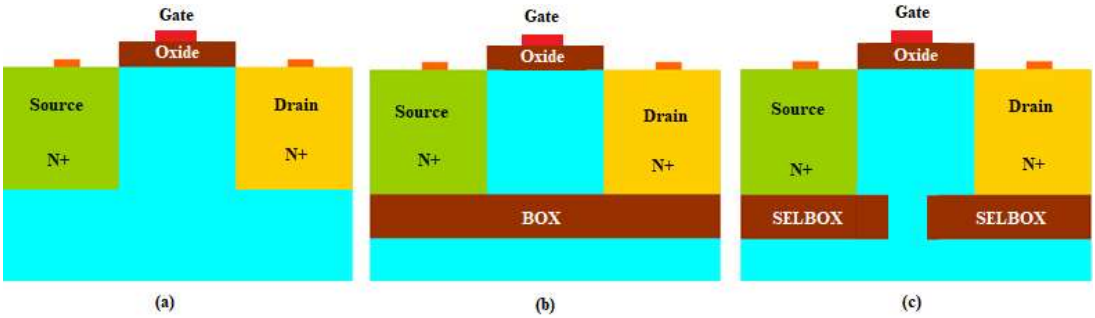

Figure 1.19 Schematic structures of (a) bulk NMOS, (b) FD-SOIMOSFET and (c) SELBOX MOSFET [74], [75].

1.1.5.5 Low Bandgap Source Material Engineering

The TFETs using a single material for their source channel and drain regions are called homojunction based-TFET devices [78]. However, when two different materials are used for the source and channel regions of the TFETs, they are called heterojunction-based-TFET devices [79]. An interface between two layers or regions of different semiconductors is known as a heterojunction [80]. In contrast to a homojunction, these semiconducting materials exhibit asymmetrical band gaps. Many solid-state device applications, such as semiconductor lasers, solar cells, and transistors, benefit from engineering electronic energy bands. A heterostructure is a device that combines many heterojunctions, though the two terms are often used interchangeably. The alignment of the energy bands at the interface determines the behaviour of a semiconductor junction. As shown in Figure 1.19, semiconductor interfaces can be classified into three types of heterojunctions: straddling gap (type I), staggered gap (type II), and broken gap (type III) [81]. In a Type-I (straddling gap) heterojunction, one material has both lower energy in the conduction band (CB), and higher energy in the valence band (V_B) than the other material as shown in figure 1.19 (a). In a Type-II (staggered gap) heterojunction, one material with lower energy in the conduction band, and higher energy in the valence band is found. Thus, electrons being collected at a lower energy in the conduction band, and

holes being collected at higher energy in the valence band, are confined in different spaces. A Type-III (broken gap) heterojunction is a special case of Type-II where lower energy in the conduction band for one material/side is lower than the higher energy in the valence band of other material/side. Here the conduction band overlaps with the valence band at the heterojunction interface; hence the name coined for this type of heterojunction is a broken gap. The low bandgap material such as germanium (E_g = 0.67 eV) is used as source material for the improvement of on-state current and subthreshold swing (*SS*). S. H. Kim *et. al*. Proposed TFET with Ge as a raised source material for the improvement of electrical performance [82]. The authors investigated the effect of thickness scaling on the band to band tunneling (BTBT) current in extended Ge source lateral TFETs. To limit tunneling to Ge exclusively, the Ge source is expanded by 2 nm inside the gate.

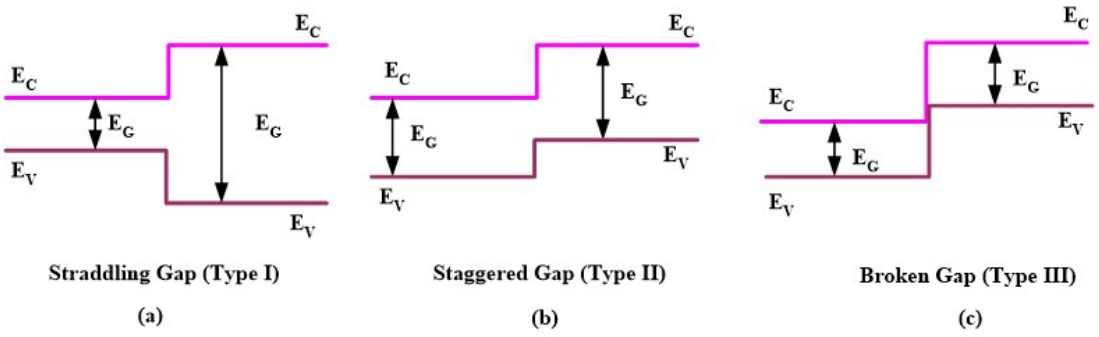

Figure 1.20 (a) Type-I or straddling gap heterojunction, (b) Type-II or staggered gap heterojunction, and (c) Type-III or broken-gap heterojunction [81].

1.1.6 Circuit and Biosensor Based Application Using TFETs

It includes the simulation of a TFET structure using the Silvaco TCAD tool to obtain its I-V and C-V characteristics and to compare it with standard MOSFETs. For use in simulations, the extracted I-V and C-V are placed in a 2-D lookup table. Because analytical models for TFETs are not publicly available, the simplest way to simulate

circuits is to use Verilog-A to create a lookup table-based model. In Cadence Spectre, the Verilog-A module is then used as an instance for circuit simulations.

1.1.6.1 Electronics Circuits Design Based on TFETs

The simplest option to simulate circuits is to use Verilog-A to create a lookup table-based model because there are no analytical models for TFETs. For both N and P-type TFET devices, a lookup table-based Verilog-A model is developed. This model is used to simulate the static and dynamic behaviour of digital circuits based on TFETs [83] [84] [85] [86]. The schematic of the Verilog-A transistor model is shown in Figure 1.21 from [83]. The model requires information on I_{ds}, C_{gs}, and C_{gd} for various values of V_{gs} and V_{ds}. A look-up table is generated based on Sentaurus 2-D simulation which provides the value of I_{ds}, C_{gs}, and C_{gd} for different values of V_{gs} and V_{ds}. It should be noted that the model used is for a device with a gate length of 30 nm. Note that the values of Q_s and Q_d are generated from the rest of the simulated parameters. An example of a lookup table as generated by the simulator for V_{ds} =0.6 V.

V_{DS}	V_{GS}	I_{DS}	C_{GS}	C_{GD}	Q_S	Q_D
…	…	…	…	…	…	….
…	…	…	…	…	…	…
…	…	…	…	…	…	…

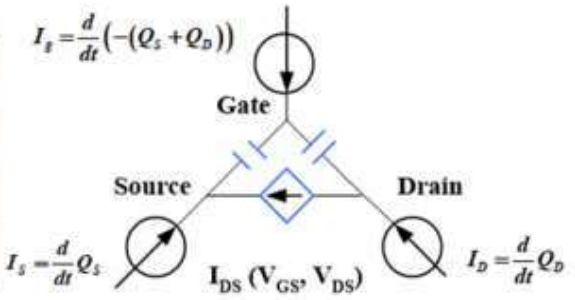

Figure 1.21 Verilog-A model schematic.

We assume similar driving currents for the n-channel and p-channel transistors in TFET Verilog-based simulations due to continuing efforts in p-type Tunnel FET research. A set of models for determining the best circuit performance. It should be noticed that the Density-of-States (DoS) of electrons and holes can be quite different in Si material and

the gate-capacitance characteristics are obtained from the Sentaurus 2-D simulation for n-type and p-type TFET, respectively, to accurately model the circuit performance.

1.1.7 Biosensors Based on FETs

In this rapidly evolving technological world, biosensors are becoming increasingly important in human existence, and the frequent usage of biosensors creates academics' interest in defining various techniques to detect biomolecules. In recent times FET based biosensors have gained a lot of attention among worldwide researchers due to their superior properties like label-free detection, small size, rapid response, and reliability [87] possibility of on-chip integration for amplification circuitry and sensor, mass production with low cost, high selectivity and reusability. To detect targeted biomolecules the oxide layer of the FET is employed with the bio receptors/bio-recognition element. Once these receptors captured the targeted biomolecules they have undergone a conjugation process that generates electrochemical reactions and these electrochemical reactions led to the gating effect in the semiconductor device [88], [89]. This gating effect changes the electrical properties of the device and is characterized as the sensitivity parameter for the detection of biomolecules before and after capturing the targeted biomolecules by the receptors. There are many parameters to measure the sensitivity like current ratios (I_{ON}/I_{OFF}), the shift in threshold voltage (V_T), and the variation of ON-state current (I_{ON}). Although FET based biosensors are having a lot of advantages, however, they are facing major issues like,

i. The scaling difficulties and the short channel effects (SECs) experienced by the FET in the process of miniaturization [2], [4], [5] [8].
ii. The theoretical limitation on the minimum achievable subthreshold swing (SS > 60 mv/dec) [2], [4], [5] [8].

These issues led to narrowing the device performance, sensitivity, and thermionic emission of the electron in FET resulting in high power dissipation. To address these issues, researchers are focusing on new technology FET-based biosensors, namely TFET-based biosensors, which have low power and excellent properties due to carrier band to band tunneling and steep subthreshold swing [88].

1.1.7.1 Types of Biosensors

Fundamentally biosensors are classified by considering their detection mechanism and transduction method. The detection mechanism involves the use of biological elements such as enzymes, biological tissues, antibodies, drugs, proteins, microorganisms, etc. [89]. The targeted biomolecules are analyzed by overlaying on the detection element. As a result, they generate some physiochemical reactions which generate some by-products that are treated as inputs for the transducer elements. Depending upon the transduction process different physiochemical reactions caused by the sensing elements are classified into four major types and some subclass as given in Figure 1.22 [90].

1.1.7.2 Structure and Working of the TFET as a Biosensor

In the Conventional FET (CFET) source and drain are doped with similar kinds of doping elements either P-type or N-type but in the case of TFET dissimilar doping is done for both source and drain. The channel region is usually intrinsic or lightly doped in TFET.

The structure resembles a p-i-n diode with a gate as shown in Figure 1.23 [21]-[24]. The barrier width of TFET is made thin to allow the tunneling of the charge carriers where mostly tunneling of the charge carrier occurs at the source-channel junction because the source region is highly doped than the drain region [22]. The performance of a TFET-based biosensor depends on how effectively the gate controls the intrinsic

channel. The electrolytic gate sensor doesn't give better control over the channel because of noise [91] and variability [92] issues. To overcome the above issue, in 2015 A. Gao *et al*. come up with new device architecture which is CMOS compatible silicon nanowire-based TFET (SiNW-TFET) biosensor [93] by using a "top-down" fabrication approach with a low-cost anisotropic self-etching technique via tetramethylammonium hydroxide (TMAH). They implemented a planar gate structure over the nanowire channel for better control of the electrical conduction. Instead of using a single wire structure, they grouped 10 nanowires into a single cluster and each wire was used to detect biomolecules. From Figure 1.24 (a) it is observed that before capturing the biomolecules the energy states of source and channel are not aligned but Figure 1.24 (b) describes the effective bending of the energy bands giving scope for the tunneling.

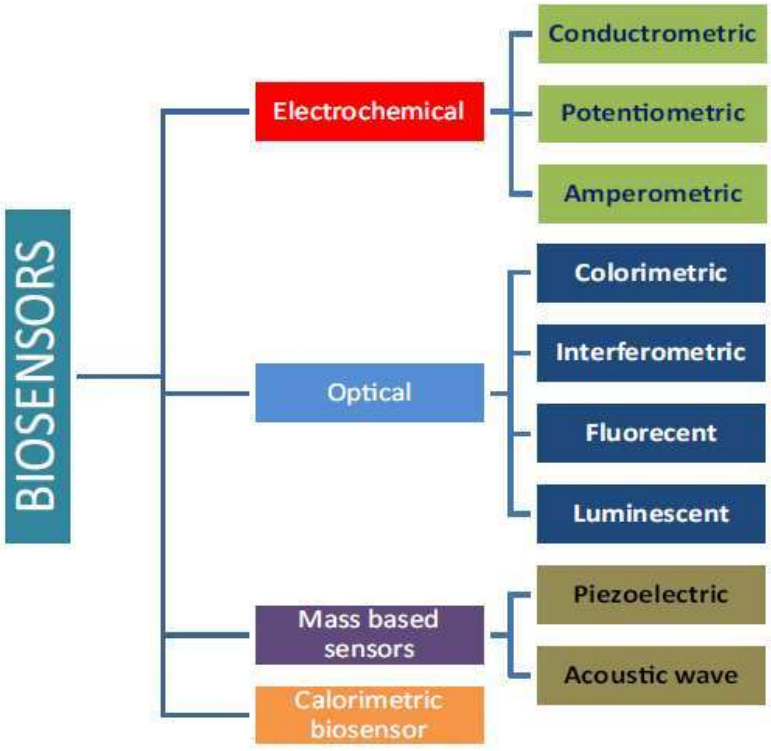

Figure 1.22 Classification of biosensors based on the transducer [90].

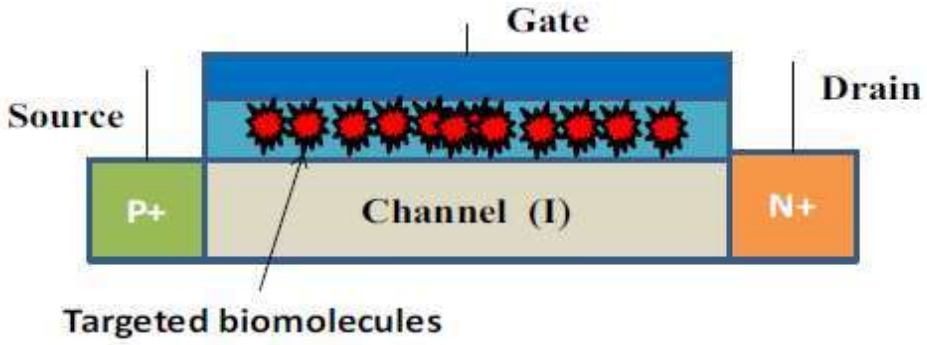

Figure 1.23 2D schematic structure of TFET-based biosensor.

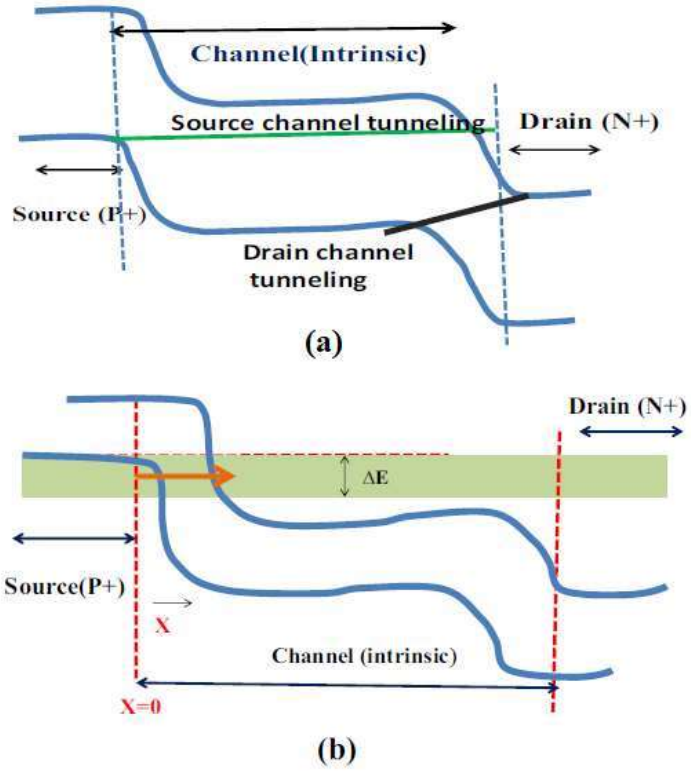

Figure 1.24 (a) Energy band diagram in off state (b) Energy band diagram in on state.

1.1.7.3 Dielectric Modulated TFET Based Biosensor

Dielectric modulated FETs as biosensors have attracted a lot of attention in recent times [94]-[96]. By applying the principle of dielectric modulated FET for biosensing, R.Narang et al. reported the dielectric modulated TFET biosensor in 2013 [97]. The

structure has a cavity region that has been formed in the oxide layer beneath the gate electrode for the targeted biomolecules to inhibit and immobilize the sensing biomolecules. The device encounters a shift in the dielectric constant of the oxide once the biomolecules become stable and because of their dielectric value. Because of the shift in dielectric constant, the effective coupling between the gate and oxide layer changes, causing the channel's energy bands to bend. The bending of the energy bands for the channel results in a decrease/increase in the effective tunneling length, which causes the drain current to drift. A double gate structure is also proposed instead of a single gate configuration for better performance in the TFETs-based biosensors [97]-[99]. In the conventional TFETs, p-i-n structures exhibit low current, therefore authors have considered the p-n-p-n structure for the designing of the dielectric modulated biosensor as shown in Figure 1.25 [98]-[100].

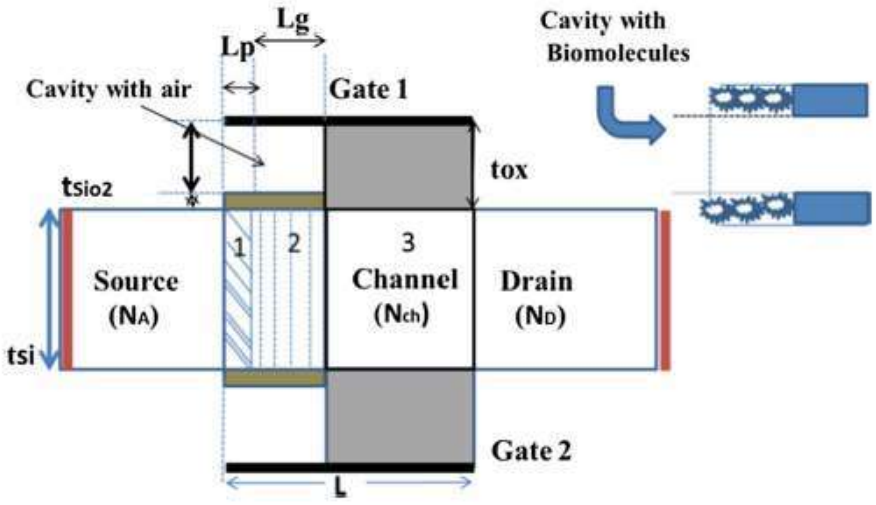

Figure 1.25 Schematic view of the dielectrically modulated TFET [100].

1.1.8 Literature Review of TFETs

TFET or Tunnel Field Effect Transistor in recent times has been the center of attraction in research communities despite having a minute subthreshold slope and excessive I_{ON}/I_{OFF}

ratio. It is known that TFETs are much more immune to short-channel effects and fluctuations of random dopants in comparison to their MOSFET counterparts [22]. In this thesis, a deep-rooted literature review has been done scanning every aspect of TFET including the variations of performance with different parameters. The literature review finally gives a picture of the recent progress of TFET in different aspects such as from subthreshold swing to a significantly lower leakage current and high on current.

The subsections are organized as follows. Subsection 1.6.1 discusses the survey of device-level simulations based on various geometries of TFETs. The emphasis has been placed on discussing geometries that are distinct from one another. Subsection 1.6.2 discussed the designing of circuits by using the TFET device. Subsection 1.6.3 provides an overview of the most commonly suggested TFET-based biosensor applications.

1.1.8.1 Device Level Simulations Related Work

This section reports the next phase of development in TFETs after the establishment of fundamental *p-i-n* geometry. Knoch and Appenzeller proposed the tunneling carbon nanotube TFTs in 2004 and discussed the method to reduce the tunneling probability at the tunnel junction [101]. The one-dimensionality of carbon nanotube results in efficient band-to-band tunneling. A minimum *SS* of 15 mV/dec was achieved for low drain bias in the band-to-band tunneling regime.

Boucart and Ionescu proposed the double gate tunnel FET [102] [103] by introducing two gate terminals: one on the front and the other on the back gate, influencing the tunnel junction. The device was reported to offer a boost on current as high as 0.23 mA, and a reduction of OFF-state current to less than 1 fA. Toh *et al*. proposed a DC TFET with Si/Ge source to modulate the tunnel barrier at the tunnel junction, thus resulting in enhanced ON-state-current and subthreshold swing (*SS*) [104]. DC TFET using InAs/Si heterojunction at the source–channel tunnel junction was reported by S. Ashish *et al*. to

reduce the tunnel window and boost the ON-state current [105]. The use of dual/hetero-dielectric in TFETs has been proposed to suppress the leakage currents ambipolar currents in TFETs. The ambipolar current in n-TFETs arises out of the band-to-band tunneling at the channel drain junction which is undesirable. Vadizadesh and Fathipour proposed the use of a low-k dielectric on the drain side of a DG TFET to reduce the leakage current [106]. Choi *et al*. proposed the concept of hetero-gate dielectric TFET for reduced ambipolarity current and higher ON-state current than conventional ones [107]. Verhulst *et al*. reported the significant effects of a gate-drain underlap in a conventional TFET. The increase in gate-drain proximity in a TFET reduces the influence of the gate on the drain junction while maintaining the electric field at the tunnel junction. Since a shorter gate length results in a lesser gate capacitance, hence, the switching speed of the device increases [108]. Similarly, J. Wan *et al*. introduced a gate-drain underlap towards the non-tunnel junction to reduce the ambipolarity current [109]. Narang *et al*. presented a stacked gate dielectric DG TFET in order to achieve better characteristics than low-k dielectric DG TFET. Use of high-k results in high leakage currents. A stacked dielectric helps to achieve characteristics better than using only low-k or high-k characteristics. Using a stacked gate dielectric structure, the authors reported an increase in ON-state current than low-k dielectric TFET by more than 10 times [110]. Saurabh and Kumar proposed a dual material gate DG TFET where a tunneling gate near the source-drain junction is used to achieve high electric fields through a low work function, and an auxiliary gate with a high work function near the channel drain junction is used to reduce the ambipolar current [111]. Bagga and Sarkar increased the number of materials on the gate and presented a triple material DG TFET in order to prevent the reverse tunneling of carriers from drain to source [112]. The use of different work functions of gate along the position of the device from source to drain forms a barrier in the channel, which helps to

reduce the off current. The metalwork functions are selected in such a way that the work functions of the metal closer to the source/drain junctions are kept smaller than the one sandwiched between the two. The ON-OFF current ratio of~ 10^7 is achieved for a body thickness of 7 nm. A similar concept has been presented in the work of Nigam *et al*. in an asymmetric source-drain doping TFET where authors have named the three gate materials a tunneling electrode, a control electrode, and an auxiliary electrode [113]. The work functions of the two materials are always kept equal to maintain the dual value of work function throughout the device. The optimized device is reported to exhibit an on-off current ratio greater than 10^{11}. Z. Yu *et al*. demonstrated an asymmetric gate dielectric DG TFET with a source pocket [114]. The concept of a source pocket is similar to a raised source on intrinsic silicon. The configuration of gate dielectric on the front and back gates are asymmetric. While the front gate consists of a dual (high-k/low-k), and the back gate consists of a low-k dielectric throughout the device terminating the drain edge. The dual dielectric on the front gate assists in achieving low ambipolar current and high electric fields at the tunnel junction, while the low-k dielectric on the back gate facilitates tunneling between the source and the body through the back gate. Tyagi *et al*. proposed a wedge-shaped structure of a high-k dielectric DG TFET to increase the tunneling area and enhance the ON-state current of the transistor by~3 times than a conventional planner DG TFET [115]. Tilted Wedge TFET or W-TFET, can achieve an ON-OFF current ratio greater than 10^{11} at a supply voltage of 1 V. The reported subthreshold swing is in the range of 45 – 50 mV/dec. Graphene nanowire (GNR) TFETs have gained interest due to high carrier mobilities and a tunable energy bandgap that depends on the nanoribbon width. Lam *et all*. Proposed various designs of nanoribbon graphene TFET and reported an extensive study on the same [116]. The authors presented bandgap-engineered solutions for GNR TFETs and showed that significant improvement in GNR TFETs may

be obtained through several of the nanoribbon widths along the channel. An I_{ON}/I_{OFF} of four orders of magnitude has been achieved with an I_{ON} of 1.5 mA/μm. Rawat and Paily proposed a GNR TFET and optimized its saturation current by introducing a modified doped channel and drain underlap [117].

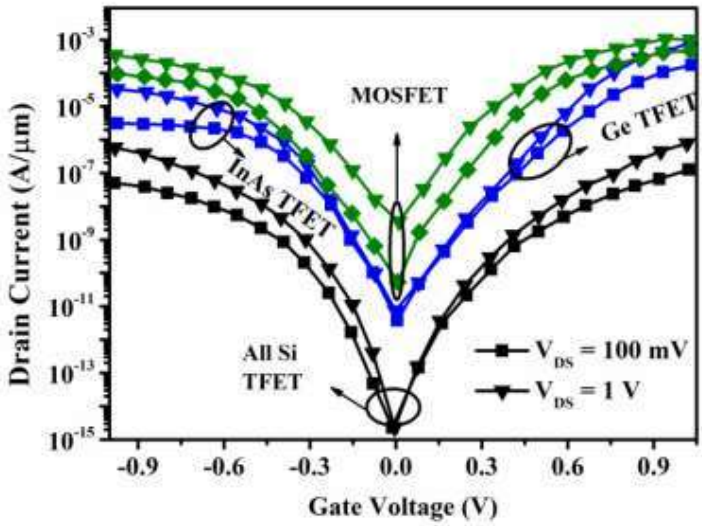

Figure 1.26: Comparison of 65 nm state-of-art CMOS technology TFETs with MOSFETs, taken from [121].

Researchers have used SiGe-based TFETs due to their mole-fraction-dependent bandgap which offers flexibility to device designs. Zhao *et al*. reported experimental and simulation studies of a-Si TFET with a buried $Si_{1-x}Ge_x$ source [118]. A gate-source overlap is used to increase the tunneling area. The presence of heterojunction further increases the tunneling probability. They reported an experimentally obtained SS of 80 mV/dec. Schmitdt *et al*. proposed a fabricated a-Si/SiGe TFET and analyzed the effect of scaling on TFET [119]. The authors reported that the ON-state current is proportional to the gate the gate-source overlap area. The U-shaped channel TFETs with SiGe source regions were proposed by Wang *et al*. [120]. The use of a U-shaped channel structure increases the tunneling area and the introduction of an n^+ layer near the source-channel

junction helps to achieve high on-current. A comparison of TFETs with MOSFETs belonging to the 65 nm state-of-the-art CMOS technology is shown in Figure 1.21 taken from [121]. Saurabh Mookergea *et all*. Temperature-dependent characteristics of vertical $In_{0.53}Ga_{0.47}As$ tunnel field-effect transistors (TFETs) at low drain bias were reported to provide important insight into device operation and design. [122]. The temperature dependence of subthreshold slope, according to the authors, results from tunneling into the conduction band after transitioning into mid-gap states at the oxide–semiconductor interface. They also stated that pure band-to-band tunneling dominates at intermediate gate voltages, whereas current transport is diffusion-limited at higher gate voltages. They have concluded that the temperature-dependent study of $In_{0.53}Ga_{0.47}As$ TFETs emphasizes the importance of passivating the III–V and dielectric interfaces. [122]. B. Das *et al*. [123] presented a numerical simulation study for the ferroelectric gate oxide tunnel field-effect transistor (Ferro-TFET). The device's performance is examined using Landau's theory, as well as its behavior in the temperature range of 200-300 K. The authors demonstrated that for the simulated device, a minimum subthreshold swing and maximum transconductance are obtained around the Curie temperature (T_C) of 58 ± 10 K. In this study, the Ferro-TFET outperforms conventional TFETs and MOSFETs in terms of reducing the negative effects of mobility degradation at high gate voltage and performance degradation at high temperatures. As a result, the operation of the Ferro-TFET at Curie temperature yields remarkable results for analog and RF applications. The temperature influence on AlGaAs/Si-based heterostructure junctionless double-gate tunnel field-effect transistors was examined in this study [124]. The increased subthreshold slope and static leakage current indicate that it will be useful in the development of future low-power switching circuits. The suggested device structure's OFF-state leakage current is essentially temperature independent, according to the 2-D computer-based simulation results. The

effect of temperature on off-state current components is investigated numerically and experimentally in this work, which is proposed by P. G. D. Agopian *et al*. [125]. They claim that higher values of underlap (reduced BTBT) and low temperatures resulted in the best off-state current behavior (reduced SRH and TAT). They conclude that these devices performed well in terms of drain current as a function of drain voltage, making them suitable for analog applications. The authors presented a comprehensive comparison study of *p-i-n* and *p-n-p-n* tunnel field-effect transistor (TFET) architectures, as well as the effect of temperature on their dc and circuit performance [126]. The device performance of *p-i-n* and *p-n-p-n* TFETs with high-*k* and HG dielectrics, as well as the effect of temperature on the drain current characteristics, I_{ON}/I_{OFF}, and threshold voltage, has been investigated and compared with MOSFETs. Furthermore, the variations in the transient characteristics of the inverter (n-TFET with resistive load) and the fall delay due to temperature variations are investigated using mixed-mode simulations performed with ATLAS device simulation software. The results show that when current conduction is dominated by band-to-band tunneling, TFET exhibits weak temperature dependence, whereas temperature dependence increases in the off-state regime, and the fall delay of a resistive load n-TFET inverter decreases with increasing temperature. R Narang *et al*. presented the effects of temperature and fixed oxide charge variability on gate, and source/channel SOI TFETs [127]. The authors claim that the response of the proposed device to changes in buried oxide thickness, back gate voltage, and the drain voltage is related to temperature variability and that a positive oxide charge degrades on current while improving ambipolarity, whereas a negative oxide charge improves on current while degrading ambipolarity. P. Venkatesh *et al.* studied the effect of positive (donor) and negative (acceptor) interface trap charges on the performance of a proposed heterogeneous gate dielectric (HD) electrically doped tunnel field-effect transistor

(EDTFET) in terms of dc, analog/RF, and linearity distortion parameters, where the HD layer is used as a gate dielectric to improve the ON-state current and device performance [128]. N. Kumar *et al.* presented a charge-plasma (CP)-based gate-all-around (GAA) silicon vertical nanowire tunnel field-effect transistor (NWTFET) [129]. Here authors took linearity performance parameters such as higher-order harmonic distortions (HDs), intermodulation distortions (IMDs), and interception points are calculated including the effects of ITCs on the cylindrical channel-surround gate-oxide interface. By inserting localized charges (donor/acceptor) at the semiconductor/insulator interface, K. S. Singh et al. studied the influence of varied interface trap charges (ITCs) on dual-material gate-oxide-stack double-gate TFET (DMGOSDG-TFET) [130]. In order to do so, the authors looked at the impacts of different ITCs on DC, analog/RF, and linearity performance metrics in both conventional dual-material control gate tunnel field-effect transistors (DMCG-TFET) and dual-material gate-oxide stacked double-gate TFETs with equal dimensions. In 2021. The effects of back-gate bias on the subthreshold swing (*SS*) of a tunnel field-effect transistor (TFET) were discussed by Jaehong Lee et al. (2019) [131]. The back-gated TFET's electrostatic properties were derived using technology computer-aided design (TCAD) simulation and described using turn-on and inversion voltage principles. As a result, as the back-gate voltage increased, SS decreased; this behaviour is attributed to the greater inversion voltage that resulted. Furthermore, it was discovered that the TFET's ON-OFF current ratio increased when S decreased due to the back-gate voltage.

1.1.8.2 Previous Works Using TFETs in Circuit Design

Circuit-level metrics were analyzed for TFET by Kam *et al.* (2008) [132] where TFET technology appeared to be compelling for sub 100MHz applications. They have found that for applications below 500 MHz, TFETs are more energy-efficient than conventional

MOSFETs. Yasin Khatami *et al.* (2009) [133] designed The T-FETs to exhibit input and output characteristics compatible with CMOS-type digital-circuit applications. They introduced new n- and p-type tunnel field-effect transistors (T-FETs) based on a heterostructure Si/intrinsic-SiGe channel layer that had very small subthreshold swings and low threshold voltages. When compared to previously reported T-FET devices, the designs have extremely low off currents on the order of 1 fA/mum and are developed to have far greater on-state currents. Inter-band tunnel field-effect transistors (TFETs) invented by D. K. Mohata et al. (2010) [134] have piqued interest due to their capacity to overcome the 60mV/dec sub-threshold slope (STS) constraint in MOSFETs. Koswatta et al. [135] at Purdue University made extensive studies on the performance comparison between TFETs and conventional MOSFETs where carbon nanotube was used as the basic material for device fabrication. They observed that TFETs had smaller switching energy than conventional MOSFETs despite having lower ON-current in the former structure. Thus, TFETs can be used for faster switching applications over MOSFETs. Miller capacitance effects were analyzed for TFET-based circuits by Kim et al. [135] and Power consumption was shown to be very less for TFETs than MOSFETs. They have compared the TFET-based ring oscillator with the CMOS ring oscillator by the use of a lookup table (LUT) based model. The same value of the oscillation frequency was obtained at lower supply voltage in TFETs as compared to CMOS technology. They have also reported an SRAM cell based on heterojunction TFETs which showed leakage current reduction in comparison with conventional CMOS devices. Mixed-mode device and circuit simulation were analyzed for delay estimation of unloaded TFET inverters by Mookerjea *et al.* [137] were the first to observe the enhanced value of C_{gd} in TFETs. They found out that the gate capacitance C_{gg} in TFET is dominated by C_{gd} as compared to *Cgs*. They have observed that the effective load capacitance for TFET-based unloaded

inverters is double the amount of the gate capacitance. The increased parasitic capacitances were attributed to increased delay in TFET circuits. They have explained the procedure to extract effective ON-current and output capacitance for TFET delay calculations. Simulation of TFET for low-power digital applications with a lower supply voltage (<0.5 V) was reported by Zhuge1 *et al.* [138]. In this work, they have found out that a better energy-delay product can be achieved in the heterostructure TFET compared to MOSFET.

1.1.8.3 Previous Work on TFET-Based Biosensors

Dielectric modulated FETs as biosensors have attracted a lot of attention in recent times [139] - [141]. The TFETs have been considered for such biosensing applications because of their property of ambipolar conduction [142] and active tunneling [143]-[148]. The geometry of dielectric modulated sensors consists of an embedded nanogap to receive the biomolecules. The dielectric thickness of these biosensors is kept higher than conventional high-k dielectric TFETs in order to accommodate the biomolecules in the nanogap. The geometries are simulated on industrial simulators considering an equivalent insulator with an equivalent dielectric constant. Several geometries have been verified to demonstrate the excellent sensitivities of biomolecules, for neutral and charged immobilization.

Driwedi P. *et al*. (2020) proposed a work based on the impact of back-gate voltage on the sensing metric of dielectric modulated TFET biosensor [149]. The authors of this study looked at transfer characteristics, energy band variation, and hole concentration as a function of back-gate voltage, and computed the drain current sensitivity and selectivity for three distinct back-gate voltage values. They found that increasing the positive back gate voltage improves drain current sensitivity by about one order of magnitude and increases selectivity by more than two times. The role of a hetero-junction p-i-n gate all

around tunnel FET design for biosensing applications is investigated by Ajay et al. (2019) [150]. The device has been modeled in terms of several characteristics such as surface potential, threshold voltage, and drain current, and it has a higher sensitivity. In this paper, V. D. Wangkheirakpam et al. (2020) [151] reported a complete comparison of sensitivity between double gate tunnel FET and n+ pocket doped vertical tunnel FET based label-free biosensors. Both biosensors have nanogaps on the left and right sides of the fixed dielectric (HfO2), which increases the biosensors' capture area. TCAD modeling studies of their sensitivities have been compared using neutral/charged biomolecules with varying dielectric constants. Due to its current conduction in both vertical and lateral directions, the sensitivity of VB is determined to be approximately 10^4 times that of DB. The impacts of steric hindrance and uneven probe/receptor position are also investigated in order to comprehend the sensors' non-ideal performance. A new charge plasma-based junctionless silicon dual cavity nanotube tunnel field-effect transistor (DC-NT-TFET) based biosensor for the detection of neutral and charged biomolecules was introduced by Gedam *et al*. (2021) [152]. The nanogap cavity is placed in both the inner and outer portions of the NT-TFET for increased sensing ability. The device's vertical position also helps to ensure that biomolecules are distributed evenly across the cavity. The sensitivity of the suggested biosensor for four dielectric constant neutral biomolecules, streptavidin (k =0.1), biotin (k = 2.63), 3-aminopropyl-triethoxysilane (APTES) (k = 3.57), and protein *(*k = 8, is investigated in this work. Deoxyribonucleic acid (DNA), a charged biomolecule with a particular dielectric constant of k = 6, is also investigated for varying positive and negative charge densities.

1.2 Scope of the Thesis

Tunnel field-effect transistors (TFETs) have long been regarded as a viable alternative to MOSFETs if the concerns surrounding their feasibility can be addressed correctly. Short

channel effects and non-scalability of *SS* in MOSFETs make them unsuitable for low-power applications. According to the International Technology Roadmap for Semiconductors 2013, TFETs will continue in research until the early 2020s before being commercialized and employed in applications. (Figure 1.14) [63].

In this thesis work till chapter 5, we have done Atlas Silvaco TCAD Simulation-based extensive analysis of some TFETs structures on SELBOX substrate. All chapters contain simulation based extensive electrostatic analysis such as DC, RF/analog, and linearity parameters. In chapter 6, we have focused on application of these device for label free biosenseing.

1.2.1 Organization and Outline of the Thesis

This thesis has been organized into eight chapters based on the sequence of the relevance. The first chapter introduces and discusses the fundamental theories and basis for taking up the work. The next five chapters take up different problems and objectives and deliver potential solutions and insights into them. The final chapter concludes the thesis by mentioning the future scope of the research work.

Chapter 1: Introduction and Scope of the Thesis

This chapter introduces the thesis by briefly presenting the drawbacks of the MOSFET including the effects of scaling, and the emergence of novel semiconductor devices. It comments on the working principle of TFETs and their suitability for low-power electronics applications. The scope of the thesis is also briefly presented in this chapter.

Chapter 2: Design and Performance Assessment of HfO_2/SiO_2 Gate Stacked Ge/Si Heterojunction TFET on SELBOX Substrate (GSHJ-STFET)

This chapter proposes an electrostatic comparison between conventional fully depleted SOI TFET and proposed HfO_2/SiO_2 Gate Stacked Ge/Si Heterojunction TFET on SELBOX Substrate (GSHJ-STFET). This chapter discusses the advantages of the

proposed TFET structure over the conventional fully depleted SOI TFET structure. Furthermore, we investigated the effect of temperature on the performance of the proposed TFET (GSHJ-STFET) structure.

Chapter 3: Effects of Interface Trap Charges and SiO_2/HfO_2 Gate-Oxide Stacking on the DC/RF performance parameters of Ge/Si heterojunction TFET on SELBOX Substrate

In this chapter, we have investigated the influence of both the donor and acceptor type interface trap charges (ITCs) on the reliability of lateral SiO_2/HfO_2 gate stacked STFET (LS-STFET) and vertical SiO_2/HfO_2 gate stacked STFET (VS-STFET) in terms of their DC, analog/RF, and linearity parameters. This is a comparative analysis work based on their DC/RF and linearity parameters.

Chapter 4: Performance Investigation of Back-Gated Ge/Si Heterojunction TFET on SELBOX Substrate with a SiO_2/HfO_2 Oxide Stacked Gate-Oxide Structure

This chapter reports the design and device-level simulation analysis of a back-gated Ge/Si heterojunction TFET on SELBOX substrate (BG-HJ-STFET). The proposed structure implements a stacked gate oxide where the conventional SiO_2 is replaced by a SiO_2/HfO_2 in a stacked manner to increase its On-current. A back gate (BG) is also considered in the proposed TFET to enhance the device-level performance. Investigation of DC, RF, and linearity parameters such as drain current, transconductance, electric field, parasitic capacitance, cut-off frequency (f_T), gain-bandwidth product (GBP), intrinsic delay (τ), higher-order of g_m (gm_2, gm_3), VIP2, VIP3, IIP3, IMD3, and 1-dB compression point are carried out for the proposed TFET and the results are compared with other conventional structures. Performance evaluation shows that BG-HJ-STFET is a suitable candidate for distortionless and high-frequency applications. Further, A CMOS inverter has been designed by using the proposed TFET for the investigation of digital circuit-level performance.

Chapter 5: Performance Investigation of Back-Gated Ge/Si Heterojunction STFETs with a SiO_2/Ferroelectric Oxide Stacked Gate-Oxide Structure

This chapter reports the device-level performance of a back gated ferroelectric heterojunction TFET on SELBOX substrate (BG-Fe-HJ-STFET). The proposed structure implements a stacked gate oxide where the conventional SiO_2 is replaced by a SiO_2/ferroelectric oxide in a stacked manner to increase its on-current. The incorporation of ferroelectric materials into the gate dielectric in BG-HJ-STFET may help in gate voltage amplification, which improves the performance of the proposed TFET (BG-Fe-HJ-STFET). Investigation of DC, RF, and linearity parameters such as drain current, transconductance, electric field, parasitic capacitance, cut-off frequency (f_T), gain-bandwidth product (GBP), intrinsic delay (ć), higher-order of g_m (gm_2, gm_3), VIP2, VIP3, IIP3, IMD3, and 1-dB compression point is carried out for the proposed TFET and the results are compared with back-gated Ge/Si heterojunction STFETs with a SiO_2/HfO_2 oxide stacked gate-oxide structure.

Chapter 6: Designing of SiO_2/Ferroelectric Oxide Stacked Ge/Si Heterojunction STFETs Based Label-Free Bio Sensor: A Possible Application of BG-Fe-HJ-STFET

A SiO_2/Ferroelectric oxide stacked back-gated Ge/Si heterojunction TFET on SELBOX substrate (BG-Fe-HJ-STFET) based dielectric modulated label-free biosensor has been designed in this chapter. The SELBOX substrate has been used in the proposed TFET-based biosensor to improve the I_{ON}/I_{OFF} sensitivity. Four cavities have been created in the ferroelectric gate-oxide of the studied TFET, and they contain the biomolecules to be sensed using the gate-dielectric modulation principle. The I_{ON}/I_{OFF} sensitivity, subthreshold swing sensitivity and threshold voltage sensitivity parameters of the proposed BG-Fe-HJ-STFET structure have been thoroughly investigated considering different biomolecules. The proposed BG-Fe-HJ-STFET structure outperforms some

recently reported TFET-based biosensors in terms of I_{ON}/I_{OFF} sensitivity, subthreshold swing sensitivity and threshold voltage sensitivity.

Chapter 7: GaSb/GaAs Type-II Heterojunction TFET on SELBOX Substrate for Dielectric Modulated Label-Free Biosensing Application

Ge/Si heterojunction has been used up until chapter 6, and in that chapter, we optimised a device that can be used for low power electronics applications. To further improve the device performance, we changed the heterojunction material in this chapter. So, in this chapter, we have designed a SiO_2/HfO_2 oxide stacked back-gated GaSb/GaAs type-II heterojunction TFET on SELBOX substrate based dielectric modulated label-free biosensor. Duel cavities in the HfO_2 of the studied TFET are created. These cavities contain the biomolecules to be sensed through the principle of gate-dielectric modulation. The proposed dual cavity heterojunction TFET on SELBOX substrate (DC-HJ-STFET) structure is shown to have the higher current sensitivity ($\sim 6.67 \times 10^{11}$) and threshold voltage sensitivity (0.38V) values over some recently reported TFET based biosensors.

Chapter 8: Conclusion and Future Prospects

This chapter concludes the thesis with comments on possible works that could result from the study in this thesis. The major difficulties associated with the proposed TFETs and their viability is commented upon including simulation and circuit analysis.