Chapter 7

Hybrid L-Z Source Inverter: CCM, NZ-DCM and DCM

7.1 Introduction

To increase the gain of Z source inverter, switched inductor cells are incorporated in ZSI [75]. Switched inductor cell consists of arrangement of diodes and inductors such that inductors are parallel connected during charging period while during discharging period, inductors are in series. The gain of the ZSI is increased by adding suitable number of switched inductor cells. Similarly, these cells may be integrated in qZSI to increase the voltage gain. However, for stable operation of ZSI and qZSI, capacitance C_1 and C_2 must be equal. Practically, it is quite difficult to keep these constant due to uneven degradation of capacitors. This limitation is sorted by using switched boost inverters(SBIs) [66,69,134] and L-Z source inverter(LZSI) [135]. Switched boost inverter consists a diode, a capacitor and an inductor [70]. On the other hand, instead using the capacitor at boosting stage, LZSI incorporates a combination of diodes and inductors. Therefore, the problem due to the presence of two capacitors is eliminated. However, in LZSI, the switched inductors arrangement directly comes in series with the load through the switching of the inverter. The switching of the inductor between source and load generates huge spikes which may damage the devices. To protect the inverter switches, a snubber circuit having small capacitance and huge value of resistor is connected across the inverter.

Based on LZSI, a hybrid LZSI(HLZSI) is recently reported [136] which is based on the idea by Ray et al [131] in the form of boost derived hybrid converter. HLZSI can

power both AC and DC load simultaneously. However, it fails to operate when inductor current saturates at the level of load current or become constant in during discharging. This mode is termed as non zero discontinuous current mode(NZ-DCM) in this paper. To restore the operation of HLZSI in continuous current mode(CCM), HLZSI is extended to modified hybrid LZSI(MHLZSI). The transition from HLZSI to MHLZSI is dependent on the operating condition of the converter. Although by taking into account the effect of average inductor current, and load power, the boundary condition was derived [136]. However, the transition from HLZSI to MHLZSI is also dependent on the peak to peak ripple current which was not considered earlier. Firstly, this chapter analyzes the effect of peak to peak ripple current on boundary condition along with its impact on converter performance. Secondly, to harness the maximum gain from the converter, MHLZSI is operated under DCM. The property of achieving high gain in DCM for DC to AC converter is presented. Both the modes are derived analytically and validated experimentally. The contributions of this chapter are: 1) To derive the boundary condition in terms of peak to peak inductor ripple current, average inductor current and peak AC current. 2)Discuss the impact of peak to peak ripple current on converter performance. 3)Operation of MHLZSI under DCM to achieve high gain.

7.2 Circuit diagram and operation

7.2.1 Circuit diagram

The circuit diagram for MHLZSI having single switched inductor cell is shown in Fig-7.1 which feed power to DC and AC load. The DC load is powered by the capacitor present at the DC link while AC load is supplied by the three phase inverter. The number of cells depends on the required gain. The switch S present in the converter avoids the NZ-DCM and pushes the converter into CCM and DCM as the case may be.

7.2.2 Operation

For operational analysis, the AC load is assumed as constant current source. The MHLZSI broadly consists of three states with respect to inverter operation. These states are classified as shoot through state, active state and zero state. The individual states for

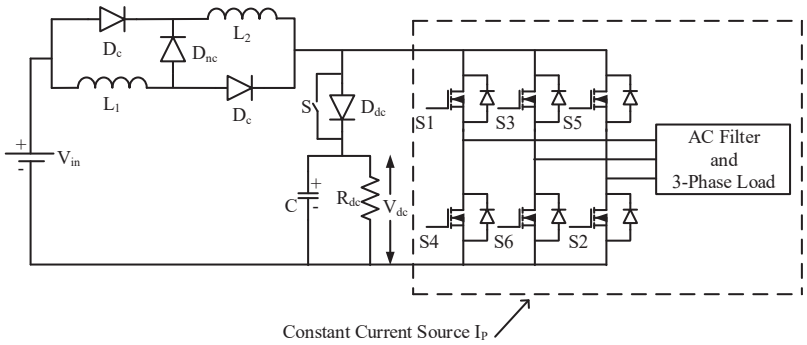


Figure 7.1: Circuit diagram of MHLZSI

MHLZSI are explained as follows

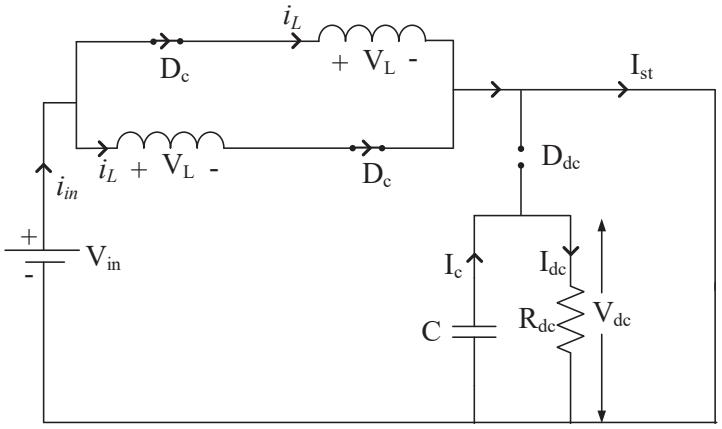


Figure 7.2: Shoot through state for MHLZSI

Shoot through state

To bring this state into the inverter for MHLZSI, the switches of the same leg are short circuited(e.g. S_1 and S_4), as shown in Fig-7.2. Source voltage is directly applied across the diode(D_c), which forward biases D_c. During this period, the inductor current slope is positive hence V_L is positive, due to which D_{nc} and D_{dc} are reversed biased. In this mode, I_P is zero, and all the current passes through the switches. The current I_{st} is equal to sum of inductor charging currents. The period for this state is defined as dT_s. where d is the duty cycle and T_s is the switching frequency.

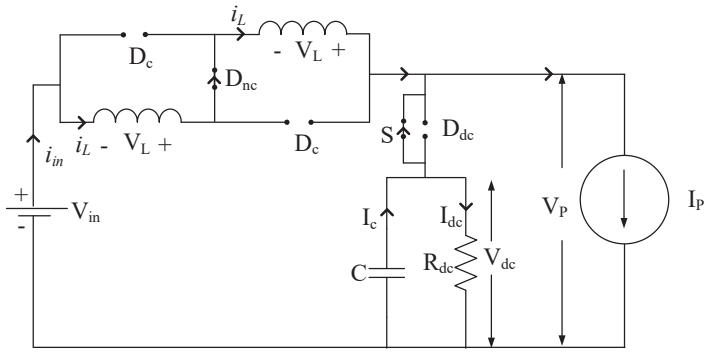


Figure 7.3: Active state for MHLZSI

Active state

During active state of the inverter, the AC and DC load is connected to the source through inverter and diode D_{dc}. The inductor starts discharging which causes the inductor current slope to be negative. So V_L changes its polarity which reverse biases D_c while forward biases D_{nc} and D_{dc} as shown in Fig-7.3. The current I_P and I_{dc} are drawn by AC and DC load, respectively. But as soon as inductor current equals the AC load current, the D_{dc} gets reverse biased. So capacitor is disconnected from the inverter DC link creating NZ-DCM. To push the converter into CCM or DCM, switch S is turned on which reconnect the capacitor at the DC link. The duration of this period is equal to the part of $(1-d)T_s$.

Zero state

Zero state for MHLZSI is shown in Fig-7.4. During this state, either upper half or lower half of the inverter is turned on(e.g. S_1, S_3 and S_5). The inductor current continues to decrease with a negative slope. So, diode D_c remains reverse biased while D_{nc} and D_{dc} are forward biased. The AC load is disconnected, and only DC load is supplied by the source.

7.3 Improved analysis of HLZSI/MHLZSI

In order to improve the analysis reported earlier, the peak to peak ripple current is included.

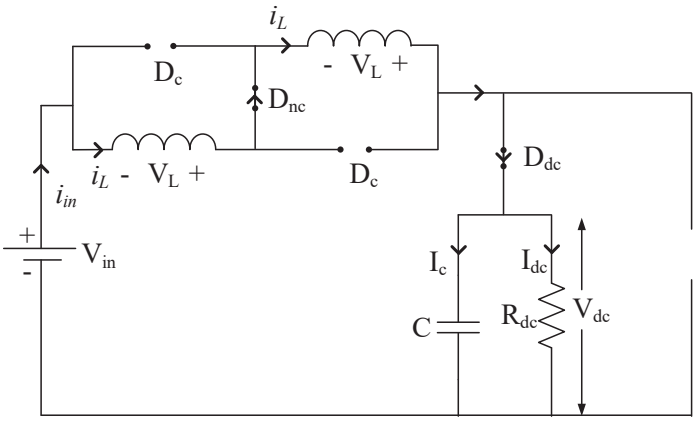


Figure 7.4: Zero state for MHLZSI

7.3.1 Steady state analysis

For steady state analysis, the inductor current and voltage across inductor is shown in Fig-7.5. During charging of the inductor, the voltage across the inductor is given as

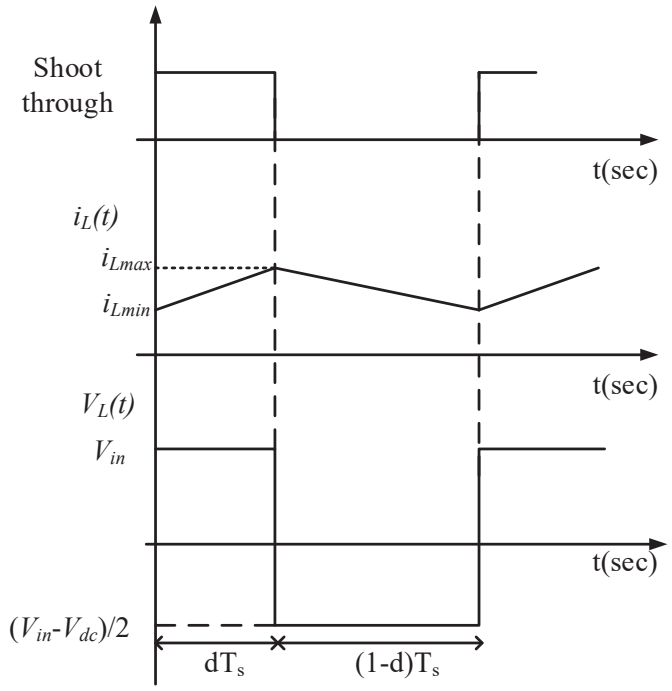


Figure 7.5: Steady state waveform in CCM

$$V_L = V_{in} = L\frac{\Delta I_L}{T_1} \tag{7.1}$$

During discharging

$$V_L = \frac{V_{in} - V_{dc}}{2} = -L\frac{\Delta I_L}{T_2} \tag{7.2}$$

As average voltage over a switching period across inductor is zero, hence from Equ-(7.1) and Equ-(7.2)

$$V_{in}dT_s + \frac{(V_{in} - V_{dc})}{2}T_s = 0 \tag{7.3}$$

this results in output DC voltage equal to

$$V_{dc} = \frac{1+d}{1-d}V_{in} \tag{7.4}$$

For three phase system, the rms AC voltage is written as V_{ac}=$mV_{dc}/2\sqrt{2}$. Hence

$$V_{ac} = \frac{m}{2\sqrt{2}}\frac{1+d}{1-d}V_{in} \tag{7.5}$$

For inductor current ripple(ΔI_L), from Equ-(7.1) and Equ-(7.2)

$$T_s = T_1 + T_2 = L\Delta I_L\frac{V_{dc} + V_{in}}{(V_{dc} - V_{in})L} \tag{7.6}$$

or

$$\Delta I_L = \frac{V_{in}(V_{dc} - V_{in})}{(V_{dc} + V_{in})f_s L} \tag{7.7}$$

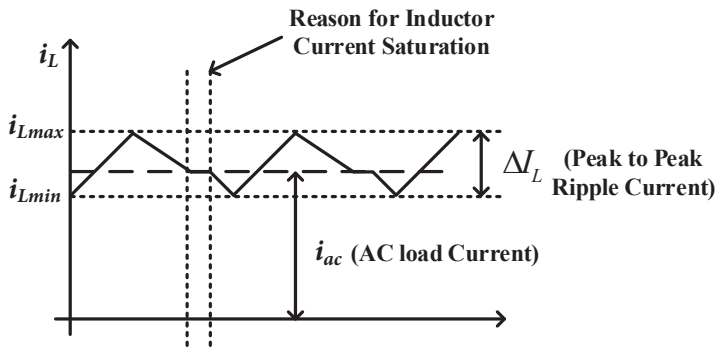


Figure 7.6: Saturation in inductor current

7.3.2 Boundary condition for NZ-DCM

During shoot through period, the input current is written as

$$i_{in} = 2i_L \tag{7.8}$$

For non-shoot through period, input current is

$$i_{in} = i_L \tag{7.9}$$

By taking the average over a switching period, average input current in terms of average inductor current is written as

$$I_{in} = 2I_L d + I_L (1-d) = (1+d) I_L \tag{7.10}$$

From the power balance theory, the total input power is equal to total output power. So

$$V_{in} I_{in} = V_{dc} I_{dc} + 3 V_{ac} I_{ac} \cos \Phi \tag{7.11}$$

From Equ-(7.10) and Equ-(7.11),

$$I_L = \frac{V_{dc} I_{dc} + 3 V_{ac} I_{ac} \cos \Phi}{(1+d)\, V_{in}} \tag{7.12}$$

If the switch S remains off, inductor current(i_L) tries to saturate at the level of load current(i_{ac}), as shown in Fig-7.6. So defining the boundary condition as $i_L - i_{ac} > 0$ [136] is less accurate. This condition suggests that when average inductor current tries to saturate at AC load current, NZ-DCM is noticed. But this is not the case rather as soon as the minimum value of inductor current reaches the level of AC load current, NZ-DCM appears. So, modified boundary condition is defined as

$$i_{Lmin} - i_{ac} > 0 \tag{7.13}$$

where i_{Lmin} is minimum value of inductor current and defined as $i_{Lmin} = I_L - \frac{\Delta I_L}{2}$. Hence, Equ-(7.13) is modified to

$$I_L - \frac{\Delta I_L}{2} - i_{ac} > 0 \tag{7.14}$$

From Equ-(7.7), Equ-(7.12), Equ-(7.14) and replacing i_{ac} by $\sqrt{2} I_{ac}$, boundary condition is written as

$$\frac{V_{dc} I_{dc} + 3 V_{ac} I_{ac} \cos \phi}{(1+d) V_{in}} - \frac{V_{in}(V_{dc} + V_{in})}{2(V_{dc} + V_{in}) f_s L} - \sqrt{2} I_{ac} > 0 \tag{7.15}$$

where I_{ac} is rms value of AC current.

By replacing the value of V_{dc} and V_{ac} from Equ-(7.4) and (7.5), Equ-(7.15) becomes

$$I_{dc} = k_L > \sqrt{2}(1-d) I_{ac} - \frac{3m}{2\sqrt{2}} I_{ac} \cos \phi + \frac{d(1-d) V_{in}}{f_s L} = k_R \tag{7.16}$$

This equation suggests that as the inductor ripple current is changed, boundary condition gets changed. For high value of inductance, the ripple current is small hence as per Equ-(7.39), the saturation occurs for smaller duration and vice-versa.

7.3.3 Capacitor voltage during NZ-DCM

During NZ-DCM operation, as shown in Fig-7.7, the inductor current saturates at AC load current(i_{ac}). Each complete switching period is divided into four parts: T_{st} is shoot through period, T_0 is zero period of inverter, T_1 is active period of inverter and T_2 is saturation period of the inductor current. From volt-sec principle across inductor:

$$V_{in}T_{st} = \frac{(V_{dc} - V_{in})}{2}T_0 + \frac{(V_{dc} - V_{in})}{2}T_1 \tag{7.17}$$

where T_s is switching period and given as

$$T_s = T_{st} + T_0 + T_1 + T_2 \tag{7.18}$$

From Equ-(7.17) and (7.18), DC voltage in NZ-DCM is given as:

$$V_{dc} = \left(1 + \frac{2T_{st}}{T_s - T_{st} - T_2}\right) V_{in} \tag{7.19}$$

In case of NZ-DCM, as per Eq-(7.19), the DC voltage is higher than the CCM. For e.g. at T_s= 115 μs, T_{st}= 29 μs and T_2=45 μs, V_{dc} is 170 V while in CCM it is only 116 V for fixed input of 70 V. However, this mode is not recommended as it injects huge THD in AC voltage due to uneven voltage appearing across the inverter input. To lift the voltage further and keeping lower THD, DCM is analyzed and explained.

7.3.4 Generalized principle for achieving high voltage during DCM

In DC-DC converter, it is quite obvious to achieve high gain under DCM. In ZSI type of converter, during CCM the inverter is connected to source through impedance network. However, during DCM, the inverter experience zero voltage across it when inductor current reaches to zero. These two level of voltages disturb the normal operation of the inverter. Therefore, operation of ZSI under DCM is not allowed. However, in certain ZSI, the DCM can be allowed to achieve higher gain than CCM. To allow DCM:

- A diode must be present at input to block the flow of current into the source.
- A capacitor with a series diode must be present across the input.
- An antiparallel switch across diode must be connected.

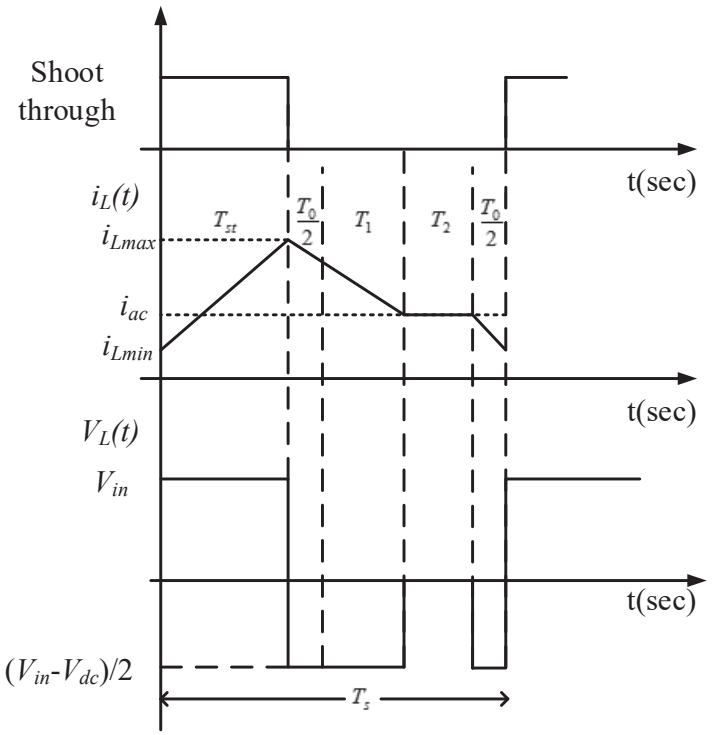


Figure 7.7: Steady state waveform during NZ-DCM

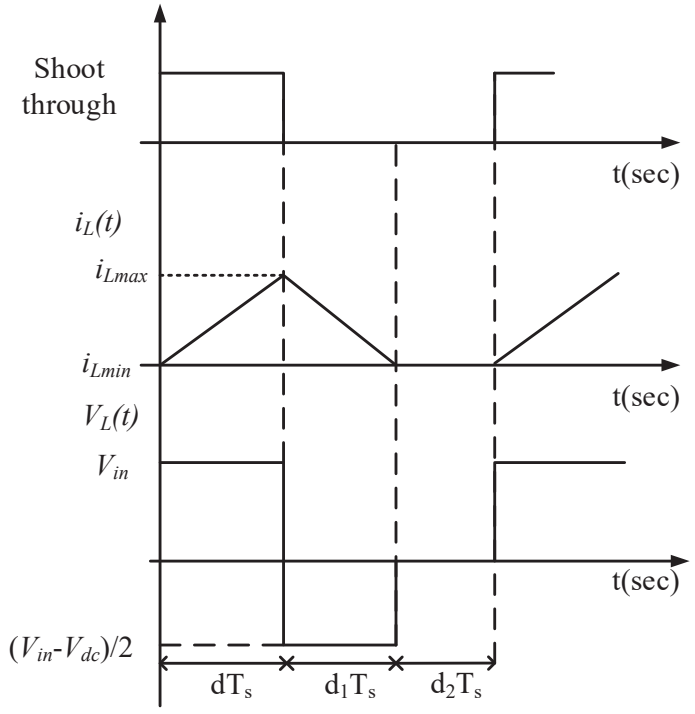


Figure 7.8: Steady state waveform during DCM

MHLZSI is considered as case study for DCM. As shown in Fig-7.1, above conditions are present in the MHLZI.

During DCM, the inductor current reaches zero before the start of next shoot through period, voltage across inductor is zero. So, the inductor voltage from Fig-7.8 is written as

$$\begin{aligned} V_L &= 0 && 0 \leq t < d_2 T_s \\ V_L &= V_{in} && 0 \leq t < dT_s \\ V_L &= \tfrac{V_{in}-V_{dc}}{2} && 0 \leq t \leq d_1 T_s \end{aligned} \tag{7.20}$$

Applying volt-sec principle across inductor

$$\int_0^{dT_s} V_L dt + \int_0^{d_1 T_s} V_L dt + \int_0^{d_2 T_s} V_L dt = 0 \tag{7.21}$$

From Equ-(7.20) and Equ-(7.21), following inequality is obtained:

$$dV_{in} + d_1 \frac{(V_{in} - V_{dc})}{2} = 0 \tag{7.22}$$

Hence, DC output voltage(say V_{dc}=V_{dcm} in DCM) is

$$V_{dcm} = \frac{2d + d_1}{d_1} V_{in} \tag{7.23}$$

where $d_1 = 1 - d - d_2$ and d_2 is period corresponding to DCM.

In Equ-(7.23), since $d_1 < (1 - d)$ for DCM, the effective DC voltage is greater as compared to case when converter is operated under CCM. For eg. at $d = 0.25$ and d_1=0.59, from Equ-(7.4), $V_{dc} = 116$ V under CCM, while from Equ-(7.23), $V_{dcm} = 130$ V for fixed 70 V input.

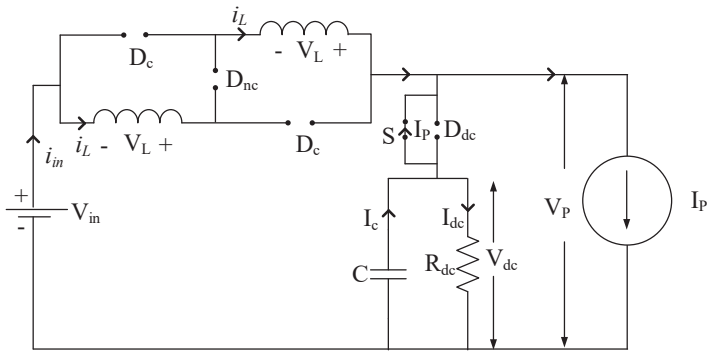


Figure 7.9: Operation of MHLZSI in DCM

As soon as the inductor current reaches zero, the diode D_{dc} is reverse biased, so the AC and DC load are isolated from the source, as shown in Fig-7.9. The DC load is supplied by the capacitor while zero voltage appears across the inverter. However, as the antiparallel switch, S is turned on, the capacitor starts supplying power to the AC load as well. So, both AC and DC load is supplied by the capacitor voltage during DCM. The rms AC load voltage in DCM is written as

$$V_{acm} = \frac{m}{2\sqrt{2}} \frac{2d + d_1}{d_1} V_{in} \tag{7.24}$$

Therefore, MHLZSI is able to operate satisfactorily in DCM with an antiparallel switch. Moreover, the MHLZSI exhibit higher gain in DCM. The gain of the converter for CCM with different cells is plotted in Fig-7.10a. It is observed that with the increase in the number of cells(n is number of cells), the voltage gain has a significant difference at higher duty ratio. For the same number of switched cells, the voltage gain in DCM is higher than CCM, as shown in Fig-7.10b. As the period of DCM increases, gain of the converter also increases. However, to achieve the optimum performance, peak to peak ripple current need to be restricted, correspondingly this imposes the limitation on the gain factor.

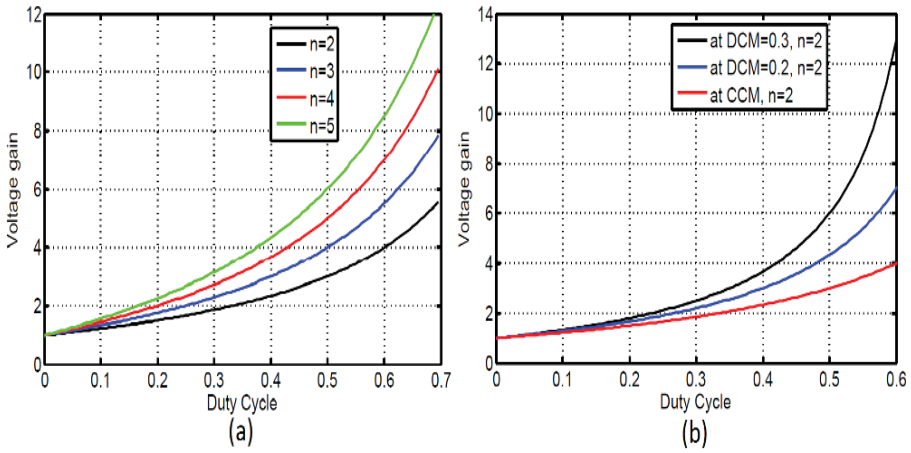


Figure 7.10: a) Gain in CCM b) Gain in DCM

7.4 PWM control pulses of proposed converter

Control pulses of the proposed converter are derived from the simple boost control strategy [113]. The schematic of control logic for generation of pulses is presented in Fig-7.11.

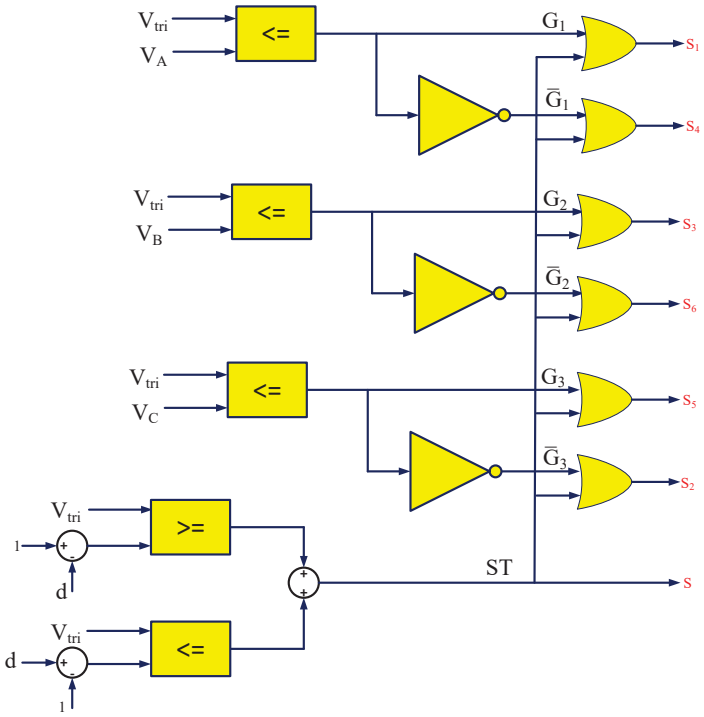


Figure 7.11: Logic diagram for control pulses

Generation of pulses is done in two steps: First, PWM for VSI is generated by comparing three phase sinusoidal pulses(V_A, V_B and V_C) with the triangular pulse(V_{tri}). The frequency of the triangular signal(f_s) must be very much higher than sinusoidal signal(f). The generated pulses have active and zero states. Secondly, for boost control, the generation of shoot through is done by comparing positive and negative dc quantities value($\pm V_s$), with the same triangular pulses as used for the three phase PWM inverter pulse generation. These shoot through pulses are placed in zero states of the inverter. The gate control signals for the converter are obtained using the following logical expression as

$$S_1 = G_1 \oplus ST, S_4 = \bar{G}_1 \oplus ST, S_3 = G_2 \oplus ST$$

$$S_6 = \bar{G}_2 \oplus ST, S_5 = G_3 \oplus ST, S_2 = \bar{G}_3 \oplus ST$$

Moreover, The switch S is controlled directly by shoot through(ST) pulses.

Mathematically, The triangular waveform is written as

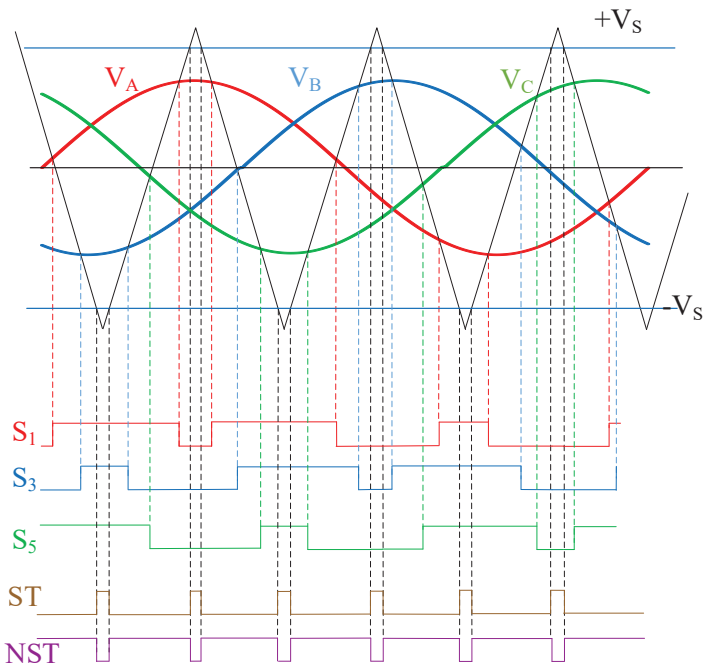


Figure 7.12: Generation for control pulses

$$V_{tri} = \begin{cases} -\frac{V_m}{T_s/4}\left(t - \frac{T_s}{4}\right) 0 < t < T_s/2 \\ \frac{V_m}{T_s/4}\left(t - \frac{3T_s}{4}\right) T_s/2 < t < T_s \end{cases} \tag{7.25}$$

From Fig-7.12, it is seen that

$$V_{tri}(t_1) = V_{tri}(t_2) = -V_s, t_2 - t_1 = \frac{dT_s}{2} \tag{7.26}$$

With the help of Equ-(7.25) and Equ-(7.26), following relations are deduced

$$t_1 = \frac{T_s}{2}\left(1 + \frac{V_s}{V_m}\right), t_2 = \frac{T_s}{2}\left(3 - \frac{V_s}{V_m}\right) \tag{7.27}$$

Replacing the values of t_1 and t_2 in Equ-(7.25), the expression for duty cycle is

$$d = 1 - \frac{V_s}{V_m} \tag{7.28}$$

Therefore, for duty cycle variation, either V_m or V_s is varied depending on the application requirement.

Moreover, the control pulse generation is done such that the condition $m + d \leq 1$ should be maintained strictly.

7.5 Design guidelines

For validation of switching frequency effect on NZ-DCM and converter gain in DCM, a 400 W prototype for proof of concept is designed and tested. The complete list for converter parameters is presented in Table-7.1.

Table 7.1: L-ZSI specification

Parameter	**Rating**
Total output power P	400 W
Maximum AC output power P_{ACmax}	320 W
Maximum DC output Power P_{DCmax}	269 W
Boost stage inductance L	0.56 mH
Boost stage capacitance C	100 μF
AC load	3.95 A
DC load	2.32 A
AC filter inductance(L_f)	1 mH
AC filter capacitance(C_f)	10 μF
Input voltageV_{in}	70 V

7.5.1 Inductor selection

In case of DC load and balanced three phase AC load, under steady state, low frequency ripple does not present. So the average inductor current is selected as per the Equ-(7.12). In Table-7.1, maximum total output power will be 400 W, however, AC power is maximized till 320 W, and correspondingly DC power is reduced to 80 W. Similarly, when DC power is at 269 W, AC power is reduced to 131 W. For 400 W power rating and duty cycle equal to 0.25, the average inductor current is I_L= 4.57 A. Generally, for boost converter 30% to 40% ripple is permissible. But in case of the high boost converter, this limit exceeds to optimize the size. In this chapter, peak to peak ripple current is chosen as 35% of average current(ΔI_L= 0.35*I_L). From Equ-(7.7), the inductor value is 0.56 mH for V_{in}=70 V and V_{dc}=116 V.

7.5.2 Capacitor selection

The capacitor has to handle the DC current in case of CCM, while in DCM it carries the sum of DC and AC load currents. So the capacitor is deigned as per the maximum current that flows through it. In this paper, the maximum current that capacitor handle is 2.32 A. The capacitance is calculated as

$$\Delta V = \frac{I_{\max} d}{f_s L} \tag{7.29}$$

For 1% of ripple voltage, from Equ-(7.29), the capacitance is 30 μF. However, in experiment 100 μF is selected due to availability issue.

7.5.3 Switch stress analysis

Inverter switches are subjected to the Boost voltage generated at the DC terminal. Therefore, the maximum voltage stress under which the switches operate, is equal to V_{dc}. Similarly, diode D_{dc} is also stressed upto voltage V_{dc}. The diode D_c is subjected to $\frac{V_{in}-V_{dc}}{2}$, on the other hand, D_{nc} is stressed by V_{in}.

The current through the inverter switches is equal to the sum of inductor currents during shoot through while it is equal to the AC load current (i_a,or i_b, or i_c) during non shoot through period. Therefore, the maximum amount of current(i_{inv}) flowing through the inverter switch is

$$i_{inv} = 2i_{L\max} + |i_{ap}| or\ |i_{bp}| or\ |i_{cp}| \tag{7.30}$$

where, subscript p denotes the peak value of corresponding phase current. $i_{L\max}$ is defined as

$$i_{L\max} = \frac{\Delta I_L}{2} + I_{Lavg} \tag{7.31}$$

The diode D_{nc} is turned ON during the non-shoot through state, hence maximum current through D_{nc} is $2i_{Lmax}$ whereas diodes D_c are forward biased during shoot through state therefore current through them is i_{Lmax}. The diode D_{dc} and switch S are connected in DC load path hence maximum current through switch S is $2i_{Lmax}$.

7.6 State space modelling

To design the PI controllers, a transfer function is required for the plant. To achieve this, state space modeling of the converter is done. During state space modelling, it is assumed

that diodes and switches are ideal.

7.6.1 Modelling for DC bus voltage

For designing the controller for DC bus voltage, inverter DC equivalent is considered. Three phase parameters are converter into its DC equivalent, where, $R_L = \frac{8}{3}R_{ac}$ and $L_L = \frac{L_{ac}}{R_{ac}}R_L$.

Shoot through state

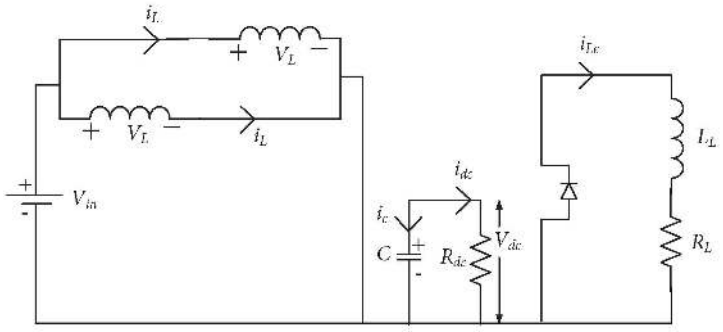


Figure 7.13: Shoot through state equivalent circuit

The reference current directions and voltage polarities for the converter are marked as shown in Fig-7.13. The steady state equation for the inductor current i_L :

$$V_L = L\frac{di_L}{dt} = V_{in} \tag{7.32}$$

$$\frac{di_L}{dt} = \frac{V_{in}}{L} \tag{7.33}$$

Upon application of KCL, state equation for V_c :

$$i_c = -i_{dc} \tag{7.34}$$

$$i_c = C\frac{dV_c}{dt} = -\frac{V_{dc}}{R_{dc}} \tag{7.35}$$

$$\frac{dV_c}{dt} = -\frac{V_{dc}}{R_{dc}C} \tag{7.36}$$

Upon application of KVL, state equation for i_{ac} :

$$L_L \frac{di_{Le}}{dt} = -i_{Le} R_L \tag{7.37}$$

$$\frac{di_{Le}}{dt} = -i_{Le} \frac{R_L}{L_L} \tag{7.38}$$

The output equations are as follows:

$$V_{dc} = V_c \; ; V_{Le} = R_L i_{Le} \tag{7.39}$$

The state space representation for shoot through state is

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \\ \frac{di_{Le}}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{1}{R_{dc}C} & 0 \\ 0 & 0 & -\frac{R_L}{L_L} \end{bmatrix}}_{A_1} \begin{bmatrix} i_L \\ V_c \\ i_{Le} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix}}_{B_1} V_{in} \tag{7.40}$$

$$\begin{bmatrix} V_{dc} \\ V_{Le} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & R_L \end{bmatrix}}_{C_1} \begin{bmatrix} i_L \\ V_c \\ i_{Le} \end{bmatrix} \tag{7.41}$$

Zero state

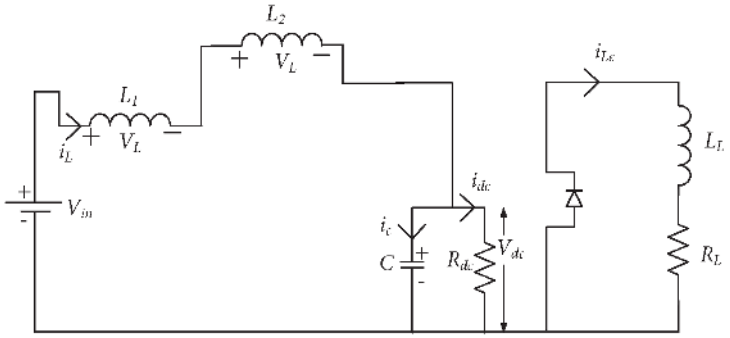


Figure 7.14: Zero state equivalent circuit

The reference current directions and voltage polarities for the converter are marked shown in Fig-7.14. The steady state equation for the inductor current i_L :

$$-V_{in} + 2V_L + V_c = 0 \tag{7.42}$$

$$V_L = \frac{1}{2}\left(V_{in} - V_c\right) \tag{7.43}$$

$$\frac{di_L}{dt} = \frac{1}{2L}\left(V_{in} - V_c\right) \tag{7.44}$$

The state equation for V_c is represented as:

$$i_c = i_L - i_{dc} \tag{7.45}$$

$$C\frac{dV_c}{dt} = i_L - \frac{V_{dc}}{R_{dc}} \tag{7.46}$$

$$\frac{dV_c}{dt} = \frac{i_L}{C} - \frac{V_{dc}}{CR_{dc}} \tag{7.47}$$

The state equation for i_{Le} is:

$$\frac{di_{Le}}{dt} = -\frac{R_L}{L_L} i_{Le} \tag{7.48}$$

The output equations will be:

$$V_{dc} = V_c \; ; V_{Le} = R_L i_{Le} \tag{7.49}$$

The state space representation for zero state is

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \\ \frac{di_{Le}}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{2L} & 0 \\ \frac{1}{C} & -\frac{1}{R_{dc}C} & 0 \\ 0 & 0 & -\frac{R_L}{L_L} \end{bmatrix}}_{A_2} \begin{bmatrix} i_L \\ V_c \\ i_{Le} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{2L} \\ 0 \\ 0 \end{bmatrix}}_{B_2} V_{in} \tag{7.50}$$

$$\begin{bmatrix} V_{dc} \\ V_{Le} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & R_L \end{bmatrix}}_{C_2} \begin{bmatrix} i_L \\ V_c \\ i_{Le} \end{bmatrix} \tag{7.51}$$

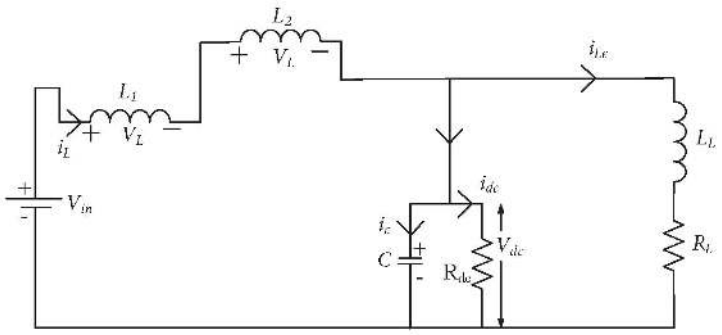


Figure 7.15: Power state equivalent circuit

Power state

Both AC load and DC load during power state is connected to source as shown in Fig-7.15. State equation for inductor current i_L is:

$$-V_{in} + 2V_L + V_c = 0 \tag{7.52}$$

$$V_L = \frac{1}{2}\left(V_{in} - V_c\right) \tag{7.53}$$

$$\frac{di_L}{dt} = \frac{1}{2L}\left(V_{in} - V_c\right) \tag{7.54}$$

The state equation for V_c is:

$$-V_c + V_{dc} = 0 \tag{7.55}$$

$$i_c = i_L - i_{dc} - i_{Le} \tag{7.56}$$

$$\frac{dV_c}{dt} = \frac{i_L}{C} - \frac{V_c}{R_{dc}C} - \frac{i_{Le}}{C} \tag{7.57}$$

The state equation for i_{Le} is:

$$\frac{di_{Le}}{dt} = \frac{V_c}{L_L} - \frac{R_L i_{Le}}{L_L} \tag{7.58}$$

The state space representation for power state is

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \\ \frac{di_{Le}}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{2L} & 0 \\ \frac{1}{C} & -\frac{1}{R_{dc}C} & -\frac{1}{C} \\ 0 & \frac{1}{L_L} & -\frac{R_L}{L_L} \end{bmatrix}}_{A_3} \begin{bmatrix} i_L \\ V_c \\ i_{Le} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{2L} \\ 0 \\ 0 \end{bmatrix}}_{B_3} V_{in} \tag{7.59}$$

$$\begin{bmatrix} V_{dc} \\ V_{Le} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & R_L \end{bmatrix}}_{C_3} \begin{bmatrix} i_L \\ V_c \\ i_{Le} \end{bmatrix} \tag{7.60}$$

For determining the dynamic behavior of the state variables, the input signals:

$$v_{in} = V_{in} + \hat{v}_{in} \tag{7.61}$$

and control variable

$$d = D + \hat{d} \tag{7.62}$$

$$m = M + \hat{m} \tag{7.63}$$

and the state variables

$$x = X + \hat{x} \tag{7.64}$$

are perturbed around their steady state value.

$$\dot{x} = Ax + Bu \tag{7.65}$$

$$\begin{aligned} \dot{X} + \hat{\dot{x}} = &\left(A_1 d + A_2 \left(1 - d - m\right) + A_3 m\right)\left(X + \hat{x}\right) \\ &+ \left(B_1 d + B_2 \left(1 - d - m\right) + B_3 m\right)\left(U + \hat{u}\right) \end{aligned} \tag{7.66}$$

With assumption: $\frac{\hat{x}}{X} << 1; \left(\hat{x} - \hat{d}\right) \to 0$

by solving the above Equ-(7.65) and Equ-(7.66),

$$\begin{aligned} \hat{\dot{x}} = &A\hat{x} + B\hat{u} + \left[\left(A_1 - A_2\right)X + \left(B_1 - B_2\right)U\right]\hat{d} \\ &+ \left[\left(A_3 - A_2\right)X + \left(B_3 - B_2\right)U\right]\hat{m} \end{aligned} \tag{7.67}$$

$$\begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \frac{dv_c}{dt} \\ \frac{di_{Le}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-D}{2L} & 0 \\ \frac{1-D}{C} & -\frac{1}{R_{dc}C} & -\frac{M}{C} \\ 0 & \frac{M}{L_L} & -\frac{R_L}{L_L} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \\ \hat{i}_{Le} \end{bmatrix} + \begin{bmatrix} \frac{1+D}{2L} & \frac{V_c+V_{in}}{2L} & 0 \\ 0 & -\frac{I_L}{C} & -\frac{I_{Le}}{C} \\ 0 & 0 & \frac{V_c}{L_L} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{d} \\ \hat{m} \end{bmatrix} \tag{7.68}$$

$$\begin{bmatrix} \hat{v}_{dc} \\ \hat{v}_{Le} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & R_L \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \\ \hat{i}_{Le} \end{bmatrix} \tag{7.69}$$

Taking the laplace transform of Equ-(7.68), following equations are obtained:

$$s\hat{i}_L(s) = -\frac{1-D}{2L}\hat{v}_c(s) + \frac{1+D}{2L}\hat{v}_{in}(s) + \frac{V_c+V_{in}}{2L}\hat{d}(s) \tag{7.70}$$

$$\begin{aligned} s\hat{v}_c(s) = {} & \frac{1-D}{C}\hat{i}_L(s) - \frac{1}{R_{dc}C}\hat{v}_c(s) - \frac{M}{C}\hat{i}_{Le}(s) - \frac{I_L}{C}\hat{d}(s) \\ & - \frac{I_{Le}}{C}\hat{m}(s) \end{aligned} \tag{7.71}$$

$$s\hat{i}_{Le}(s) = \frac{M}{L_L}\hat{v}_c(s) - \frac{R_L}{L_L}\hat{i}_{Le}(s) + \frac{V_c}{L_L}\hat{m}(s) \tag{7.72}$$

To eliminate $\hat{d}(s)$ from the above equations, consider $\hat{i}_L(s) = \hat{i}_{ref}(s)$, $\hat{m}(s) = 0$, $\hat{v}_{in}(s) = 0$

$$\hat{d}(s) = \frac{2Ls\hat{i}_{ref}(s) + (1-D)\hat{v}_c(s)}{V_c+V_{in}} \tag{7.73}$$

Since, during current mode control, the dynamics of the converter gets simpler due to the fact that the pole coming from the inductor pushed to the higher frequency. So, the current mode control is adopted for converter operation. The resultant control rule in terms of i_{ref} after eliminating $\hat{d}(s)$ from Equ-(7.70), Equ-(7.71) and Equ-(7.72), is:

$$\begin{aligned} & \left.\frac{\hat{v}_c(s)}{\hat{i}_{ref}(s)}\right|_{\hat{m}(s)=0,\hat{v}_{in}(s)=0} \\ & = \frac{\left(\frac{1-D}{C}\right)\left(s+\frac{R_L}{L_L}\right)\left(1-\frac{LI_L}{V_{in}}s\right)}{\left[s^2 + \left[\frac{R_L}{L_L} + \frac{I_L}{C}\frac{(1-D)^2}{2V_{in}}\right]s + m^2 + \frac{I_L}{C}\frac{(1-D)^2}{2V_{in}}\frac{R_L}{L_L}\right]} \end{aligned} \tag{7.74}$$

Since $m^2 <<<< \frac{I_L}{C}\frac{(1-D)^2}{2V_{in}}\frac{R_L}{L_L}$ we can neglect m^2 so the control rule is:

$$\left.\frac{\hat{v}_c(s)}{\hat{i}_{ref}(s)}\right|_{\hat{m}(s)=0,\hat{v}_{in}(s)=0} = \frac{-\left(\frac{LI_L}{V_{in}}\right)\left(\frac{1-D}{C}\right)\left(s+\frac{R_L}{L_L}\right)\left(s-\frac{V_{in}}{LI_L}\right)}{\left(s+\frac{R_L}{L_L}\right)\left(s+\frac{I_L}{C}\frac{(1-D)^2}{2V_{in}}\right)} \tag{7.75}$$

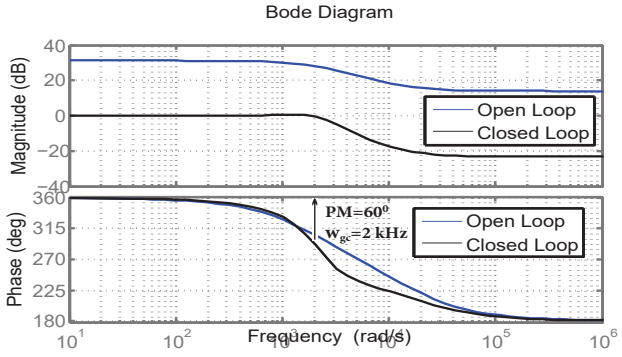


Figure 7.16: Bode plot for DC bus voltage controller

From system transfer function, it is clearly shown that a zero is present in the right half plane. So, this system is non-minimum phase system. To make system stable in closed loop, PI controller is designed. The system phase margin is kept at 60° while gain cross over frequency is equal to 2 kHz. The bode plot corresponding to open loop and close loop system are shown in Fig-7.16.

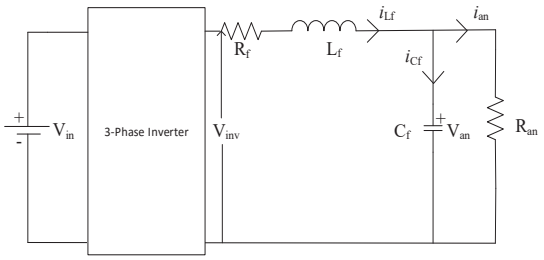


Figure 7.17: AC equivalent circuit

7.6.2 AC voltage controller

For AC voltage controller, DC load is assumed to be zero as this controller has to handle only AC current. So, equivalent circuit corresponding to AC load is shown in Fig-7.17.

From Fig-7.17, following equations are written

$$\frac{di_{Lf}}{dt} = \frac{R_f}{L_f} i_{Lf} + \frac{1}{L_f}\left(V_{inv} - V_{an}\right) \tag{7.76}$$

$$\frac{dV_{an}}{dt} = \frac{1}{C_f} i_{Lf} - \frac{V_{an}}{R_{an} C_f} \tag{7.77}$$

d-q representation of these equations is given as

$$\begin{bmatrix} \dot{I}_d \\ \dot{I}_q \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & \omega \\ -\omega & -\frac{R_f}{L_f} \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \frac{1}{L_f} \begin{bmatrix} V_{inv} - V_d \\ V_{inv} - V_q \end{bmatrix} \tag{7.78}$$

$$\begin{bmatrix} \dot{V}_d \\ \dot{V}_q \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_{an} C_f} & \omega \\ -\omega & -\frac{1}{R_{an} C_f} \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} + \frac{1}{C_f} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{7.79}$$

By taking laplace transformation on both side for both equation and re-arranging them

$$\frac{I_d}{W_{id}(s)} = \frac{I_q}{W_{iq}(s)} = \frac{1}{sL_f + R_f} \tag{7.80}$$

$$\frac{V_d}{W_{Vd}} = \frac{V_q}{W_{Vq}} = \frac{R_{an}}{sR_{an}C_f + L} \tag{7.81}$$

where,

$W_{id}(s) = V_{inv} - V_d + \omega L_f I_q$, $W_{Vd}(s) = I_d + \omega C_f V_q$

$W_{iq}(s) = V_{inv} - V_q - \omega L_f I_d$, $W_{Vq}(s) = I_q - \omega C_f V_d$

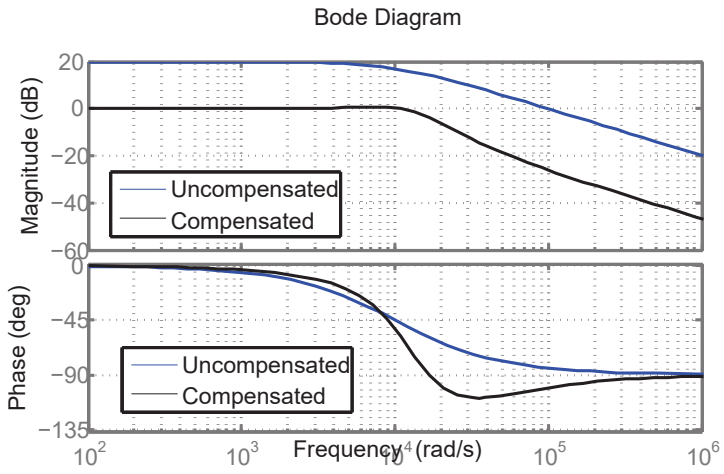


Figure 7.18: AC current controller

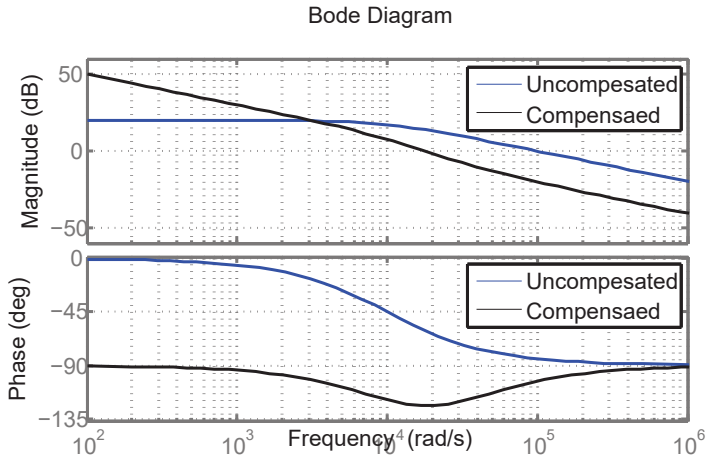


Figure 7.19: AC voltage controller

The bode plot for compensated and uncompensated current control loop is shown in Fig-7.18. The tuning for closed loop control is done for 60° phase margin and 11 kHz gain cross over frequency.

Similarly, for voltage control loop the tuning is achieved at 60° phase margin but gain cross over frequency is equal to 112 rad/sec. The compensated and uncompensated loop are shown in Fig-7.19.

7.7 Closed loop of hybrid LZSI

The closed loop schematic is shown in Fig-7.20. The closed loop control consists two controlling parts, one is dc bus voltage control and other is three phase AC voltage control. DC bus voltage control consists two parts itself: inner current control and outer voltage control loop. The reference signal for inner current loop is generated by the voltage controller. In the inner current loop, the reference signal is compared with the inductor current obtained after sensing to generate the duty cycle. This duty cycle serves as the control pulse for the boost stage.

AC voltage control is done in three steps: 1) three phase AC quantity is converted into two phase quantity. To achieve this, three phase quantity is first converter into α-β co-ordinates using Clark transformation. To converter this into d-q reference frame park

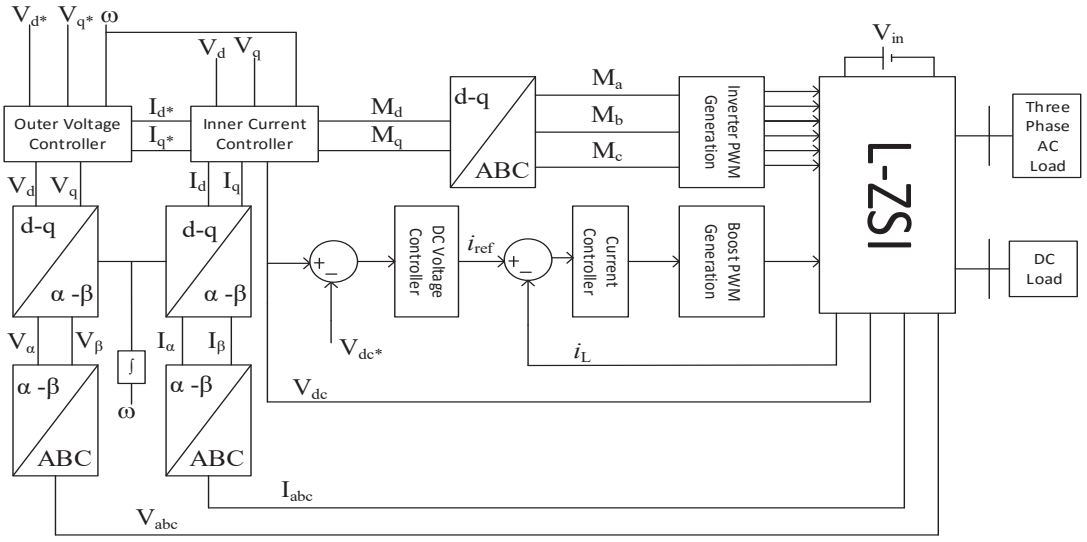


Figure 7.20: Closed loop schematic of hybrid LZSI

transformation is used. Clark transformation is

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & \frac{1}{3} \\ 0 & \frac{2}{\sqrt{3}} & -\frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{7.82}$$

and Park transformation is given as

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ \cos\theta & -\sin\theta \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \tag{7.83}$$

2) After conversion, *d-q* voltage and current is determined. These quantities are compared with the reference signals. The reference voltage V_d^* is set equal to the required AC voltage, while reference V_q^* is equal to zero. To control the error in voltage, two separate PI controllers are designed. These PI controllers generate reference currents I_d^* and I_q^*. These reference currents are compared with sensed *d-q* currents. To control the error in current again two PI controller are designed. These PI controller generates modulating signals in *d-q* frame.

3) These quantities are then converter into a-b-c quantity using inverse Clark and park transformation. These signals are compared against the triangular carrier wave so as to generate three phase inverter pulses.

7.8 Simulation and experimental results

The maximum power rating of AC and DC load is decided to validate the CCM as listed in Table-7.1. For changing the mode of the converter from CCM to NZ-DCM or DCM, the resistance of either AC load or DC load is changed. The other design parameters for the experiment are also presented in Table-7.1. To validate the converter performance under CCM, NZ-DCM, FCCM and DCM, a layout of proposed structure is designed using proteus software. For PCB designing, the shortest length for interconnection between different nodes is ensured so as to minimize the stray inductance. The printed hardware is shown in Fig-7.21. The components detail used in the hardware with their manufacturers and rating are presented in Table-7.2. For measurement of current, Agilent probe is used. The spikes observed in experimental results are due to the stray inductance of connecting wire.

Table 7.2: Components used

Component	**Manufacturer**	**Model No.**	**Rating**
MOSFET	Semiconductor Tech.	STW10WK60Z	600V, 10A
Diode	Fairchild	ISL9R1560G2	600V, 15A
Capacitor	Multicomp	MCKSK400M101K32S	400V, 100μF
Inductor	Coilcraft	PCV-2-564-082	7A, 560μH

For generation of control pulses in hardware, field programmable gate array board (NEXYS-4) is used which has 450 MHz internal clock frequency. Though various control techniques are available for controlling [105,106,113], simple boost technique is considered so as to provide independent control of m and d. The gate pulses for the S_1, S_4, S_3 and S_6 are indicated in Fig-7.22a. For S_5 and S_2, controlling pulses are shown in Fig-7.22b. To control the antiparallel switch present across the diode, a non shoot through(NST) pulse is generated, which is shown in Fig-7.22b.

For ensuring the feasibility of designed prototype, the proposed converter is validated for CCM, NZ-DCM, FCCM and DCM.

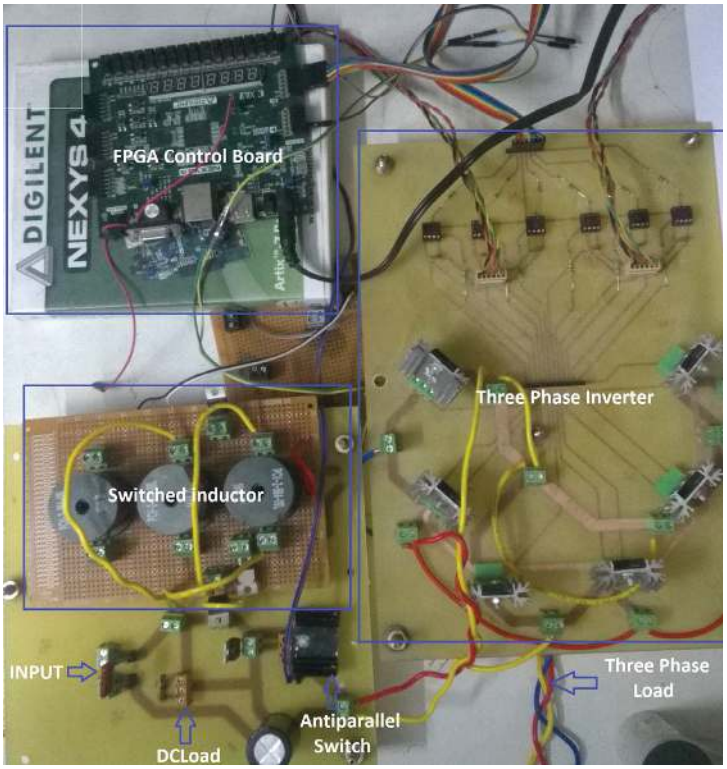
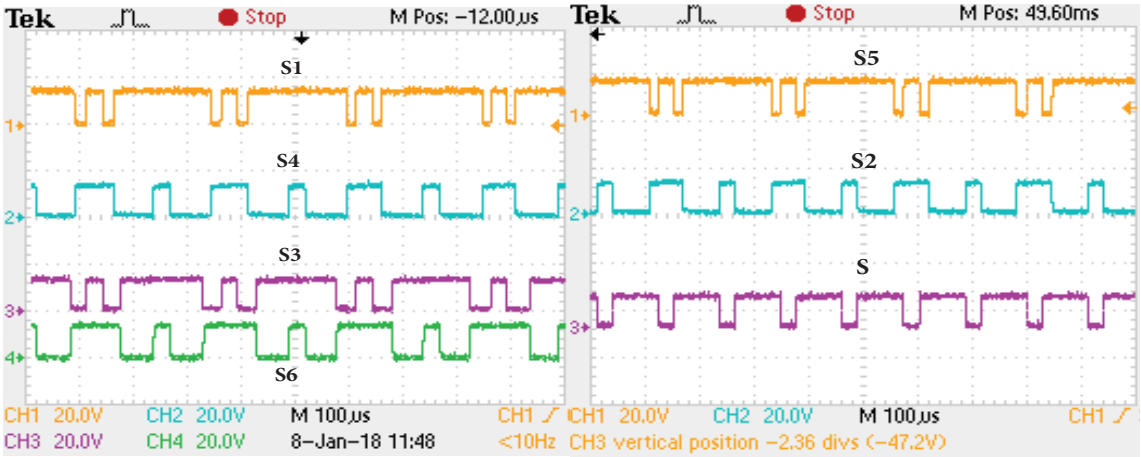


Figure 7.21: Experimental set up



(a) Pulses for S_1, S_4, S_3, S_6

(b) Pulses for S_5, S_2, S

Figure 7.22: Control pulses

7.8.1 CCM

For CCM operation, duty cycle and modulation index are kept at 0.25 and 0.675 respectively. Both AC and DC load are 50 Ω each. As per Equ-(7.16), for CCM, $k_L > k_R$ which is achieved in this case, as k_L=2.32 and k_R=0.209. The inductor current is triangular in nature, and DC link voltage has constant level during NST, as shown in Fig-7.23. The AC voltage has lower THD(i.e., 4%) , as shown in Fig- 7.24. Moreover, DC voltage is stiff in nature and has low ripple(<1%) as shown in Fig-7.24. Therefore, in CCM, HLZSI operates satisfactorily with lower THD in AC voltage and lower DC voltage ripple.

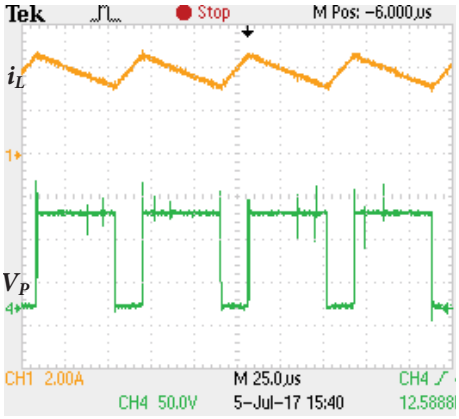


Figure 7.23: MHLZSI CCM: a) Inductor current b) DC link voltage [$Ch1 : 2A/div, Ch4 : 50V/div$]

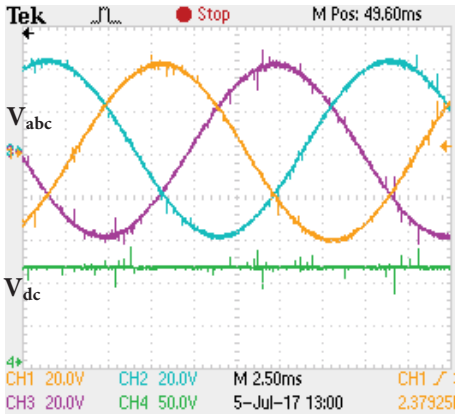


Figure 7.24: MHLZSI CCM: a) AC phase voltage b) DC voltage [$Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div$]

7.8.2 NZ-DCM

For NZ-DCM, duty cycle and modulation index kept same as CCM while AC load is changed to 7 Ω and DC load varied to 200 Ω. To evaluate the dependency of switching frequency or inductor on NZ-DCM, two cases are considered.

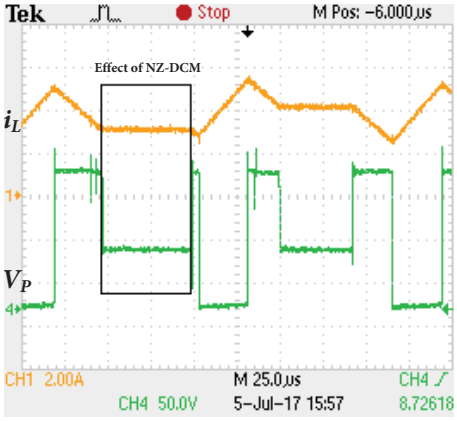


Figure 7.25: NZ-DCM at 10kHz: a) Inductor current b) DC link voltage [$Ch1 : 2A/div, Ch4 : 50V/div$]

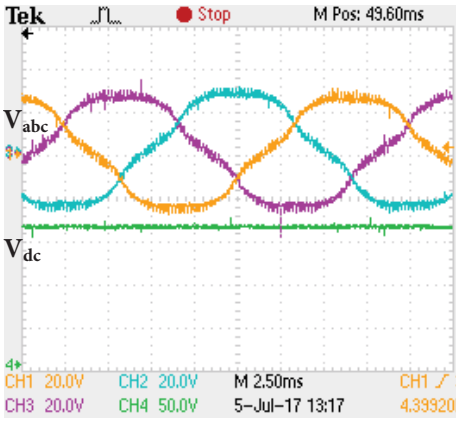


Figure 7.26: NZ-DCM at 10kHz: a) AC phase voltage b) DC voltage [$Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div$]

NZ-DCM at 10 kHz

In this case, k_L=0.6 and k_R=1.36 which violates the Equ-(7.16), thereby converter enters into NZ-DCM. The inductor current during NZ-DCM saturates due to which the diode is reverse biased, and DC link voltage experiences a dip, as shown in Fig-7.25. This mode

increases the DC voltage to higher than the expected and injects high THD(14%) in AC voltage, as presented in Fig-7.26. Therefore, the performance of AC load is deteriorated. The DC voltage observed is 50 V higher than the theoretical which is not desirable. This high voltage increases the voltage stress across the capacitor and inverter switches. This would increase the losses present in the converter and therefore efficiency will be reduced.

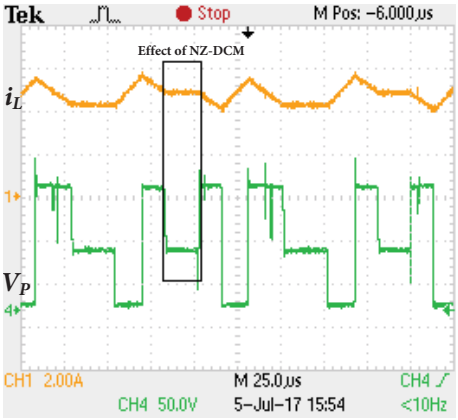


Figure 7.27: NZ-DCM at 20kHz: a) Inductor current b) DC link voltage $[Ch1 : 2A/div, Ch4 : 50V/div]$

NZ-DCM at 20 kHz

The parameter k_L is same as 10 kHz operation, while due to change in frequency, k_R is changed to 1.34 which violates the Equ-(7.16). Though the converter is still in NZ-DCM, the NZ-DCM appears for small duration as k_R is reduced. The profile of inductor current and DC link voltage confirms that NZ-DCM occurs for the smaller duration, as shown in Fig-7.27. The DC link voltage rises by 40 V from expected value, and THD in AC voltage is increased to 10%, as shown in Fig-7.28. This shows that at the higher switching frequency, the effect of NZ-DCM is relaxed and converter performance is improved. This will further reduce the losses and improve the efficiency.

7.8.3 Forced continuous current mode(FCCM)

To bring the converter into FCCM, the antiparallel switch(S) is turned ON by NST. As soon as, NZ-DCM comes into picture, diode D_{dc} is reverse biased and switch S is turned ON, facilitating the flow of current. Due to this, inductor current discharges through

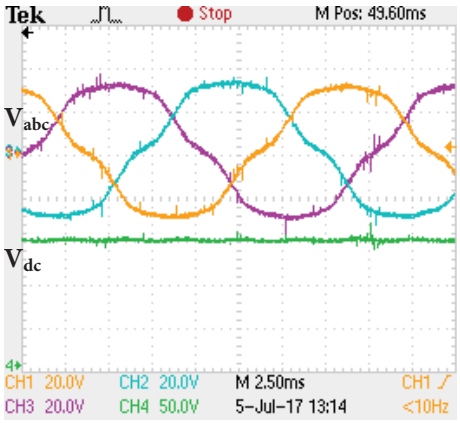


Figure 7.28: NZ-DCM at 20kHz: a) AC phase voltage b) DC voltage $[Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div]$

the AC load and follows the triangular nature. Also DC link voltage is stiff during NST period, as shown in Fig-7.29. The DC voltage is same as theoretical and AC voltage experiences lower THD(<4%), as shown in Fig-7.30. Hence, lower voltage across switch and capacitor is achieved. So, the antiparallel switch allows the converter to operate satisfactorily in wide range and therefore performance of the AC load is improved. In addition, antiparallel switch may be utilized to achieve higher gain in DCM which is explained in the following section.

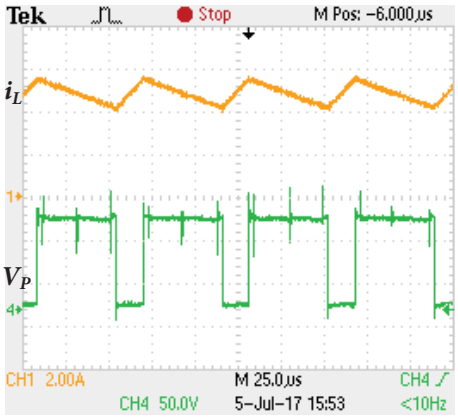


Figure 7.29: FCCM: a) Inductor current b) DC link voltage $[Ch1 : 2A/div, Ch4 : 50V/div]$

7.8.4 DCM

Due to the presence of antiparallel switch in the proposed converter, an extra benefit in terms of gain is achieved during DCM. To prove the feasibility of MHLZSI under DCM,

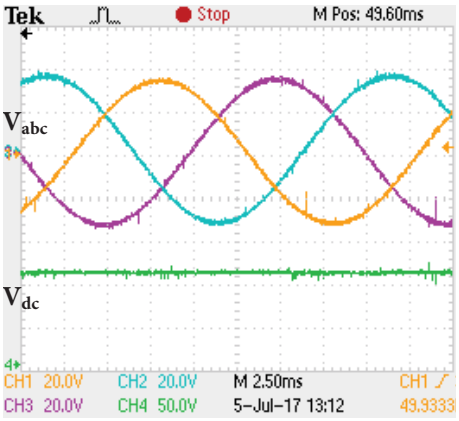


Figure 7.30: FCCM: a) AC phase voltage b) DC voltage $[Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div]$

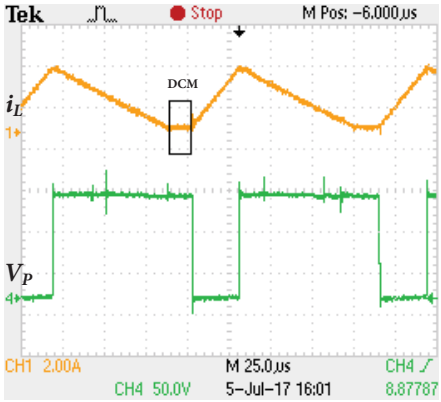


Figure 7.31: Resistive DCM: a) Inductor current b) DC link voltage $[Ch1 : 2A/div, Ch4 : 50V/div]$

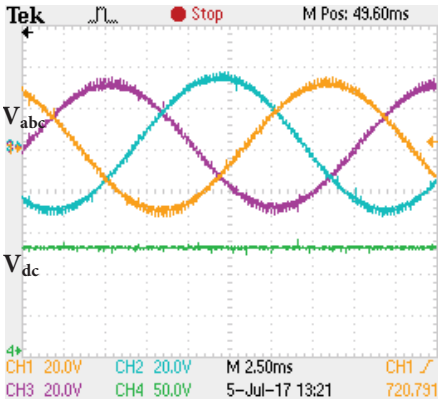


Figure 7.32: Resistive DCM: a) AC phase voltage b) DC voltage $[Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div]$

the converter is validated for resistive and highly inductive load.

Resistive load

To validate this, following parameters are considered: d=0.25, m=0.675, switching frequency 5 kHz, DC load is 200 Ω and AC load is 100 Ω. In experiment, as shown in Fig-7.31, the duty cycle d_2 is 0.16 which brings d_1=0.59, as per Equ-(7.23). The DC output is lifted to 130 V as shown in Fig-7.32, which is 14 V higher than the CCM. Moreover, the converter performance is similar to FCCM, as stiff DC voltage and lower THD is maintained. Therefore, the same converter is beneficial when higher voltage gain is required with better performance.

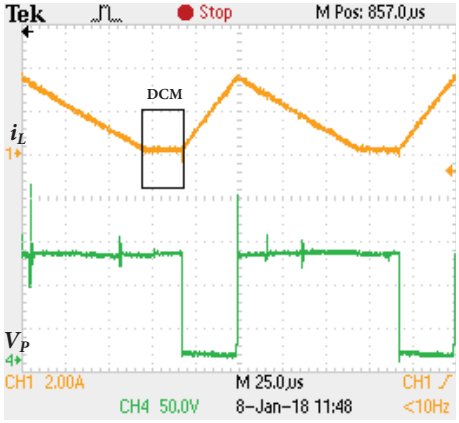


Figure 7.33: Inductive DCM: a) Inductor current b) DC link voltage [$Ch1 : 2A/div, Ch4 : 50V/div$]

Inductive load

For high inductive load testing, following parameters are considered: d=0.25, m=0.675, switching frequency 4 kHz, R_{dc}=200 Ω , R_{ac}= 50 Ω and X_L=94 Ω. As $\frac{X_L}{R_{ac}} > 1$ or phase angle is 62^0, therefore, inductive load is said to be highly inductive in nature. At this load, as shown in Fig-7.33, d_2 is 0.2, therefore d_1 is 0.55, as per Equ-(7.23). From Equ-(7.23), the DC gain is 134 V which is 18 V higher as compared to CCM. As the AC voltage and current are sinusoidal in nature as shown in Fig-7.34, the MHLZSI satisfactorily operates in inductive load condition. However, THD in AC voltage is around 9% which is due to inductive load. So, the proposed converter is suitable for resistive and inductive load to have higher gain in DCM.

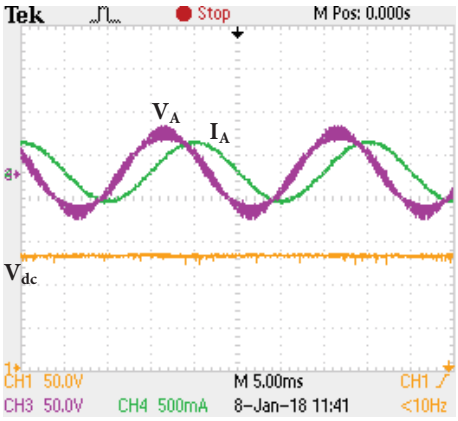


Figure 7.34: Inductive DCM: a) AC phase voltage b) DC voltage $[Ch1 : 50V/div, Ch2 : 0.5A/div, Ch3 : 50V/div, Ch4 : 50V/div]$

7.8.5 Closed loop analysis

For verification of closed loop under different operating condition, the simulation is done on MATLAB/Simulink platform.

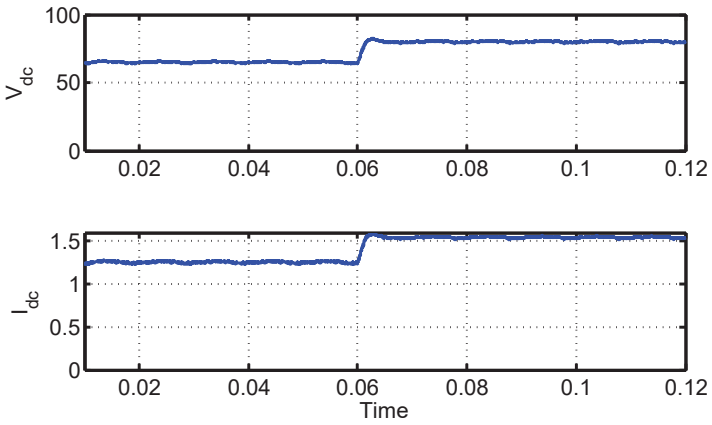


Figure 7.35: DC reference tracking a) DC voltage b) DC current

Reference DC voltage tracking characteristics

DC voltage tracking shows the performance of DC voltage controller and its characteristics. To validate this, change in voltage from 65 V to 85 V DC is given at reference input. The controller exhibits the excellent tracking characteristics with 0.004 sec settling time. The response is shown in Fig-7.35. With no change in AC voltage or load there must be no change at AC end. Therefore, ruggedness of the controller against the load variation

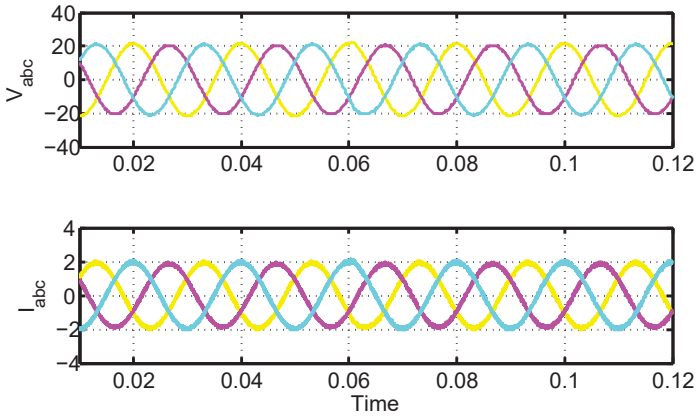


Figure 7.36: DC reference tracking a) AC voltage b) AC current

is ensured as shown in Fig-7.36 by adjusting the modulation index.

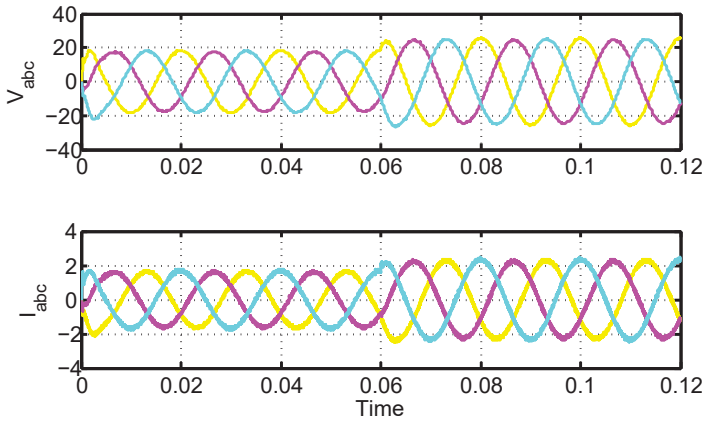


Figure 7.37: AC reference tracking a) AC voltage b) AC current

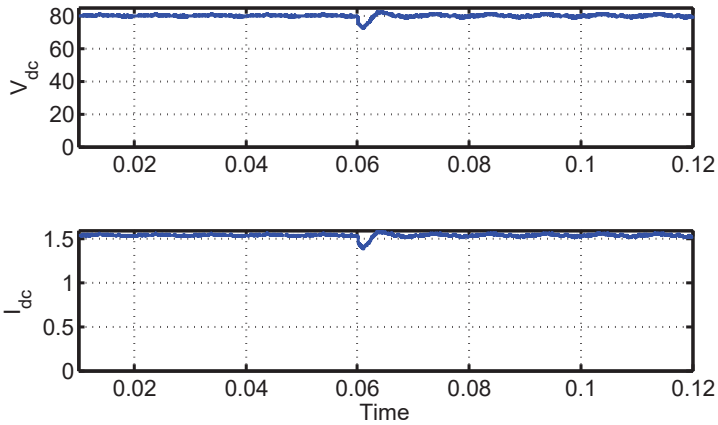


Figure 7.38: AC reference tracking a) DC voltage b) DC current

Reference AC voltage tracking characteristics

Maintaining DC voltage at 80 V, AC voltage controller is subjected to step change in input from 18 V to 25 V. As shown in Fig-7.37, the voltage is changed from 18 V to 25 V very quickly. This reflects the controller excellent characteristics to track the reference voltage. In this case, the DC voltage controller will also subject to transient change in addition to AC controller. This is due the fact that, as AC voltage changes the load current at AC increases so the current in inductor also increases. Increase in inductor current affects the performance of the DC controller transiently. But with in 0.007 sec, it is able maintain constant voltage and current at DC end as shown in Fig-7.38.

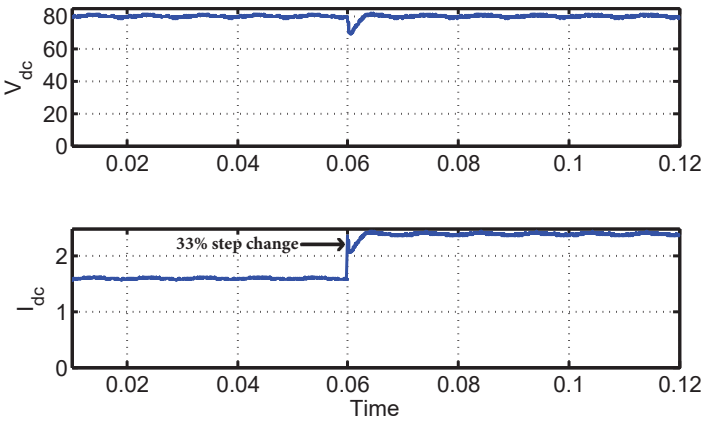


Figure 7.39: DC load variation at fixed AC load a) DC voltage b) DC current

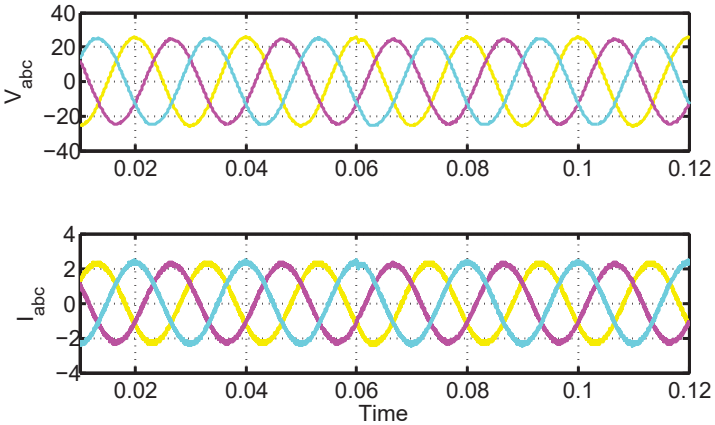


Figure 7.40: DC load variation at fixed AC load a) AC voltage b) AC current

DC load variation characteristics

The DC load variation characteristics represents robustness against the variable in load for constant voltage. The controller is subjected to step increase in load of 33% higher magnitude. The current at the DC end is increased to 2.42 A form 1.6 A. Although at transient, the controller observes a dip in DC voltage but settled to 80 V within 0.005 sec as shown in Fig-7.39. This shows the controller is able to stabilize the load variation. On the other hand, AC controller still able to supply constant demand as shown in Fig-7.40

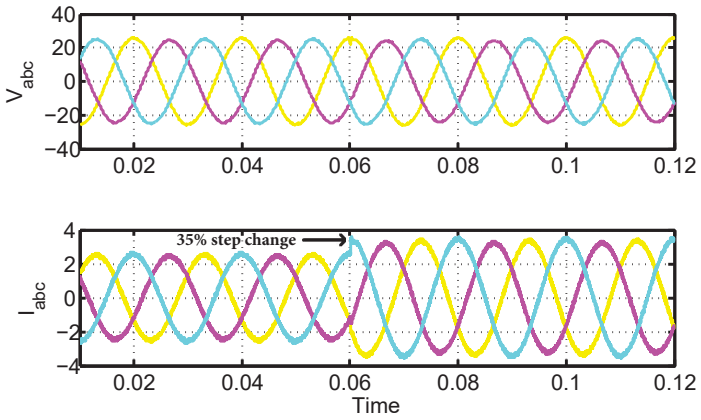


Figure 7.41: AC load variation at fixed DC load a) AC voltage b) AC current

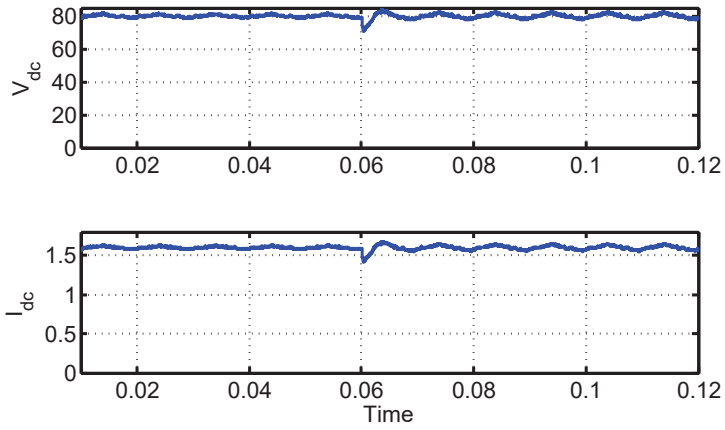


Figure 7.42: AC load variation at fixed DC load a) DC voltage b) DC current

AC load variation characteristics

Similar like DC load variation, AC load variation characteristics represents AC controller performance. Step change in AC load of 35% is applied at AC load end. The current tend

to increase but controller is still able to maintain constant AC voltage which is the sign of sublime controller. The performance of DC controller is shown in Fig-7.41. But DC capacitor which is designed on the basis of 10 Ω resistance, subjected to higher average output current due to increase in load. This produces the ripple in DC voltage and current as shown in Fig-7.42.

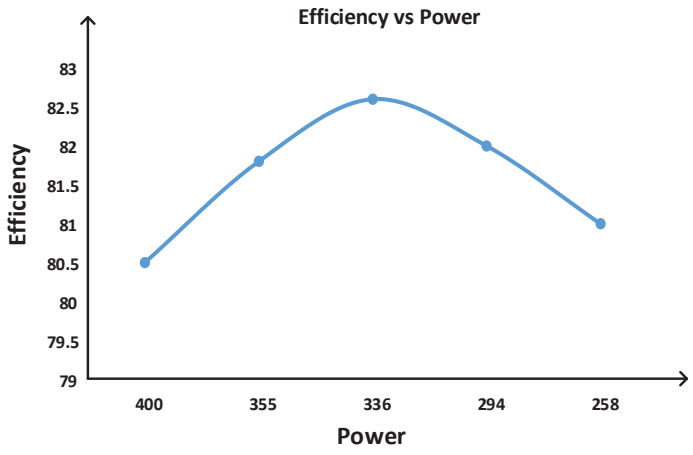


Figure 7.43: Efficiency of proposed converter

7.8.6 Efficiency

The efficiency of MHLZSI is dependent on the forward voltage drop of diode(V_f) and MOSFET(V_{sd}), switching frequency, internal resistance of inductance(r_L) and capacitance(r_c). From the data sheet, different parameters are selected as: V_f=2.2 V, V_{sd}=1.2 V, r_L=0.2 Ω, and r_c=1.57 Ω. The switching frequency is selected as 5 kHz. At simulation platform, the calculated efficiency is 83.5% which does not take into account the switching losses, and core losses. However, for the same rating, the experimental calculated efficiency is 81.5% which considers both switching and core losses. For different power rating, the efficiency curve is shown in Fig-7.43.

7.9 Conclusion

In depth analysis of NZ-DCM along with DCM for MHLZSI is presented in this chapter. The inter dependency of NZ-DCM on switching frequency or inductor is proved theoretically and validated experimentally. At 10 kHz, the inductor current becomes constant

for larger duration as compared to 20 kHz. The effect of switching frequency is noticed in terms of DC voltage and THD in AC voltage. At higher switching frequency, the difference between the theoretical and obtained DC voltage is low and THD is also small as compared to the case when switching frequency is low. The FCCM is validated to offer the better performance of the converter. In addition, switch present for FCCM to occur, increases the gain of the converter under DCM. For the same operating condition, the converter gain is lifted by 14 V during DCM as compared to CCM. Moreover, feasibility of MHLZSI to operate under highly inductive load condition is validated. Additionally, closed loop response of the proposed converter is validated which is suitable from dynamical point of view.

In chapter 6 and 7, hybrid converters are reported which can feed both AC and DC load. However, the DC voltage available will be always higher than the input voltage. In the next chapter, a buck boost derived hybrid converter will be presented which can buck and boost the DC voltage.