Chapter 5

5.1 Introduction

The metal oxide thin film transistors (TFT) are appropriate candidates for the application in many advanced electronics, such as flexible and transparent electronics due to their high carrier mobility, excellent operational stability, high optical transparency and diverse fabrication methods.[187] Additionally, because of the development in the synthesis of metal oxides through different solution-processed, oxide TFTs can be fabricated in a large area and in a roll-to-roll fabrication method that can reduce the production cost of those electronics significantly.[151] Instead of these advantages, metal oxide TFT with traditional SiO_2 requires high operating voltages (≥40V) due to low dielectric constant (κ) of SiO_2 which is not suitable for many applications like lightweight portable electronics.[213] This issue has been greatly resolved by developing different high dielectric constant (high-κ) gate insulator that not only reduces the operating voltage of the device but also improves the carrier mobility with respect to the traditional SiO_2 dielectric. Few examples of such kind of high-κ dielectrics are TiO_2 [196, 197] , Ta_2O_5[194], Y_2O_3[195], ZrO_2[198, 199], HfO_x[65], $HfLaO_x$[200], $LaAlO_3$[201], silicates[202, 203]. Apart from the high-κ dielectric, low leakage current density with minimum semiconductor/dielectric interface-trap-states density (N_{max}) of the gate insulator are key requirements to achieve high performance and low operating voltage TFT. Therefore, it would be advantageous for the application of oxide TFT, if it is possible to lower leakage current of high-k dielectric films with reduced dielectric/semiconductor interface-trap-

states. Such kind of TFT will not only improve on/off ratio of the device but also reduce the operating voltage of the device below 1.0 V.

High-k TiO_2 has chemical and thermodynamically stable interfaces with the silicon substrate.[214, 215] TiO_2 is a low-cost and non-toxic material. TiO_2 has drawn consideration on account of its scavenging properties.[216] This high dielectric constant usually occurs with a smaller band gap resulting in high leakage current through the gate dielectric. In comparison, Li_5AlO_4 has a wide band gap, low leakage current density, sufficient band offset and excellent thermal stability. On the other hand, high-k ion conducting Li_5AlO_4/IZO transistor exhibits high subthreshold swing and interfaces states as well as operating voltage. In Li_5AlO_4 dielectric Li^+ ion provide the high capacitance for TFT operation at 2V. The capacitance of dielectric Li_5AlO_4 thin film rapidly decreased with increasing frequency because of the ion mobility limits the polarization response time[55], which interferes with the operation of TFT in the high-frequency region. Thus to overcome this undesirable polarization delaying effect in Li_5AlO_4 a thin layer of TiO_2 was inserted through the solution process between the gate dielectric Li_5AlO_4 and a gate electrode. Comprehensively it is difficult to obtain the prime requirements (e.g., low subthreshold swing, minimum interface states and low voltage <1V) for the TFT at the low voltage with the single layer of the oxide gate dielectric. Therefore to accomplish these key requirements at low operating voltage <1 V, a combination of a gate dielectric with the TiO_2 and Li_5AlO_4 may be beneficial rather than using single-layer of a dielectric.

To reduce the semiconductor/dielectric interface-trap-states, charge carriers can be donated to the interface trap states from the gate dielectric itself. This carrier donation can fill the interface trap states partially, which is effectively capable of reducing the N_{max} of the

device. In that particular case, an additional gate voltage (V_G) is not required to fill those interface-trap-states that essentially can enhance the effective charge accumulation in the semiconductor channel. This mechanism can be realized by fabricating a bilayer stack dielectric of high-κ ion-conducting oxide with high-κ n-type semiconductor gate interface and has been presented in this chapter successfully. Specifically, for solution processed indium zinc oxide (IZO) TFT, stack layers of Li_5AlO_4 (ion-conducting dielectric) with TiO_2 gate interface has been used to establish the mechanism of this proposed device. The key advantage of using TiO_2 is its n-type semiconducting nature and high-κ value. Moreover, TiO_2 has ~1 eV band offset with respect to highly p-doped silicon (p^{++}-Si) gate electrode that has been used as a substrate for all TFT fabrications in this chapter. A TiO_2 thin film can not be used as a gate dielectric in our device due to its smaller band gap (3.3 eV) resulting in a high gate leakage current of the device. In contrast, high-κ Li_5AlO_4 has a wide optical band gap (5.8 eV) that can introduce very low leakage current density and has a much higher band offset with excellent thermal stability. The earlier report on Li_5AlO_4 dielectric based oxide TFT indicates that the subthreshold swing (SS) of the device is significantly high arising from the higher dielectric/semiconductor interfaces states.[114] As a consequence, Li_5AlO_4-only dielectric required 2 V operating voltage. Relatively, Li_5AlO_4/TiO_2 stacked dielectric exhibits lower subthreshold swing and interface states that enable us to fabricate 1.0 V (operating voltage) TFT with significantly improved carrier mobility and on/off ratio. For comparison, four TFTs were fabricated with Al_2O_3, Li_5AlO_4, Li_5AlO_4/TiO_2 and Li_5AlO_4/Al_2O_3 dielectric, respectively by keeping all other parameters same **figure 5.1**. Comparative electrical studies clearly indicate the role of electron

donation from TiO_2 gate interface layer to the semiconductor/dielectric interface-trap-state that reduces operating voltage to 1.0 V with a potential improvement of device parameters.

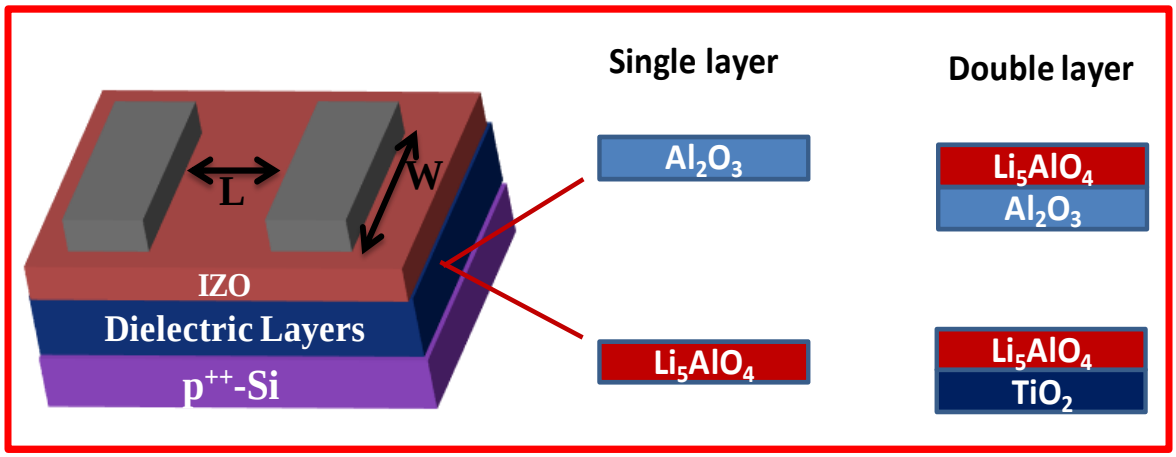

Figure 5.1: *Schematic diagram of the device structures for TFTs with single-layer (Al_2O_3 and Li_5AlO_4) and bilayer (Li_5AlO_4/ TiO_2 and Li_5AlO_4/ Al_2O_3) gate dielectrics.*

5.2 Results and discussion

5.2.1 Grazing incidence X-ray diffraction (GIXRD) study and X-ray reflectivity (XRR) of dielectric thin films

To investigate the structural properties of the spin-coated dielectrics thin film, grazing incidence X-ray diffraction (GIXRD) were carried out for both the single and bilayer stacked dielectrics as shown in **figure 5.2 a)**. Single layer 500 ^oC annealed Al_2O_3 dielectric shows the amorphous nature whereas, 500 ^oC annealed TiO_2 and Li_5AlO_4 show crystallization nature. This is consistent with an earlier report on where it has shown that Al_2O_3 required ~900 ^oC to form a crystalline thin film.[174] The GIXRD data of Li_5AlO_4 thin film shows the diffraction peak position at 30.6^o, 35.6^o and 51.1^o which are responsible for the reflection planes of (220), (222) and (413) respectively of the α phase Li_5AlO_4.[114] The single layer of TiO_2 thin film shows one intense peak at ~25.2^o,

represented (101) plane of the anatase phase of TiO_2.[197] The Li_5AlO_4/Al_2O_3 and Li_5AlO_4/TiO_2 bilayer stacked dielectrics exhibited the same set of reflection planes of α-Li_5AlO_4 that has observed in single layer Li_5AlO_4 thin film. For ion-conducting dielectric, such kind of crystalline phase is required to get the advantages of ionic polarization that is responsible for the higher dielectric constant of the gate insulator. Again, the high-κthe dielectric thin film is capable of fabricating low operating voltage TFT. X-ray reflectivity (XRR) measurement has been done to determine the thickness of the stacked dielectric. XRR analysis of Li_5AlO_4/ TiO_2 bilayer dielectric thin film is shown in **figure 5.2 b).** The experimental data were fitted with the Parrot-32 software basis of parrot formalism. The extracted thickness of Li_5AlO_4 and TiO_2 thin film are ~ 60 nm and 10 nm respectively.

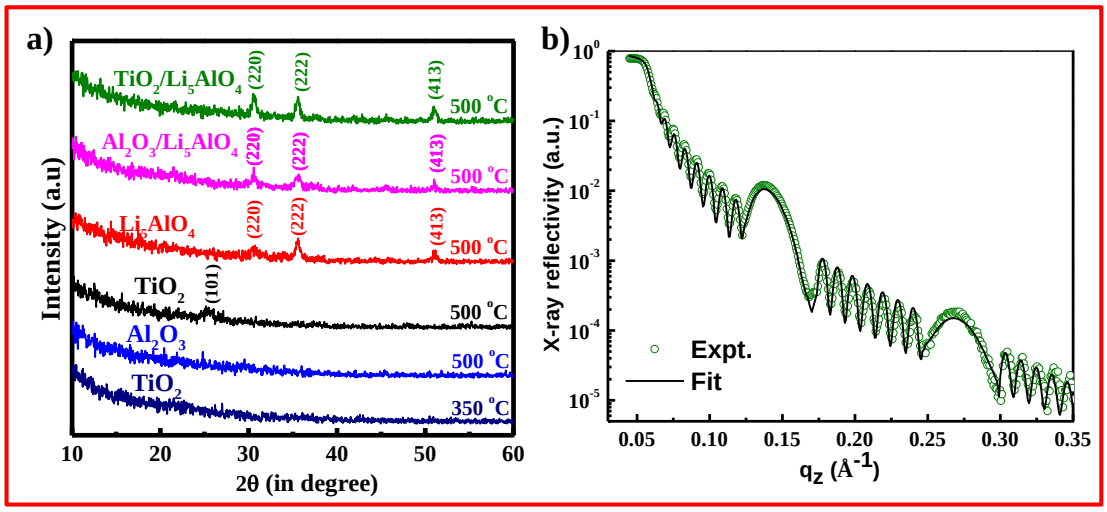

Figure 5.2: a) *Grazing incidence X-ray diffraction (GIXRD) pattern of sol-gel coated thin films of single layer and bilayer dielectrics* ***b)*** *X-ray reflectivity data and theoretical fit as a function of q_z of Li_5AlO_4/TiO_2 stacked dielectric.*

5.2.2 Surface morphology

The surface morphologies of different single or bilayer dielectric thin films have been studied by atomic force microscopy (AFM) and micrograph of different dielectric has been

shown in **figure 5.3**. All these thin films have been deposited on p^{++}-Si (111) wafer exactly under the same condition of TFT fabrication.

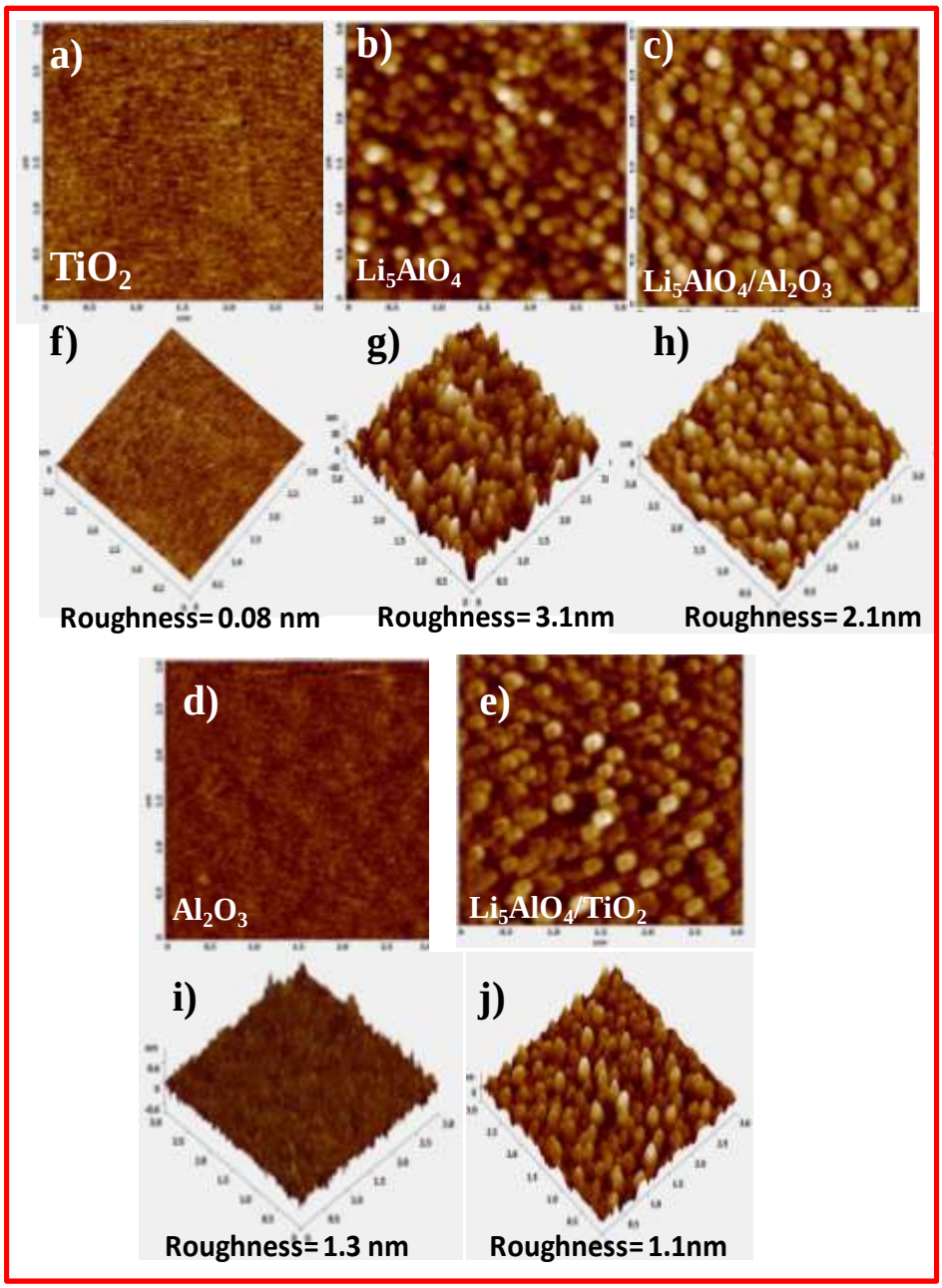

Figure 5.3: *2D-Surface morphologies of spin-coated thin films of various single layer and bilayer dielectrics* ***a)*** *TiO_2,* ***b)*** *Li_5AlO_4,* ***c)*** *Li_5AlO_4/ Al_2O_3,* ***d)*** *Al_2O_3,* ***e)*** *Li_5AlO_4/ TiO_2 and 3D-AFM images of* ***f)*** *TiO_2 (R_{rms} =0.08 nm),* ***g)*** *Li_5AlO_4 (R_{rms} =3.1 nm),* ***h)*** *Li_5AlO_4/Al_2O_3 (R_{rms} =2.3 nm),* ***i)*** *Al_2O_3 (R_{rms} = 1.3)* ***j)*** *Li_5AlO_4/ TiO_2 (R_{rms}=1.1 nm).*

The study indicates that the deposited TiO_2 thin film is mostly in the amorphous phase with a root mean square (RMS) roughness of 0.08 nm which is around 40 times lower than that of Li_5AlO_4 thin films (3.1 nm) and 16 times lower than that of Al_2O_3 thin film (1.3 nm) as shown in **figure 5.3 a), b) and d).** The smooth surface of the TiO_2 thin films on p^{++}-Si substrate indicates the existence of a good interface between p^{++}-Si and TiO_2 layer. In a combination of good interface and band alignment of TiO_2/p^{++}-Si heterojunction, it is possible to transfer charge carrier through TiO_2/p^{++}-Si interface efficiently without significant charge trapping which has been observed in earlier studies for photocatalytic effect.[217] The roughness of Li_5AlO_4 film (same thickness) with underlying Al_2O_3 and TiO_2 thin film are 2.1 nm **(figure 5.3 c)** and 1.1 nm **(figure 5.3 e)** respectively, which are smoother than single layer Li_5AlO_4 film implying the difference nature in crystal growth of Li_5AlO_4 on p^{++}-Si (111) from amorphous TiO_2 and Al_2O_3 substrate. This Li_5AlO_4/TiO_2 stacked dielectric with lower roughness is capable of offering low interface trap states in the semiconductor/dielectric interface, which can reduce the subthreshold swing of the device significantly. Additionally, dielectric with lower roughness reduces carrier scattering that can improve the effective carrier mobility of the device. Therefore, Li_5AlO_4/TiO_2 stacked dielectric with lower roughness can be beneficial for the fabrication of high performance low operating voltage TFT.

5.2.3 Dielectric and electrical characterizations

To measure the leakage current density and capacitance of various gate dielectric thin films, devices were fabricated with the geometry of p^{++}-Si/dielectric/Al. **Figure 5.4 a)** shows the leakage current density vs. applied voltage data for different dielectric thin films. It is obvious from the figure that Li_5AlO_4/TiO_2 thin film shows the least leakage current

density of 1.0 μA/cm^2 at 30 V. The leakage current density of the device with Al_2O_3 and Li_5AlO_4/ Al_2O_3 thin films are very close and slightly higher than that of the Li_5AlO_4/TiO_2 thin film. However, the leakage current density of Li_5AlO_4 only devices is quite higher compared to the devices with other dielectrics.

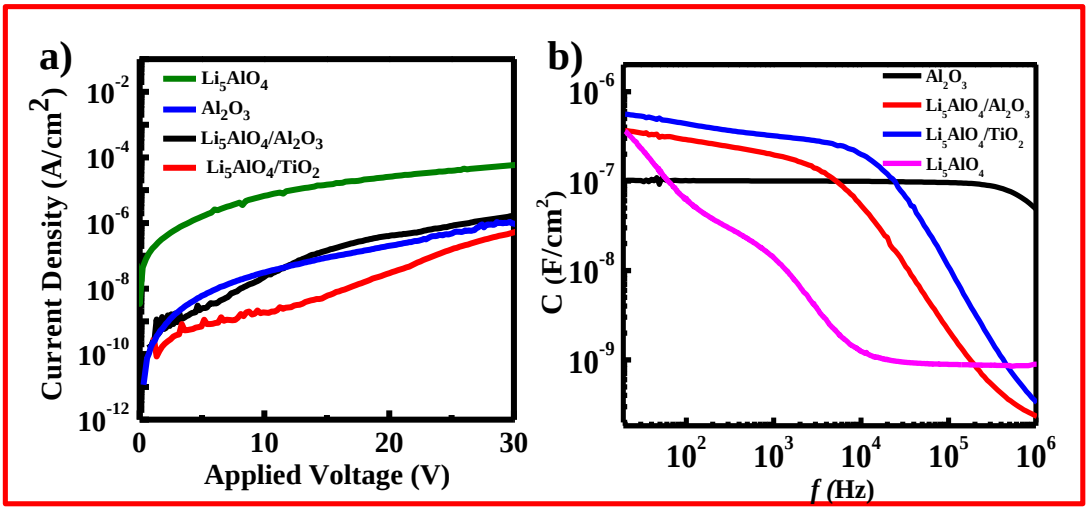

Figure 5.4: a) *Leakage current density vs applied voltage and* ***b)*** *capacitance vs frequency curve of sol-gel derived thin films of various single (Al_2O_3 and Li_5AlO_4) and double gate dielectric (Li_5AlO_4/TiO_2 and Li_5AlO_4/Al_2O_3) layers with MIM device architecture.*

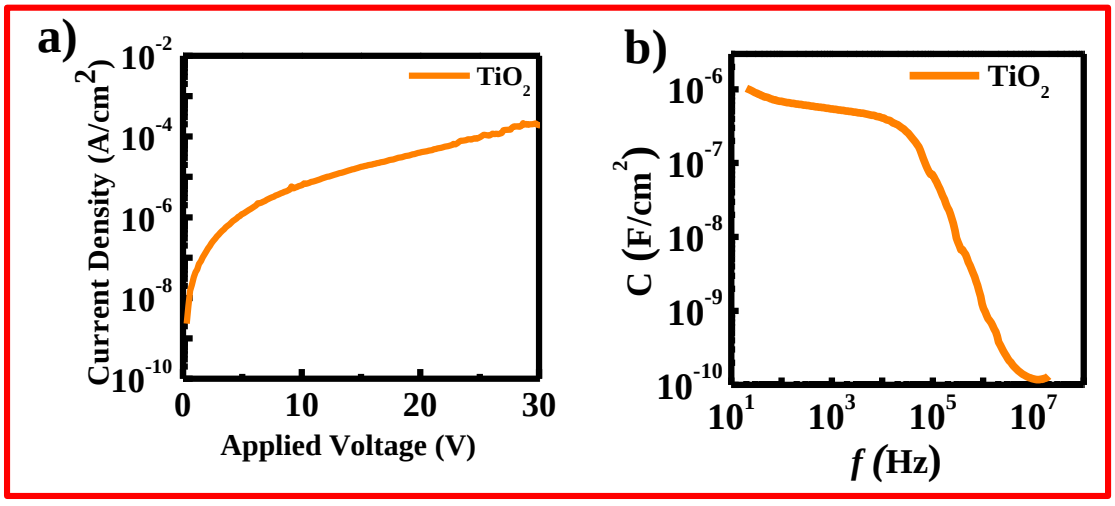

Figure 5.5: a) *Leakage current density vs applied voltage and* ***b)*** *capacitance vs frequency curve of sol-gel derived TiO_2 thin film.*

These differences are mainly due to the surface roughness and film packing of the different dielectric thin films. As shown in AFM studies of different thin films, Li_5AlO_4 thin film sample has the highest surface roughness. Additionally, multilayered dielectric always reduces gate leakage, mainly due to the lattice mismatch of two different materials with different grain shapes at the interfaces, which is well understood from earlier multilayered dielectric studies.[218] For comparison, we have investigated the leakage current density of TiO_2 only thin film, which is 0.1mA/cm^2 at 30 V as shown separately in **figure 5.5 a)**. Such a high leakage current density originated from the lower band gap (3.3 eV) of TiO_2 makes it inappropriate as a gate dielectric of TFT. These comprehensive electrical and AFM studies suggest that the leakage current density of bilayer Li_5AlO_4/TiO_2 stacked dielectric (device-4) is not only extremely low but also reduces surface roughness, that may be responsible for the higher drain current (I_D) with low subthreshold swing and interface states.

In addition to leakage current density study, the same sets of devices were used to investigate the dielectric properties of different gate insulators. The variation of capacitances per unit area at different frequencies is shown in **figure 5.4 b).** Commonly, the capacitance decreases with increasing frequency, which is known as the dispersion behavior of the dielectric. The capacitance of Al_2O_3 thin film is practically frequency independent up to 10^6 Hz. Similar to Al_2O_3, the areal capacitance of the TiO_2 layer is shown in **figure 5.5 b)** which is nearly constant up to the frequency 10^5 Hz. In the case of TiO_2 and Al_2O_3 dielectric layers, as the frequency increases from 20 Hz to 10^5 Hz, the areal capacitance decreases slightly from 550 nF/cm^2 to 390 nF/cm^2 and 100 nF/cm^2 to 90 nF/cm^2 respectively. However, the capacitances of Li_5AlO_4 dielectric changes rapidly with

frequency **figure 5.4 b)** which is due to the lack of accumulation of interface Li^+ at a higher frequency. Interestingly, with bilayer (Li_5AlO_4/Al_2O_3 and Li_5AlO_4/TiO_2) device structure, the variation of capacitance with frequency is between that of Al_2O_3 and Li_5AlO_4 thin films indicate the significant improvement in the dielectric dispersion behavior of bilayer dielectrics. Moreover, the capacitance of the bilayer Li_5AlO_4/TiO_2 dielectric thin film is effectively higher than that of Li_5AlO_4/Al_2O_3 bilayer because of the higher dielectric constant of TiO_2 than Al_2O_3 ($1/k = 1/k_{TiO_2} + 1/k_{Li_5AlO_4}$) and the single layer of Li_5AlO_4. The areal capacitance of different dielectric thin films at the frequency of 50 Hz is 100 nF/cm^2, 330 nF/cm^2, 300 nF/cm^2 and 550 nF/cm^2 for Al_2O_3, Li_5AlO_4, Li_5AlO_4/Al_2O_3, and Li_5AlO_4/TiO_2 thin films respectively that have been chosen for mobility calculation of TFTs. The lower frequency region has been chosen for the calculation to neglect the overestimation of mobility.[174] Thereto the capacitance variation at the low frequency of the dielectric layers is commonly linked to well known Maxwell-Wagner and Keer effect space charge polarization which is an implicit a non-uniform charge accumulation.[219] [220] Ganon et.al. suggested that these effects are also related to electrode polarization where the mobile charges generate an EDL against the electrodes resulting in a high EDL capacitance.[221] Li^+ ions are positively charged and mobile in the intermixing layer of bilayer TiO_2/Li_5AlO_4. Li^+ ion will have sufficient time to respond to the applied bias and go back and forth in the vicinity of the space charge layer under the low-frequency AC bias. This can be observed as a macroscopic dipole with oscillating with the field. The distance of oscillations increases when the frequency is decreased and finally the larger the capacitance density.

5.3 Transistor characterization of single and bilayer dielectric TFTs

To study the effect of different gate interface on the device performance, four sets of TFTs have been fabricated in a bottom gate, top contact (BG-TC) architecture as shown in **figure 5.6.** The devices with Al_2O_3, Li_5AlO_4, Li_5AlO_4/ Al_2O_3 and Li_5AlO_4/TiO_2 dielectric were named as device-1, device-2, device-3 and device-4 respectively. Out of these four devices, device-2 is the reference device with Li_5AlO_4 gate dielectric whereas device-3 and device-4 are with Li_5AlO_4/Al_2O_3 and Li_5AlO_4/TiO_2 bilayer stacked dielectrics respectively.

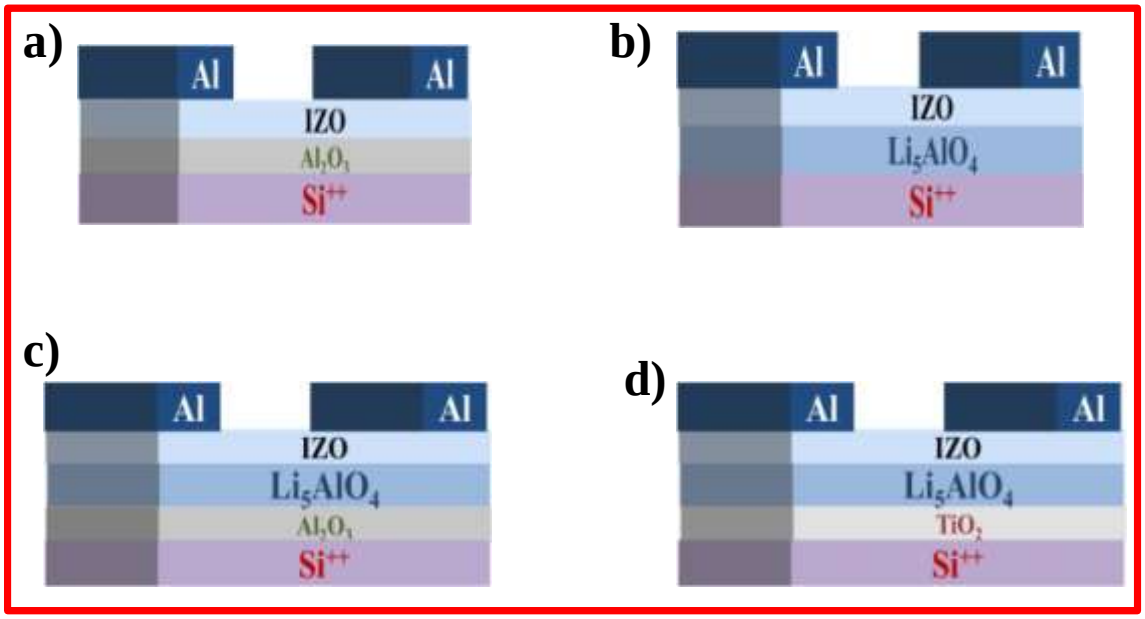

Figure 5.6: *Schematic device structure for IZO TFT with* ***a)*** *device-1;* Al_2O_3 ***b)*** *device-2;* Li_5AlO_4 *single dielectric layer* ***c)*** *device-3;* Li_5AlO_4/ Al_2O_3 ***d)*** *device-4;* Li_5AlO_4/ TiO_2 *bilayer.*

All these TFTs have the same width to channel length ratio of 118 (W/L = 23.6 mm/0.2 mm). To avoid the overestimation of carrier mobility (μ) due to grain boundary effect, which is highly dominating below 25 μm channel width with a W/L ratio less than 10, the channel width (200 μm) of all TFTs has been chosen sufficiently higher with high W/L

ratio (118).[222] [210] Moreover, high-performance TFT with larger device area demands a good quality of dielectric thin film with pinhole free uniform thin film and very fewer defect states. **Figure 5.7 - 5.10** shows the two sets of output and transfer characteristics of IZO TFTs to study the capability of these all TFTs in the operating voltage range of 1.0 V and 2.0 V respectively for the device 1, device 2, device 3 and device 4.

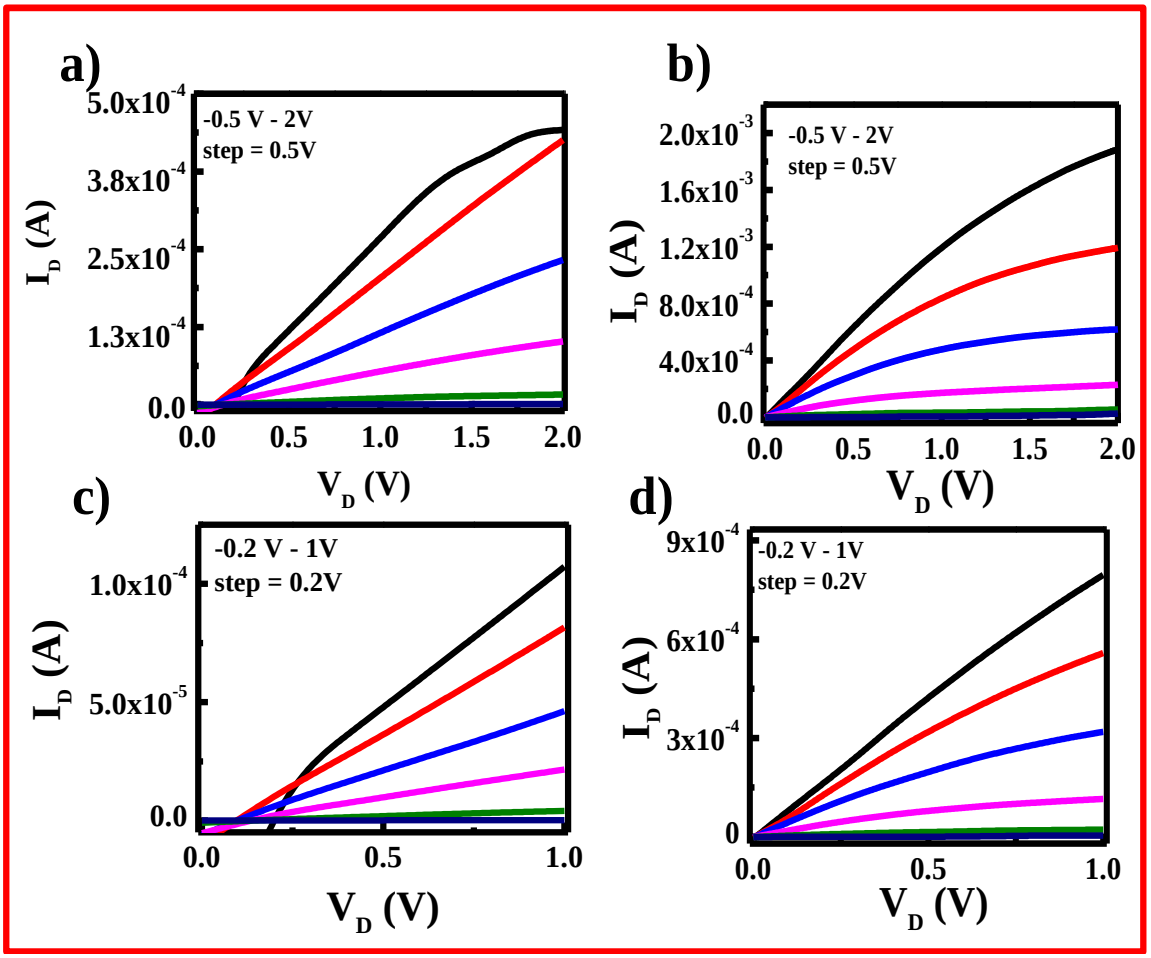

Figure 5.7: *Transistor characterization of single-layer gate dielectric IZO TFT under the different bias; output characteristics of* ***a)*** *device-1* ***b)*** *device-2 under 2.0 V operation* ***c)*** *device-1 and* ***d)*** *device-2 under 1.0 V.*

To study 1.0 V TFTs output characteristics, drain voltage (V_D) was swept from 0 V to 1.0 V with the gate voltage (V_G) varying from -0.2 V to 1.0 V whereas, for 2.0 V TFT, these drain and gate voltage ranges were 0.0-2.0 V and -0.5 -2.0 respectively. To study 1.0 V TFTs transfer characteristics, V_G was varied from -1.0 to 1.0 V with a V_D of 1.0 V. Similarly, V_G was varied from -2.0 to 2.0 V with a V_D of 2.0 V for 2.0 V TFTs transfer characteristics as shown in **figure 5.8** and **figure 5.10**.

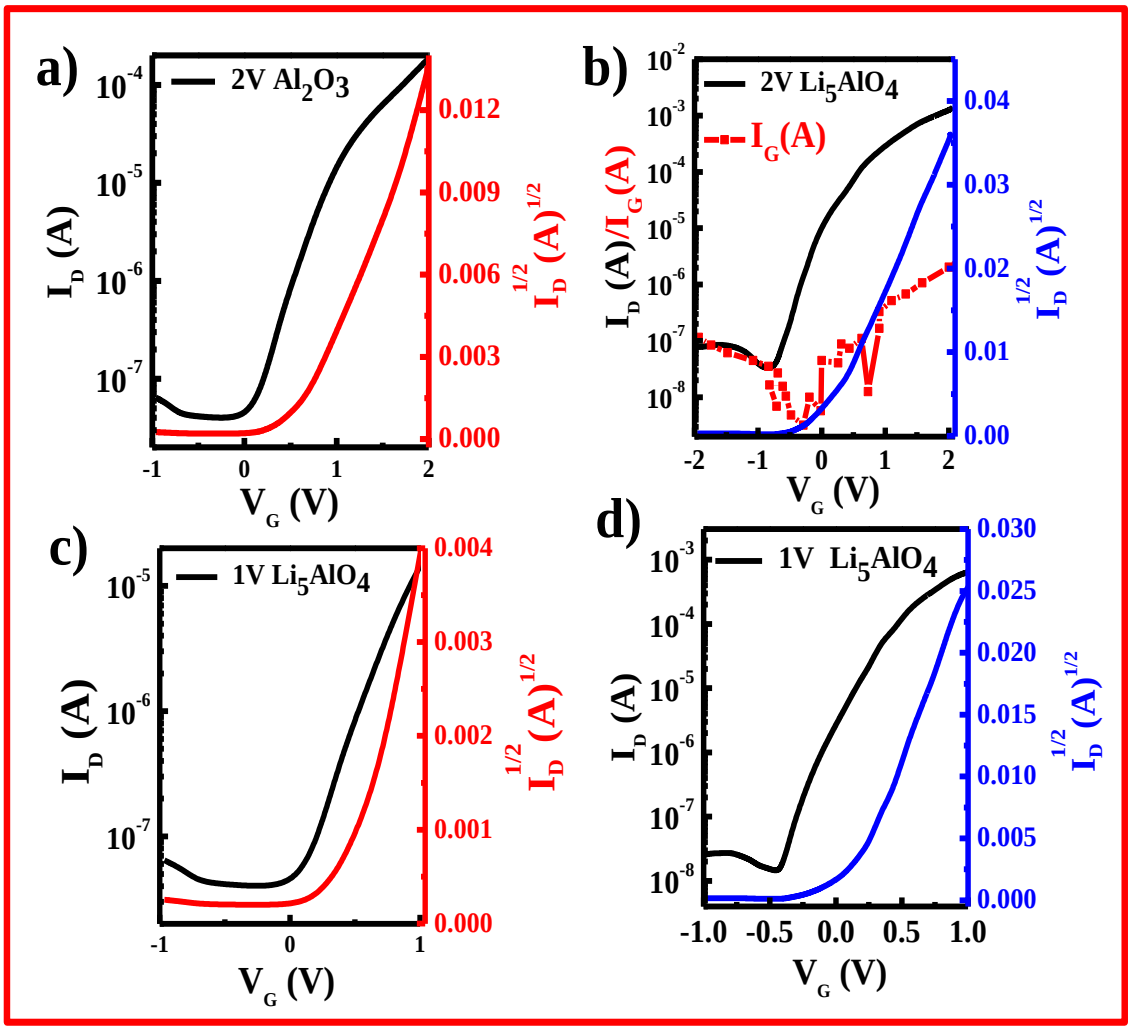

Figure 5.8: *Transistor characterization of single-layer gate dielectric IZO TFT under the different bias; transfer characteristics of* ***a)*** *device-1* ***b)*** *device-2 under 2.0 V operation* ***c)*** *device-1 and* ***d)*** *device-2 under 1.0 V.*

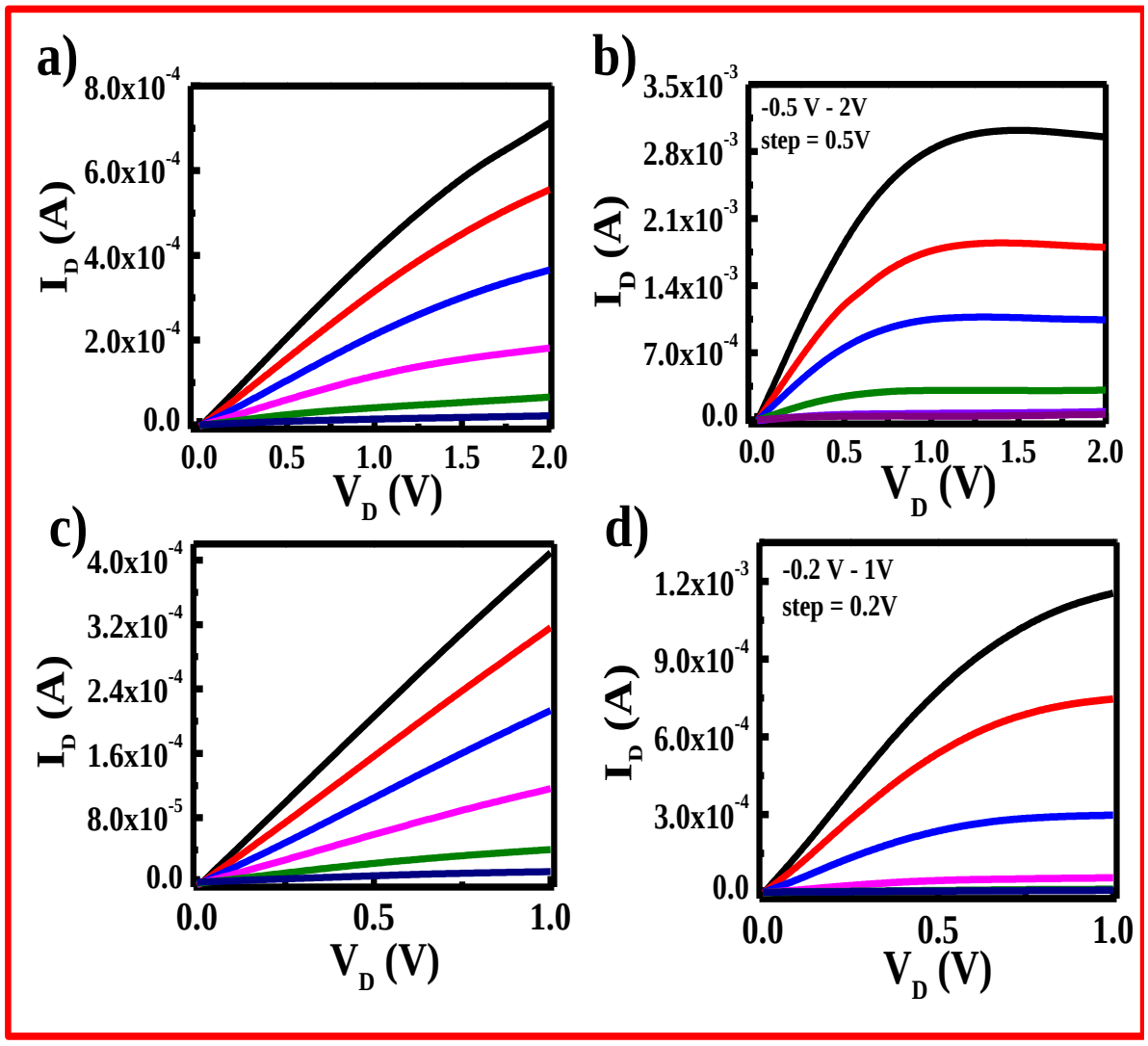

Figure 5.9: *Transistor characterization of bilayer gate dielectric IZO TFT under the different bias; output characteristics of* ***a)*** *device-3* ***b)*** *device-4 under 2.0 V operation* ***c)*** *device-3 and* ***d)*** *device-4 under 1.0 V.*

From these comparative studies, it has been observed that under 2.0 V operation, device-4 shows a clear linear and saturation region **(figure 5. 9 b) and d))** with clear pinch-off and good current saturation at 3 x 10^{-3} A (with V_G=2 V), whereas device-3 (**figure 5.9 a) and c))** and device-1 **(figure 5.7 a) and c))** shows mostly the linear region in this 2.0 V range. The reference device (device-2) with single layer Li_5AlO_4 shows some tendency of current

saturation within this 2.0 V range. Again, only device-4 shows current saturation in 1.0 V operating range. Three other devices (device-1,2 and 3) show a linear region only. This comprehensive study clearly shows that only device-4 shows good TFT behavior within the 1.0 V operating voltage with current saturation. Comparing to these devices, Al_2O_3 only dielectric doesn't show any current saturation neither in 1.0 V nor in 2.0 V operating voltage as depicted in **figure 5.7 a) and c).**

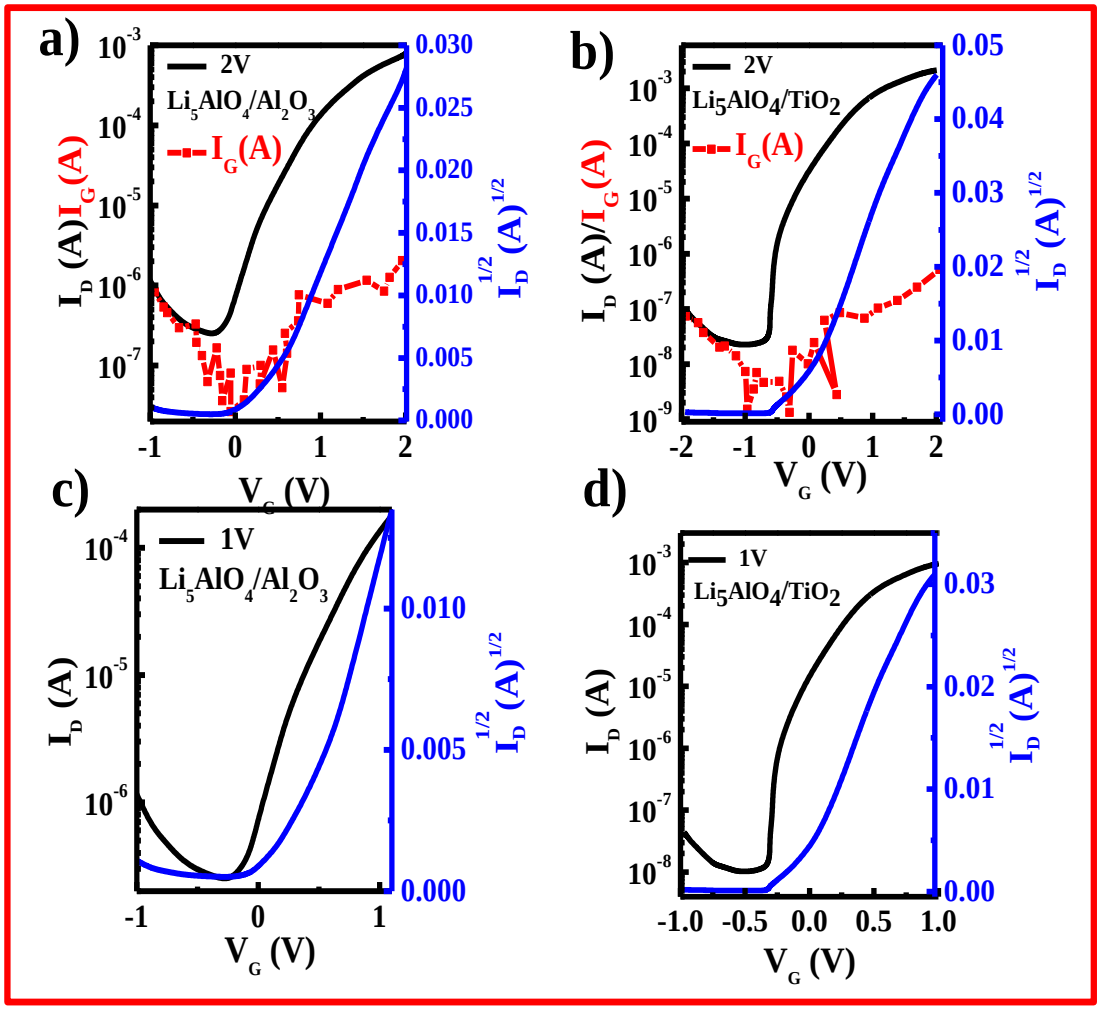

Figure 5.10:*Transistor characterization of bilayer gate dielectric IZO TFT under the different bias; transfer characteristics* ***a)*** *device-3* ***b)*** *device-4 under 2.0 V operation;* ***c)*** *device-3* ***d)*** *device-4 under 1.0 V operation.*

Effective carrier mobility (μ), sub-threshold swing (SS) and interface states of these TFTs are calculated from the following equations respectively,

$$\mathbf{I_D = \mu C \frac{W}{2L}(V_G - V_T)^2} \quad \text{.....} \quad \mathbf{(5.1)}$$

$$SS = \left[\frac{d(log\, I_D)}{dV_G}\right]^{-1} \quad \text{.....} \quad \mathbf{(5.2)}$$

$$\mathbf{N_{SS}^{max} = \left[\frac{SS \times \log e}{kT/q} - 1\right]\frac{C}{q}} \quad \text{.....} \quad \mathbf{(5.3)}$$

Where I_D, C, V_G, V_T, SS, k and q are saturation drain current, capacitance per unit area, gate voltage, threshold voltage, subthreshold swing, Boltzmann constant and electronic charge of electron respectively.

The extracted carrier mobility, on/off ratio, and subthreshold swings from the transfer curve **figure 5.8 and 5.10** are listed in **table 5.1**. The threshold voltage of the device has been determined by extrapolating the straight line of $I_{DS}^{1/2}$ versus V_G curve. Among the four different TFTs, device-4 shows the highest electron mobility with a value of 32 $cm^2/V.s$ whereas the electron mobility of device-1, 2, and 3 are 4.0 $cm^2/V.s$, 18.0 $cm^2/V.s$, and 10.0 $cm^2/V.s$ respectively. In addition to electron mobility, device-4 also shows comparatively the highest on/off ratio of 5×10^5 with a minimum subthreshold swing of 110 mV/dec. Therefore, device-4 among the four devices shows the best device performance with the highest electron mobility and on/off ratio with least SS value in both the operating voltage ranges of 1.0 V and 2.0 V. The extracted carrier mobility, on/off ratio and subthreshold swings of all the four devices are listed in **table 5.1.**

Table 5.1: *Summarized data of the electrical characterizations of single and bilayer dielectric IZO TFT*

Device no.	Dielectric	C (nF/cm^2) at 50 Hz	V_{Th} (V)	ON/OFF ratio	Density of interfaces sates (N_{ss}^{max}) (in cm^{-2})	Subthreshold swing (SS) (mV/decade)	Electron Mobility (μ) ($cm^2\ V^{-1}\ sec^{-1}$)
1.	Al_2O_3	100	0.25	5×10^2	$\sim 10^{13}$	320	4
2.	Li_5AlO_4	330	-0.1	3×10^4	8×10^{12}	290	18
3.	Li_5AlO_4/Al_2O_3	310	-0.2	4×10^3	9.5×10^{12}	315	10
4.	Li_5AlO_4/TiO_2	550	0.0	5×10^5	1.1×10^{12}	110	32

This distinguishable higher performance of device-4 is mainly due to two reasons. One of them is the smoother surface morphology of Li_5AlO_4/TiO_2 compared to other combinations, that has been confirmed from AFM studies and discussed in the earlier section. This smoother surface helps in achieving fewer surface states in the semiconductor-dielectric interface, which has been realized from the least SS value of device-4. The extracted interface state density (N_{ss}^{max}) is $1.1 \times 10^{12}/cm^2$ which is around one order lower than the other three different types of TFT **(table-5.1).** Smoother surface and lower N_{ss}^{max} lead to the less scattering and trapping of charge carriers in the dielectric/semiconductor interface resulting in improvement of effective mobility and higher drain current (I_D) of the device.[198] The second reason is the electron donation from TiO_2 gate interface which is more dominating in our study. This phenomenon can be realized from **figure 5.11** that indicates p^{++}-Si (111)/TiO_2 interface works as Schottky junction.[223, 224] Under zero bias, electron transfer to p^{++}-Si leaving TiO_2 as positively charge layer that induces electron of IZO film to accumulate in Li_5AlO_4/IZO interface

which effectively donates electrons to the dielectric-semiconductor interface trap state from the dielectric of device-4 **figure 5.11 a).** Under forward bias, TiO_2 film accumulates more positive charge and extra electrons mostly accumulate in the channel and give high drain current under accumulation mode operation **figure 5.11**. Thus, TiO_2 film effectively reduces the effective trap states and improves in device performance as realized from the comparative study of device-3 and device-4.[225] The difference between these two devices is the gate interface that is Al_2O_3 and TiO_2, respectively. As we know, Al_2O_3 is a very good electrical insulator with extremely low electron carriers. In contrast, TiO_2 is an n-type semiconductor and is commonly used as an electron transport layer in many electronic devices including solar cells and light emitting diodes. Therefore, due to the heterojunction formation by p^{++}-Si (111)/TiO_2 interface, a significant number of electrons get transferred to p^{++}-Si (111) under zero gate bias leaving TiO_2 layer as positively charged **(figure 5.12 d)**. However, such kind of charge transfer is not possible for device-3 due to the insulating nature of Al_2O_3 **(figure 5.12 c)**. Again, positively charged TiO_2 repels Li^+ at the Li_5AlO_4/TiO_2 interface resulting in the accumulation of Li^+ at the other side of Li_5AlO_4 thin film, i.e., in Li_5AlO_4/IZO interface. This Li^+ accumulation under zero gate bias induces electron carriers of IZO film to get accumulated at the Li_5AlO_4/IZO interface and fills interface trap states partially. This phenomenon reduces N_{ss}^{max} considerably which, in turn, reduces the SS value of the device and enables to achieve the lower operating voltage of the device to 1.0 V.

For better understanding, a schematic diagram of the energy-band of different IZO TFT is illustrated in **figure 5.12**. Comparing to device-1 (Al_2O_3 dielectric) and device-2 (Li_5AlO_4

dielectric), the earlier TFT has a lower surface roughness of the dielectric than that of the latter. However, the SS value of device-2 is significantly lower than that of device-1.

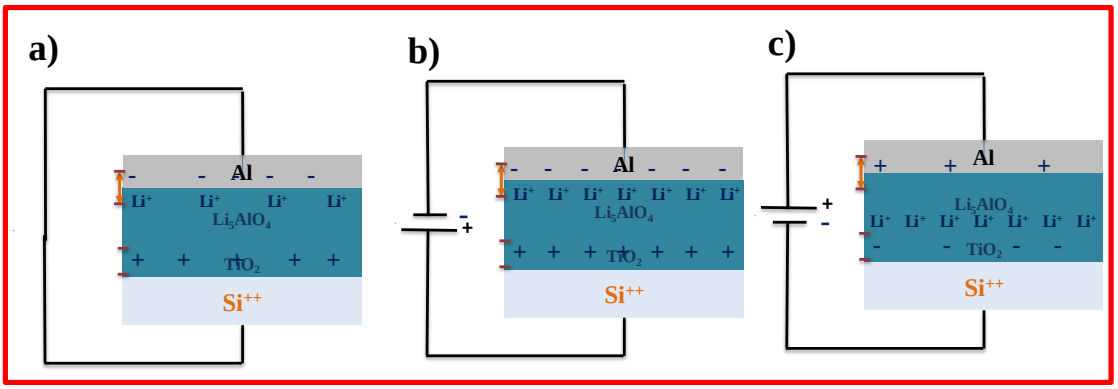

Figure 5.11: *Schematic presentation of the bilayer dielectric layer of p^+-Si/TiO_2 Schottky junction under* ***a)*** *zero bias* ***b)*** *forward bias,* ***c)*** *reversed bias.*

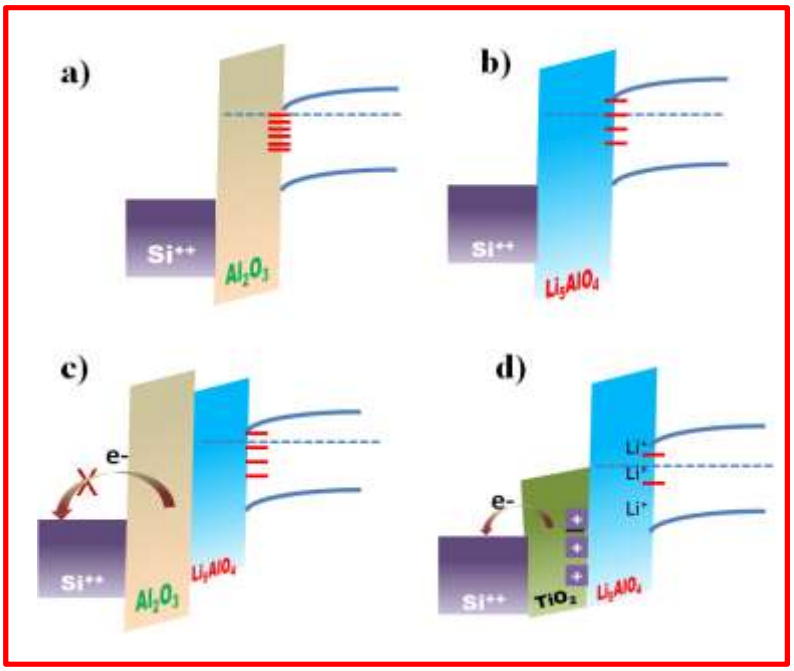

Figure 5.12: *Depiction of metal-insulator/semiconductor structures illustrating the mechanism of variation in the transistor performance using various gate dielectrics. Energy band diagram of the* ***a)*** *a single layer of insulator Al_2O_3 dielectric* ***b)*** *single layer of Li_5AlO_4 dielectric* ***c)*** *Li_5AlO_4/Al_2O_3 bilayer dielectric and* ***d)*** *Li_5AlO_4/TiO_2 bilayer dielectric.*

This is because of the acceptor-like trap sites in the IZO/Al_2O_3 interface of device-1 as depicted in **figure 5.12 a),** which results in a relatively poor SS, higher N_{ss}^{max} and very low field-effect mobility **(Table-5.1).**[174],[225] Mobile Li^+ ions are abundant in the Li_5AlO_4 dielectric thin film of device-2. Under the applied positive gate bias (V_G>0) condition, these Li^+ ions are rearranged towards the Li_5AlO_4/IZO interface attracting more electrons in the IZO active layer. Consequently, the device-2 exhibits much higher field effect mobility. However, it shows quite poor SS which is due to the larger number of interface states because of the Li^+ ion displacements.[226] Among all devices, device-4 (with Li_5AlO_4/TiO_2 dielectric) shows least SS and N_{ss}^{max} value compared to the device-2 (Li_5AlO_4 dielectric) and 3 (Li_5AlO_4/Al_2O_3 dielectric), while the dielectric/semiconductor interface was not altered in all three devices. This indicates that the observed SS and interface states are not merely the contribution of the dielectric surface roughness, but also a secondary effect that may control the electron traps behavior. Since p^{++}-Si (111)/TiO_2 interface forms a Schottky junction at zero gate bias, the electron of the TiO_2 layer transferred to the p^{++}-Si gate electrode creates a depleted layer of positive charge at TiO_2 thin film. Although, a hole is not allowed to transfer to TiO_2 layer due to a large potential barrier in p^{++}-Si (111)/TiO_2 interface.[223, 224] In the same time, this junction form a high barrier for a hole to cross from the p^{++}-Si side. Therefore, this layer of the positive charge of TiO_2 thin film induces electrons of the IZO layer to accumulates at the Li_5AlO_4/IZO interface, which initially fills the electron trap states at the gate/dielectric interface **(figure 5.12 d))**. Since this phenomenon is happening under zero gate bias, therefore, this TiO_2 thin film is effectively reducing the interface state density (N_{ss}^{max}) of TFT resulting in a reduced SS value of the device. However, this phenomenon does not occur in device-3 due to the

insulating nature of the Al_2O_3 layer **(figure 5.12c))**. In accumulation mode operation, a positive voltage is applied to the gate with respect to the drain electrode to all the devices. However, this bias doesn't change the depletion layer width of p^{++}-Si (111)/TiO_2 interface of device-4 due to the intermediate insulating Li_5AlO_4 layer. This phenomenon effectively accumulates more mobile carriers in the channel of device-4 that enhances the device performance over other devices. Additionally, due to least SS value, device-4 also shows a perfect 1.0 V operating voltage by maintaining high carrier mobility. Moreover, the depletion layer of p^{++}-Si (111)/TiO_2 interface also helps to achieve the least gate leakage current among four devices.

5.4 Conclusions

In summary of this chapter, high-performance solution-processed one-volt indium zinc oxide thin film transistor (TFT) has been fabricated onto sol-gel derived ion-conduction gate dielectric by utilizing electron donating TiO_2 gate interface. A comparative device characterization of two different TFTs with TiO_2, Al_2O_3 gate interface reveals that n-type TiO_2 works as an electron donor to the semiconductor/dielectric interface trap state that essentially reduces the subthreshold swing of the device. Moreover, the depletion layer of p^{++}-Si (111)/TiO_2 interface reduces gate leakage current significantly that helps to improve the on/off ratio of the device. Specifically, by inserting a high-k TiO_2 layer between the Li_5AlO_4 gate dielectric and the gate electrode, a high capacitance of the dielectric film has been achieved that also helps to get current saturation at lower gate bias. Comparing four TFTs with Al_2O_3, Li_5AlO_4, Li_5AlO_4/Al_2O_3 and Li_5AlO_4/TiO_2 dielectric, device with Li_5AlO_4/TiO_2 dielectric exhibited the best performance with electron mobility of 32 cm^2/V.s, on/off ratio of 5×10^5, and sub-threshold swing of 110 mV/dec. This investigation

suggests a new direction for the development of high-performance, low voltage TFT fabrication by selecting proper material combinations for gate dielectrics.