Chapter 2

Effect of Source Pocket Engineering on the Device Level Performance of GaSb/Si Heterojunction Vertical TFET

2.1 Introduction

The tunnel field effect transistors (TFETs), also known as "Green Transistors" [60], have gained enormous interests for low power digital VLSI applications due to their extremely low OFF-state current, low power dissipation, and the lowest possible subthreshold swing (SS) even below the Boltzmann limit of 60 mV/decade over the conventional MOS transistors [43],[51],[53],[59],[61],[81],[114],[145] as discussed in Chapter-1. However, improvement of the ON-current and reduction of the ambipolar current conduction are still a challenge for applications of TFETs in different digital circuits like inverter, SRAM, DRAM etc. [63],[65],[82],[89],[106],[107],[143]. The literature survey of Chapter-1 shows that researchers have explored the heterojunction engineering techniques by using a narrow-bandgap material in place of Silicon (Si) in the source region of conventional TFET to enhance the driving current (ON-current) and to lower subthreshold slope (SS) as well as to minimize the ambipolar conduction effect [59],[79],[85],[100],[103],[109],[113],[117],[126],[135],146],[154],[158]. In such heterojunction TFETs, the drain current is increased due to the increase in the band-to-band tunnelling (BTBT) probability at the source/channel hetero-tunnel junction of the device. The commonly used low band gap materials are Ge and InAs and InGaAs to form a source/channel heterojunction in the TFETs [100],[111],[113]. Although Ge is the most widely used material for better lattice matching with the Si, the III-V direct band gap material InAs has been also used in heterojunction in TFET to enhance its

ON-current significantly [100],[134]. However, the major drawback of the InAs/Si based heterojunction TFET is its higher OFF-state current which may restrict its use for low-power VLSI applications [89]. Recently GaSb/Si heterojunction has been experimentally validated for different electronic applications [134],[147],[156]. In view of the above, the GaSb/Si heterojunction has been explored for the source/channel junction of the TFETs for the first time in the present thesis.

The literature survey of Chapter-1 shows that the source pocket engineering (i.e., use of a very thin heavily doped pocket region sandwiched between the source and channel) in the conventional TFET structures can play a significant role in controlling driving current (ON-current), subthreshold swing (SS) and reliability of the device [61],[78],[83],[84],[95],[100],[110]. It is also discussed in Chapter-1 that the vertically grown TFET (VTFET) has improved performance parameters over its lateral structure due to its very sharp dopant profile [83], good electrostatic control of the gate over channel region [81],[105], observation of NDR effects at room temperature and reduction of off-state reverse biased p++/i/n+ leakage [66],[74],[136] and comparatively easier in fabrication [65],[81],[145]. The VTFET has better integration density, low leakage current and less trapping related issues [136].

In view of the above discussions, the present chapter aims to investigate the DC and RF performance parameters of a source pocket engineered GaSb/Si heterojunction VTFET considering Al_2O_3 as gate-oxide in place of SiO_2 to enhance its ON-current [74]. The SILVACO ATLAS^{TM} 3D TCAD tool has been used to simulate the proposed Al_2O_3 gate-oxide based GaSb/Si heterojunction VTFETs with and without using a source pocket. All the major electrical performance parameters such as ON-current, threshold voltage, SS, OFF-state current, transconductance (g_m), output conductance (g_d), gate to drain capacitance (C_{gd}), gate to source capacitance (C_{gs}), cut-off frequency

(f_T), gain bandwidth product (GBP), maximum frequency of oscillation (f_{max}), transit time (τ), transconductance generation factor (TGF) and transconductance frequency product (TFP) have been analysed in this chapter. The performance parameters of the proposed VTFET have also been compared to its all-Si VTFET counterpart to investigate the superiority of the proposed device. The layout of the present Chapter is given as follows:

Section 2.2 deals with the TCAD simulation framework of the proposed VTFET using the SILVACO ATLAS^{TM} 3D TCAD tool along with fabrication steps to realize the proposed structure. Some important results and related discussions have been presented in Section 2.3. In Section 2.4, device-level performance comparison has been made for source pocket engineered GaSb/Si heterojunction vertical TFET (SPE GaSb/Si HJ VTFET) with vertically grown source pocket engineered all-Si TFET (SPE All-Si VTFET). Finally, Sec. 2.5 includes the summary and conclusion of the present chapter.

2.2 TCAD Simulation Framework

The schematic structure of the proposed TFET and its various parameters used for the TCAD simulation study are discussed. Possible fabrication feasibility of the proposed device structure is also discussed. Different models used in the TCAD simulation are briefly discussed in this section.

2.2.1 Proposed Vertical TFET Architectural Specifications

Figures 2.1 (a) and (b) show the schematic view of proposed GaSb/Si heterojunction based vertical TFETs without and with a source pocket. Their corresponding 2D cross-sectional views in X-Y plane are shown in Fig. 2(c) and (d), respectively. We will denote the GaSb/Si heterojunction vertical TFET without source pocket as GaSb/Si HJ

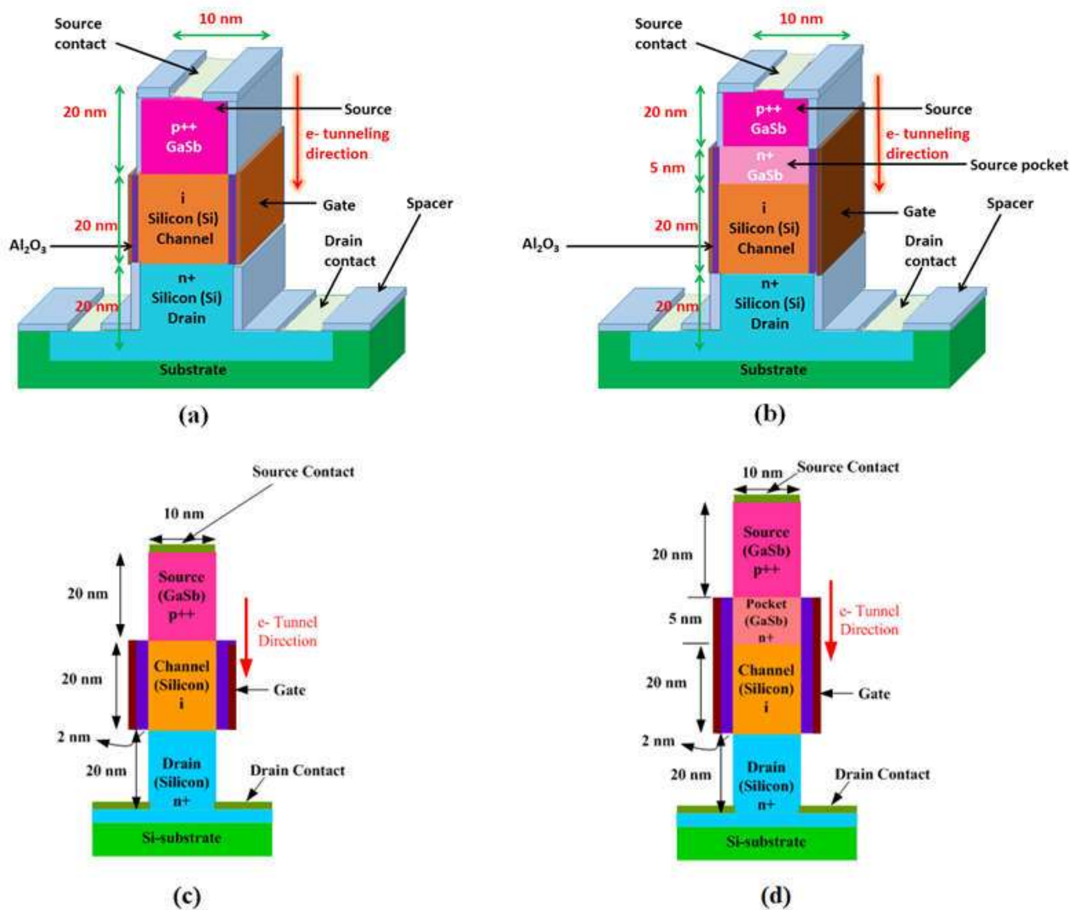

Fig. 2.1: (a) Schematic diagram of GaSb/Si heterojunction vertical TFET without source pocket (GaSb/Si HJ VTFET), and (b) Schematic diagram of GaSb/Si heterojunction vertical TFET with source pocket (SPE GaSb/Si HJ VTFET); (c) Cross sectional view of GaSb/Si HJ VTFET, and (d) Cross section view of SPE GaSb/Si HJ VTFET.

VTFET and the GaSb/Si heterojunction vertical TFET with source pocket as SPE GaSb/Si HJ VTFET for simplicity of discussion. The proposed devices are simulated using SILVACO ATLAS^{TM} 3D simulator. Various parameters used for the simulation are listed in Table-2.1.

2.2.2 Possible Fabrication Steps to Realize the Proposed TFET

The fabrication process flow of the proposed SPE GaSb/Si HJ VTFET is described in Fig. 2.2 pictorially in step-by-step manner. In this context it is worth mentioning that

TABLE 2.1

DIFFERENT PARAMETERS OF THE PROPOSED GaSb/Si HETEROJUNCTION VERTICAL TFET

Parameters	**GaSb/Si HJ VTFET**	**SPE GaSb/Si HJ VTFET**
Source doping concentration (N_A)	2×10^{19} cm^{-3}	$2\times10^{19}cm^{-3}$
Pocket doping concentration (N_D)	-	7×10^{18} cm^{-3}
Channel doping concentration (N_A)	5×10^{16} cm^{-3}	5×10^{16} cm^{-3}
Drain doping concentration (N_D)	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
Thickness of channel (t_{Si})	10 nm	10 nm
Thickness of gate oxide (t_{ox})	2 nm	2 nm
Gate work function (Φ_m)	4.2 eV	4.2 eV
Gate dielectric permittivity of Al_2O_3 (ε)	9.3	9.3
Gate length (L_G)	20 nm	25 nm
Source length (L_S)	20 nm	20 nm
Drain length (L_D)	20 nm	20 nm
Hole tunnel mass in GaSb (m_{htGaSb})	$0.4m_o$	$0.4m_o$
Electron tunnel mass in GaSb(m_{etGaSb})	$0.0410m_o$	$0.0410m_o$
Hole tunnel mass in silicon (m_{htSi})	$0.24m_o$	$0.24m_o$
Electron tunnel mass in silicon (m_{etSi})	$0.20m_o$	$0.20m_o$
Pocket length (GaSb)	-	5 nm
Lattice constant of GaSb	6.09 ^{0}A	6.09 ^{0}A
Lattice constant of Si	5.43 ^{0}A	5.43 ^{0}A
Bandgap energy GaSb	0.70 eV	0.70 eV
Bandgap energy Si	1.12 eV	1.12 eV
Electron affinity GaSb	4.06 eV	4.06 eV
Electron affinity Si	4.05 eV	4.05 eV

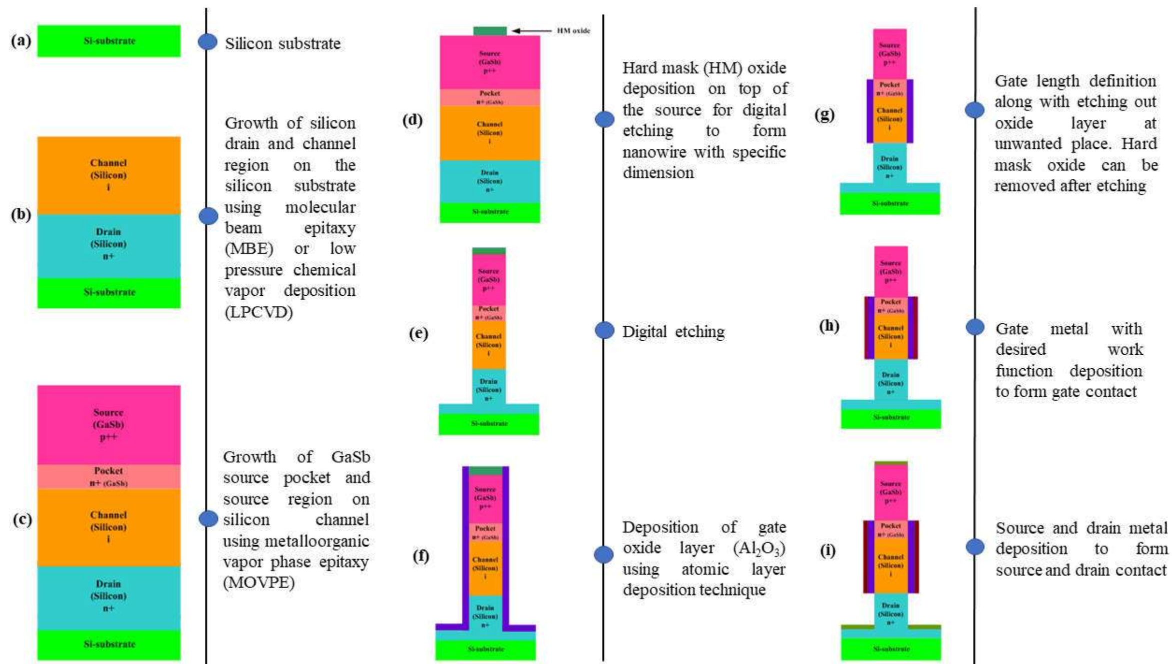

Fig. 2.2: Fabrication steps of the proposed structure in 2D view (a) Starting with a silicon (Si) substrate, (b) growth of silicon drain and channel region on the silicon substrate using molecular beam epitaxy (MBE) or low-pressure chemical vapor deposition (LPCVD), (c) growth of GaSb source pocket and source region on silicon channel using metalloorganic vapor phase epitaxy (MOVPE), (d) hard mask (HM) oxide deposition on top of the source for digital etching to form form width of the vertical TFET with specific dimension, (e) digital etching, (f) deposition of gate oxide layer (Al_2O_3) using atomic layer deposition (ALD) technique, (g) gate length definition along with etching out oxide layer at unwanted place. Hard mask oxide can be removed after etching, (h) gate metal with desired work function deposition to form gate contact, (i) source and drain metal deposition to form source and drain contacts.

this type of vertical TFET has been fabricated by different researchers earlier [81],[105],[119],[145],[89]. The process flow for fabricating the proposed SPE GaSb/Si HJ VTFET can start with a clean silicon substrate. The deposition of n^+ drain region followed by the deposition of the *i*-Si channel region can be done using the molecular beam epitaxy (MBE) or low pressure chemical vapor deposition method (LPCVD). GaSb material can then be grown for the source pocket followed by the growth of the

source region using the metalloorganic vapor phase epitaxy (MOVPE). Oxide hard mask (HM) can be deposited on the top of the source layer to define the vertical structure width. The digital etching can be used to etch out the rest of the portion to form vertical nanowire like structure. The Al_2O_3 layer (i.e. high *k* dielectric) of 2 nm can be deposited using atomic layer deposition (ALD). Oxide layer from the unwanted area can be removed by selective etching technique. The oxide hard mask can be removed after defining gate length. The gate metal electrode of required work function can be deposited on the gate oxide dielectric. The source and drain metallization can be done by Ti/Au or Ni/Au using sputtering method.

2.2.3 TCAD Simulation Methodology

The presented VTFETs have been simulated using SILVACO ATLAS^{TM} TCAD tool. Following models are used in the ATLAS^{TM} TCAD tool for simulating the proposed vertical TFET: (i) Non-local band-to-band tunneling (BTBT) model for including the local variation in the energy band for better tunneling accuracy; (ii) Shockley-Read-Hall generation-recombination model is included to consider the carrier generation-recombination phenomenon; (iii) band gap-narrowing model is used to incorporate the heavy doping effects on the bandgap of source, drain and source pocket regions; (iv) the Auger recombination model is used to include the non-radiative recombination processes; (v) the Fermi-Dirac statistics for carrier distribution in conduction band and valence band of the device, and (vi) The Lombardi Mobility model (CVT) is used to include the effect of transverse electric field on the mobility of the carriers in semiconductors. Uniform doping concentrations are assumed in various regions of the proposed device. A donor doping concentration (N_D) of $5x10^{18}$ cm^{-3} is considered for Si-drain region to reduce ambipolar effect in the TFET [59]. Note that the lattice and

thermal co-efficient mismatching between Si and GaSb may lead to the creation of bulk trap centers at the source-channel interface. To include the effects of such traps on the device performance, we have also included the non-local trap assisted models TAT.NLDEPTH and TAT.RELEI in the TCAD simulation tool. The dielectric constant of 9.3 for the Al_2O_3 material is considerd for our simulation [74]. Various parameter values used for the simulation of the proposed VTFET structures are listed in Table-2.1. Source pocket thickness of 5 nm is used in the entire thesis for achieving optimum performance. The values of the tunnel masses of electrons and holes listed in the table have taken from the SILVACO ATLAS^{TM} TCAD manual.

2.2.3.1 Description of Various Models used in the Simulations

In this sub-section, the objective of using various models for simulating the proposed TFETs using SILVACO ATLAS TCAD have been briefly discussed. The non local band-to-band tunnelling model is mostly used where tunnelling process is needed with the utmost accuracy. The local band-to-band tunnelling model based on Kane's work [4] is used to calculate generation and recombination rate at each point solely based on a constant local electric field in the tunelling path of the carriers. This does not consider the spatial variation in energy band profile. On the other hand, the non-local band-to-band tunneling model depends on the energy band profile of the semiconductor along the entire tunneling path [93]. It includes the effect of the variation in the electric field at each point in the tunneling path. The non-local Band-To-Band (BTB) tunneling model (BBT.NONLOCAL) of the SILVACO ATLAS TCAD allows the modeling of the forward and reverse biased tunneling currents. In the non-local BTB tunnelling model, tunnelling is assumed to take place on a series of 1D slices through the tunnelling junction. Here each of the slices is locally perpendicular to the junction and

they are approximately parallel to each other. ATLAS has two methods of setting up these areas of slices. At the time of simulation of the proposed device structures, the tunnelling area has been set up by specifying the number of tunnelling slices and the number of mesh points along the slices using the QTX.MESH and QTY.MESH statements. In addition, tunnelling direction has been using QTUNN.DIR in the model statement. In case of highly doped tunneling junction, the BTB tunneling current can be very high depending on the energy band profile of the junction. This in turn creates a charge dipole and affects the potential in a greater extent. Consequently, the band energies at and near the junction get affected and this type of coupling may create convergence issues. This problem can be resolve using BBT.NLDERIVS in the model statement which uses the non-local coupling to resolve the convergence issues. Effective mass models (ME.TUNNEL and MH.TUNNEL) of the carriers have been used with the values of the effective masses of carriers listed in Table 2.1.

Carrier generation-recombination is the process where a semiconductor tries to return to its equilibrium state after being disturbed by certain excitations. For instance, when light falls on a semiconductor, electrons get excited from the valence band to the conduction band and disturbs the equilibrium concentrations of electrons and holes in the semiconductor. The excess photogenerated electron-hole pairs get recombined so that thermal equilibrium carrier concentrations are achieved. The Shockley-Read-Hall (SRH) Recombination model has been used to include the effect of carrier recombinations in the semiconductors. This model also include the effect of phonon transitions occurred in the presence of a trap (or defect) within the forbidden gap of the semiconductors as suggested initially by Shockley and Read [2] and modified later by Hall [3]. Since the carriers' lifetime is a function of impurity concentration [18],[20],

the *SRH Concentration-Dependent Lifetime Model* (CONSRH) is used in our simulation to include the effect of carrier concentration on the generation-recombination process at the trap centers located at the source-channel junction.

The Auger recombination process occurs through a three-particle transition whereby a mobile carrier is either captured or emitted by the trap center according to the physics of the Auger recombination phenomenon [15]. Narrow band gap Auger model suggested by Beattie [26] is more suitable when the bandgap of the semiconductor is less than 1.5 eV. The AUGER model in the TACD is used to include the effect of the narrow band gap GaSb in the proposed TFET structures. The Fermi-Dirac statistics is used via the FERMI model of the TCAD for the carrier distribution in conduction band and valence band of the semiconductors used in the device. The Lombardi Mobility model (CVT) is used to include the effect of transverse electric field on the mobility of the carriers in semiconductors.

It is well known that heavy doping in any semiconductor reduces its bandgap energy. The band gap narrowing model (BGN) of the TCAD includes the effect of heavy doping of the source, pocket and drain regions on the performance of the proposed vertical TFET device. The GaSb material used for the source region has a lattice mismatching with silicon of about ~11%. For this reason, the non-local trap assisted tunneling models TAT.NLDEPTH and TAT.RELEI are used in the TCAD simulation. The traps are assumed to be nearer to the valence band of the source material.

The numerical method “NEWTON” is used in the METHOD statements of the input file. The NEWTON method solves the total number of system of unknowns together. It is believed to be an very effective method strongly coupled system equations with a quadratic convergence.

Meshing plays an important role in the TCAD simulation of TFETs using non-local BTB model. The various important regions like the electrodes, junctions, interface between semiconductor and oxide layer etc. of the device must be accurately represented by the mehing. The finer is the meshing, the accurate is the result. We have used fine rectangular meshing for the simulation of our proposed vertical TFETs to achieve the optimum results.

2.2.3.2 Models Callibration

We have first calibrated the models used for simulation using SILVACO ATLAS TCAD tool for our proposed VTFET structures of Fig. 2.1. The TCAD simulation results (i.e. I-V characteristics for both linear-linear and log-linear scale) of the Ge/Si heterojunction based VTFET have been compared with the measured data reported by Nerves *et al.* [119]. The device design parameters of the Ge/Si heterojunction based VTFET was kept same as the experemetal data based on fabrication report by Nerves *et al.* [119] having an oxide thickness of 2 nm at V_{DS} of 0.9 V. Better fitting with the experimental data can be obtained by adjusting the effective masses (ME.TUNNEL and MH.TUNNEL) of the carriers in the material statement. However, we used the values of the effective masses of the carriers from the ATLAS manual which are listed in the Table-2.1. Fine rectangular meshing is used to define various regions of interest (e.g., tunneling junction, at contact terminals etc.) of the proposed device. Temperature dependency on the I-V characteristics has been checked thoroughly. We observed a reasonably good matching between the two results which ensures the validity of the chosen models. A slight difference between the simulation and experimental results in Fig. 2.3 can be attributed to the non-ideal measured characteristics of the practical VTFET.

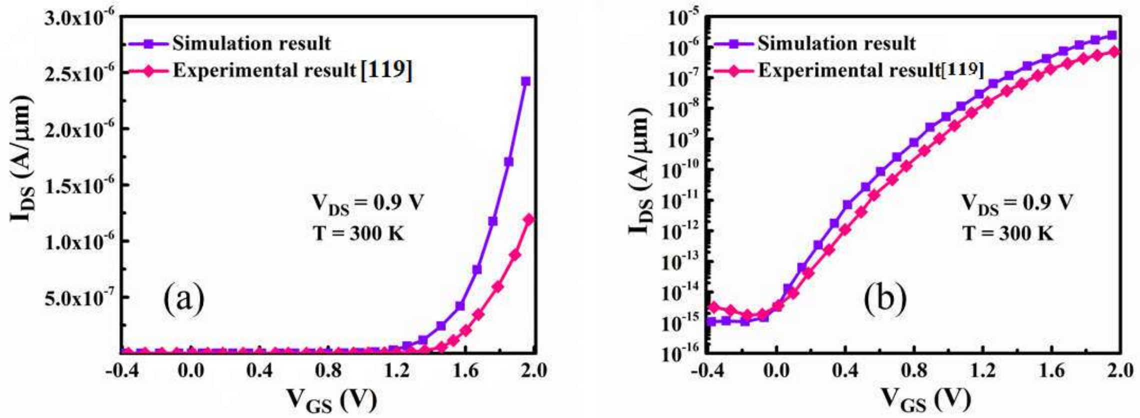

Fig. 2.3: Calibration of used models in SILVACO ATLAS^{TM} 3D TCAD tool: comparison of simulation results of I_{DS}-V_{GS} in (a) linear-linear scale (b) log-linear scale with experimental results of a Ge source based VTFET [119]

2.3 Results and Discussion

In this section, we will first present device-level performance analysis of vertically grown GaSb/Si heterojunction TFET with and without source pocket namely SPE GaSb/Si HJ VTFET and GaSb/Si HJ VTFET respectively using SILVACO ATLAS^{TM} TCAD tool.

2.3.1 DC Performance Analysis

Fig. 2.4 (a) and (b) show the energy band diagrams of the SPE GaSb/Si HJ VTFET and GaSb/Si HJ VTFET under OFF as well as ON-states of operations, respectively. Under OFF-state (i.e. zero gate bias) misalignment between the valence band of source and the conduction band of the channel does not allow the electrons to tunnel through the source-channel junction. However, when a positive gate bias is applied under ON-state, electron-occupied valence band of the source is aligned with the empty states of the conduction band of the channel due to a significant band bending. This causes tunneling of electrons from the valence band of the source to the conduction band of the channel

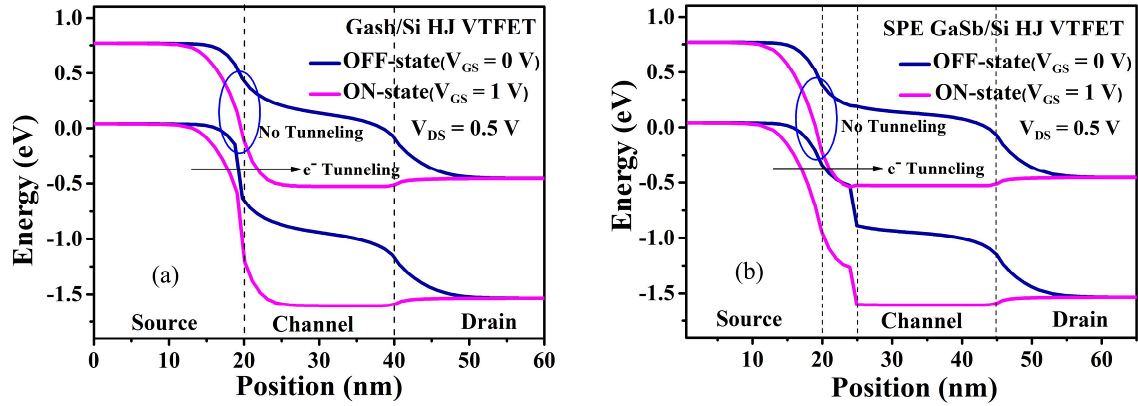

Fig. 2.4: (a) Energy band distribution of GaSb/Si HJ VTFET in OFF-state as well as in ON-state; (b) Energy band distribution of SPE GaSb/Si HJ VTFET in OFF-state as well as in ON-state.

as shown in Fig. 2.4. The GaSb/Si forms a staggered gap heterojunction (Type-II) at the source-channel interface. Fig. 2.4(a) and (b) show that tunneling of carriers through the source/channel heterojunction is increased with the applied positive gate voltage.

The transfer characteristics of the proposed VTFETs with and without pocket have been compared in Fig. 2.5(a) while their output characteristics have been compared in Fig. 2.5(b). The I_{ON}/I_{OFF} ratio of 6.87×10^{11} and 7.5×10^{11} are obtained for GaSb/Si HJ VTFET and SPE GaSb/Si HJ VTFET, respectively. While the drain voltage (V_{DS}) of 0.5 V and the gate voltage (V_{GS}) varying from 0 V to 1 V are used in Fig. 2.5(a), V_{GS} of 0.5 V and (V_{DS}) varying from 0 V to 1 V are considered in determining the output characteristics shown in Fig. 2.5(b). The parameters like I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, average SS (calculated using constant current method [55]) and the threshold voltage (V_T) of the proposed VTFETs with and without pocket are listed in Table-2.2 which is given at the end of device level performance comparison between the aforesaid two VTFETs. The average sub-threshold swing (SS) of 26 mV/dec and 43 mV/dec are obtained for SPE GaSb/Si HJ VTFET and GaSb/Si HJ VTFET respectively. Clearly, SPE GaSb/Si HJ VTFET

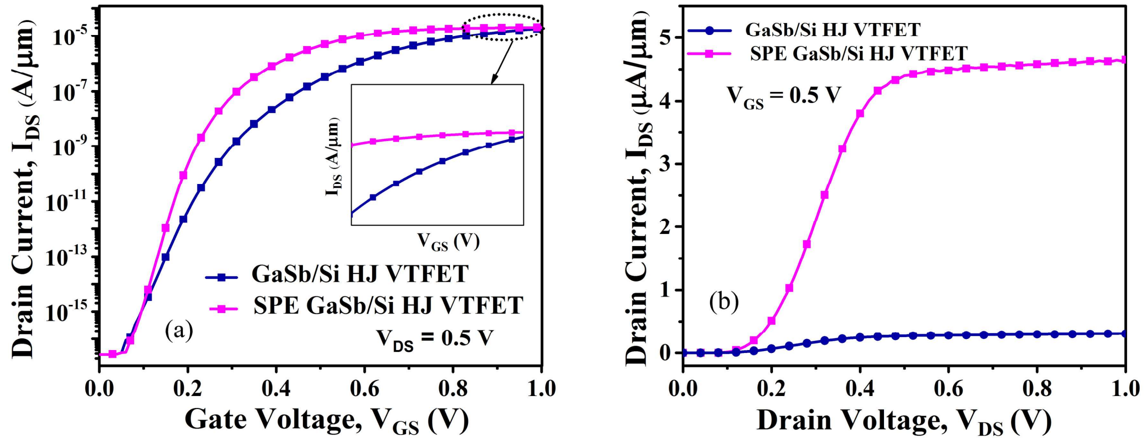

Fig. 2.5: (a) Transfer characteristics of GaSb/Si HJ VTFET and SPE GaSb/Si HJ VTFET; (b) Output characteristics of GaSb/Si HJ VTFET and SPE GaSb/Si HJ VTFET.

shows a better performance over the GaSb/Si HJ VTFET in terms of improved I_{ON}/I_{OFF} ratio and SS. It is important to mention that the ON-current in SPE GaSb/Si HJ VTFET is slightly higher than that of the GaSb/Si HJ VTFET. However, the SS is considerably smaller in the SPE GaSb/Si HJ VTFET than that of the GaSb/Si HJ VTFET structure. Further, I_{OFF} is observed to be almost same for both VTEFTs. The higher ON-current results in higher I_{ON}/I_{OFF} ratio of SPE GaSb/Si HJ VTFET over the GaSb/Si HJ VTFET structure despite having almost same OFF-state current for both VTEFTs. The improved sub-threshold performance of the SPE GaSb/Si HJ VTFET makes the device better suitable for low power applications than the GaSb/Si HJ VTFET device. The lower threshold voltage in SPE GaSb/Si HJ VTFET enables to achieve the saturation drain current at a lower gate voltage thereby making it a better choice for low-voltage and low-power applications over the GaSb/Si HJ VTFET device.

2.3.2 Temperature Reliability Analysis

Since the I-V characteristics of TFET are highly temperature dependent [74], we will now discuss the performance of the VTFETs under study for different temperatures.

Fig. 2.6(a) compares the average SS of two types of VTFET under study for different temperatures ranging from 250 K to 400 K for fixed drain and gate voltages. The SS of GaSb/Si HJ VTFET is significantly higher at high temperatures than that of the SPE GaSb/Si HJ VTFET. Clearly, the introduction of pocket in VTFET improves the temperature stability of the VTFETs. The variation of I_{ON}/I_{OFF} ratio as a function temperature of the two VTFET structures is shown in Fig. 2.6(b) for temperature range of 250-400 K. Though the I_{ON}/I_{OFF} ratio of SPE GaSb/Si HJ VTFET is larger than that of the GaSb/Si HJ VTFET at lower temperature below 300K, but the ratio of the both the VTFETs is significantly decreased at nearly same rate at higher temperatures above 350 K. However, both the proposed VTFET structures based on GaSb/Si heterojunction under study maintains an I_{ON}/I_{OFF} ratio of 10^8 above room temperature which meets the minimum requirements prescribed in the ITRS 2.0 [140].

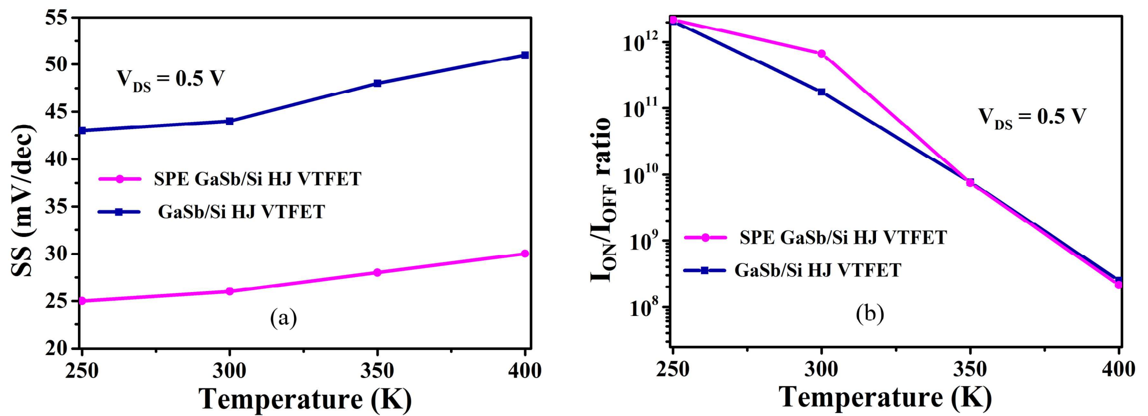

Fig. 2.6: Comparative plot of (a) SS, and (b) I_{ON}/I_{OFF} ratio with respect to temperature for GaSb/Si HJ VTFET and SPE GaSb/Si HJ VTFET.

2.3.3 Analog/RF Performance Evaluation

We will now compare various RF figures of merit (FOMs) like transconductance (g_m), output conductance (g_d), gate to drain capacitance (C_{gd}), gate to source capacitance

(C_{gs}), cut-off frequency (f_T), gain bandwidth product (GBP), maximum frequency (f_{max}), transit time (τ), transconductance generation factor (TGF) and transconductance frequency product (TFP) of both GaSb/Si HJ VTFET and SPE GaSb/Si HJ VTFET.

Fig. 2.7(a) compares the transconductance (g_m) characteristics of VTFETs with and without pocket while the output conductance (g_d) of the two VTFET structures are compared in Fig. 2.7(b). It is observed from Fig. 2.7(a) that g_m of SPE GaSb/Si HJ VTFET is comparatively higher than GaSb/Si HJ VTFET with the maximum transconductance of 66 μS/μm in SPE GaSb/Si HJ VTFET larger than the maximum transconductance of 54 μS/μm of GaSb/Si HJ VTFET. As g_m represents the ability of the device to convert the gate voltage to drain current, the higher value of g_m in SPE GaSb/Si HJ VTFET signifies better rate of gate voltage to drain current conversion than that of the GaSb/Si HJ VTFET structure. The comparison of output conductance characteristics (g_d) of the two VTFET devices under study shown in Fig. 2.7(b) demonstrates a significantly larger g_d of the SPE GaSb/Si HJ VTFET than that of the GaSb/Si HJ VTFET with the maximum values of 19 μS/μm and 11 μS/μm in V-TFETs

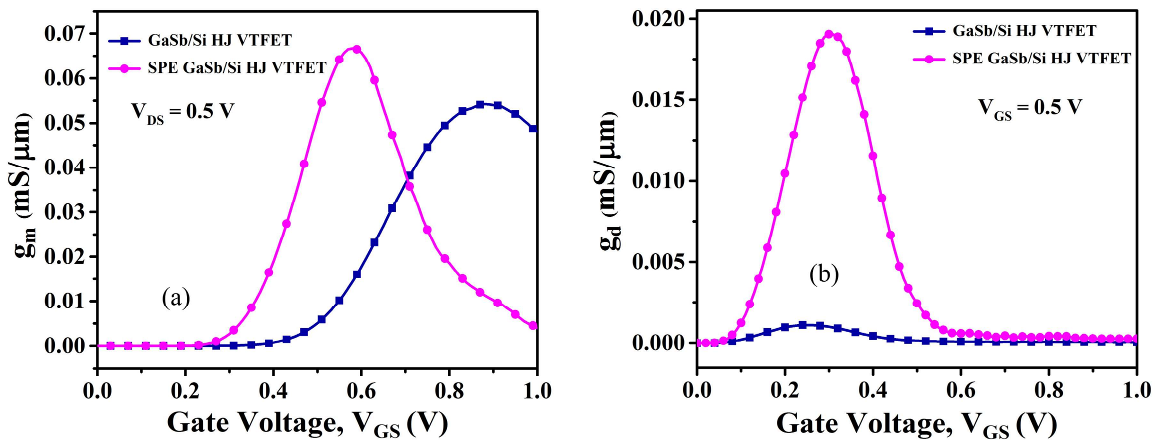

Fig. 2.7: (a) Transconductance (g_m) comparison of GaSb/Si HJ VTFET and SPE GaSb/Si HJ VTFET. (b) Output conductance (g_d) comparison of GaSb/Si HJ VTFET and SPE GaSb/Si HJ VTFET.

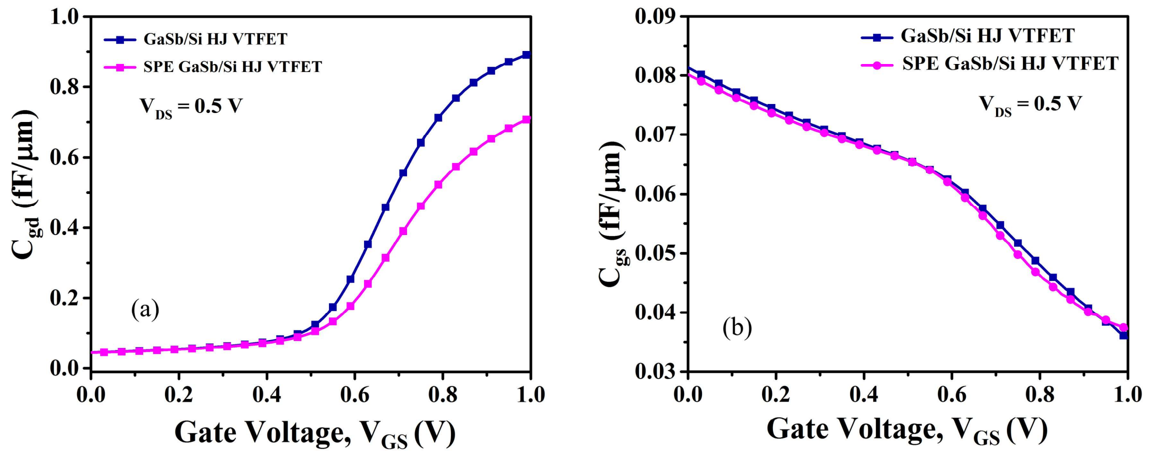

Fig. 2.8: Comparative plot of (a) gate to drain capacitance (C_{gd}) (b) gate to source capacitance (C_{gs}) with respect to gate to source voltage (V_{GS}) for GaSb/Si HJ VTFET and SPE GaSb/Si HJ VTFET.

with and without pocket respectively. This implies that SPE GaSb/Si HJ VTFET has a better conversion capability of drain voltage to drain current than that of the GaSb/Si HJ VTFET structure.

Now we will consider the intrinsic gate-drain capacitance (C_{gd}) and intrinsic gate-source capacitance (C_{gs}) which are important parameters for the RF performance analysis of any MOS transistor. Unlike conventional MOSFETs, C_{gd} in TFETs is treated as parasitic or Miller capacitance which is much larger than C_{gs} [71] as shown in Fig. 2.8 for both the proposed VTFET devices under consideration. Therefore, the effect of paracitic capacitance C_{gs} is sometimes neglected in TFET. Fig. 2.8(a) compares the C_{gd} for two devices whereas Fig. 2.8(b) shows the comparison of C_{gs} of the devices under study. The C_{gd} of the GaSb/Si HJ VTFET is found to be larger than SPE GaSb/Si HJ VTFET as reported by others [91]. This implies that SPE GaSb/Si HJ VTFET with smaller C_{gd} has better circuit level performance due to smaller parasitic effects. Fig. 2.8(b) shows nearly same C_{gs} value for the two presented VTFETs.

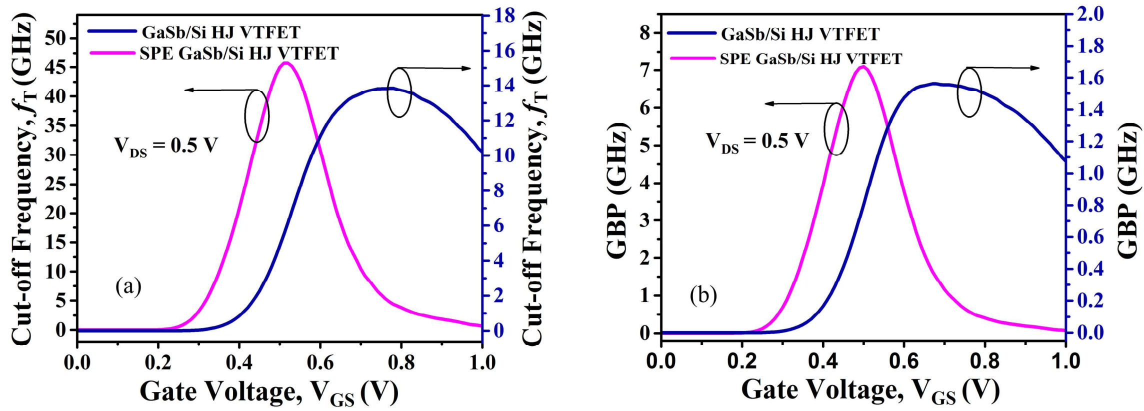

Fig. 2.9: Comparative plot of (a) f_T, and (b) GBP with respect to gate to source voltage (V_{GS}) for GaSb/Si HJ VTFET and SPE GaSb/Si HJ VTFET.

The cutoff frequency (f_T) and GBP are essential parameters for investigating the RF performance of any MOSFET device. The cut-off frequency (f_T), defined as the frequency at which the short-circuited current gain becomes unity. It is given by the formula [46]:

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \tag{2.1}$$

Equation (2.1) shows that f_T is proportional to g_m and (nearly) inversely proportional to the C_{gd}. From the results of Fig. 2.7 and Fig. 2.8 show that f_T of the SPE GaSb/Si HJ TFET should be higher than that of the non-SPE GaSb/Si HJ structure. Further, f_T versus V_{gs} characteristics the devices should be nearly proportional to the g_m versus V_{gs} characteristics of the devices. The comparison of f_T for both the devices under study is shown in Fig. 2.9(a). It demonstrates that f_T increases initially with the gate-source voltage due to increase in g_m. But it starts to decrease with the increased gate-source voltage after a value due to the decrease in g_m at higher gate-source voltage owing to the mobility degradation [135]. The SPE GaSb/Si HJ VTFET possesses a much larger

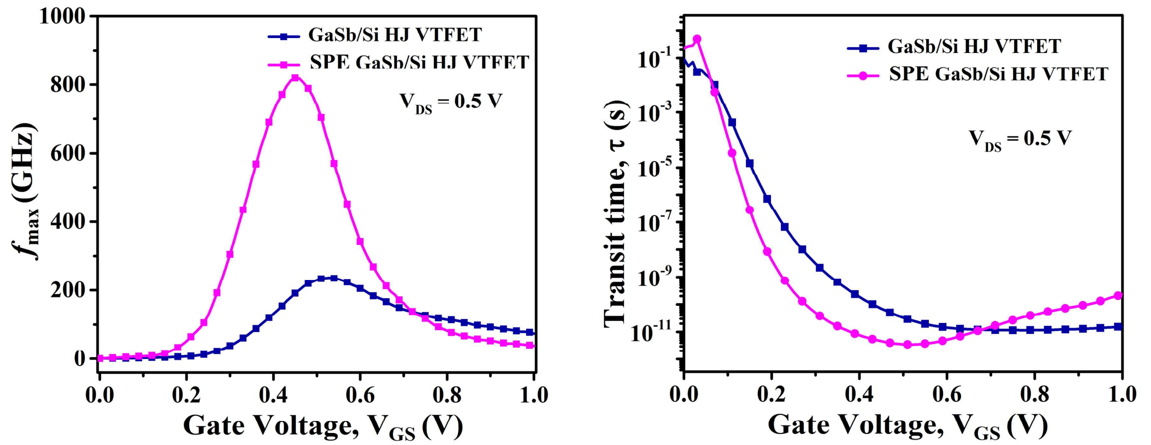

Fig. 2.10: Comparative plot of (a) f_{max}, and (b) transit time for GaSb/Si HJ VTFET and SPE GaSb/Si HJ VTFET.

value of f_T (~46 GHz) than that of the GaSb/Si HJ VTFET (with ~13 GHz) due to larger g_m in the device with a pocket. The gain-bandwidth product (GBP) calculated for a DC gain of 10 can be formulated as [153]

$$GBP = \frac{g_m}{2\pi(10C_{gd})} \tag{2.2}$$

The GBP signifies the constant gain region of operation of a MOS device. Fig. 2.9(b) shows the GBPs of the SPE GaSb/Si HJ VTFET and GaSb/Si HJ VTFET are ~ 7 GHz and 1.6 GHz respectively which is 5 times larger GBP of the SPE GaSb/Si HJ VTFET than that of the GaSb/Si HJ VTFET is obtained by introducing the source pocket.

The maximum frequency of oscillation (f_{max}), defined as the frequency at which unilateral power gain drops to unity, is formulated as [137]:

$$f_{max} = f_0\sqrt{\frac{|Y_{21}-Y_{12}|^2}{4[Re(Y_{11})Re(Y_{22})-Re(Y_{12})Re(Y_{21})]}} \tag{2.3}$$

where [illegible] are the Y-parameter of the device at applied frequency f_0 which is

considered as 1 MHz for all the Y parameter extraction from Eq.(2.3). Fig. 2.10(a) shows that f_{max} follows the same trend as that of f_T. The f_{max} of the SPE GaSb/Si HJ VTFET is ~800 GHz which is 3.5 times higher than that of the GaSb/Si HJ VTFET. The transit time (τ) is also considered as an important parameter for analog/RF performance analysis. It is used to measure the time required for the charge carriers to move from source to drain region. Hence, it enumerates the faster operation of the device in circuit and can be formulated as given below [46]:

$$\tau = \frac{1}{2\pi f_T} \tag{2.4}$$

For better switching performance, the transit time is desired to be as low as possible. Fig. 2.10(b) compares the transit time plots for both VTFET devices under investigation. The smaller value of τ in the SPE GaSb/Si HJ VTFET ensures its higher speed of operation over the GaSb/Si HJ VTFET structure.

The device efficiency or transconductance generation factor (TGF) is defined as the capability of a device to convert the current into transconductance. It is a trade-off between power and high-speed operation of any MOSFET device. The TGF can be

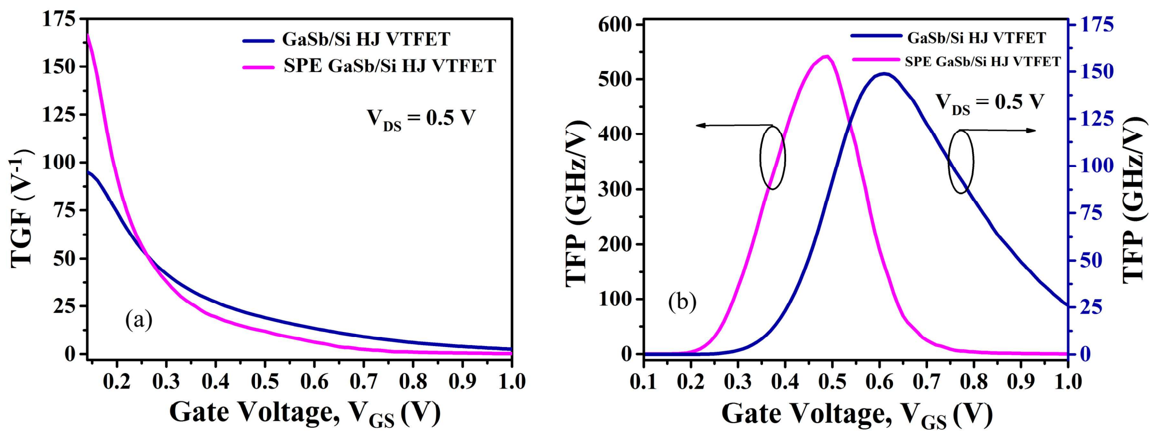

Fig. 2.11: Comparative plot of (a) TGF, and (b) TFP with respect to gate to source voltage(V_{GS}) for GaSb/Si HJ VTFET and SPE GaSb/Si HJ VTFET.

TABLE 2.2

COMPARISON OF DIFFERENT DC/RF PARAMETERS OF THE PROPOSED HETEROJUNCTION VERTICAL TFETS WITH SOME REFERENCES

Parameters	**GaSb/Si HJ VTFET**	**SPE GaSb/Si HJ VTFET**	**Seema *et al.* [153]**	**Wang *et al.* [137]**
I_{ON} (A/μm)	1.89 x 10^{-5}	2.068 x10^{-5}	1.8 x 10^{-5}	1.9x10^{-6}
I_{OFF} (A/μm)	2.75× 10^{-17}	2.76x10^{-17}	1.2x 10^{-16}	2.0x10^{-17}
I_{ON}/ I_{OFF}	6.87x10^{11}	7.5x10^{11}	1.46x10^{11}	9.5x10^{10}
Avg.SS (mV/dec)	43	26	40.44	79.8
g_m (μS/μm)	54	66	74	7
g_d (μS/μm)	11	19	-	3
f_T (GHz)	13	46	0.17	0.7
f_{max}(GHz)	225	800	-	36
GBP(GHz)	1.6	7	0.16	0.4
TGF (V^{-1})	94	165	-	-
TFP (GHz)	150	550	500	-

given by [153]:

$$TGF = \frac{g_m}{I_{ds}} \tag{2.5}$$

Fig. 2.11 (a) compares TGF as a function of gate voltage. It is noted that SPE GaSb/Si HJ VTFET has higher device efficiency than that of the GaSb/Si HJ VTFET structure. The transconductance frequency product (TFP) is also an essential RF FOM of the TFETs. It is the product of TGF and f_T as given by [135]:

$$TFP = \left(\frac{g_m}{I_{ds}}\right) \times f_T \tag{2.6}$$

The TFP represents a trade-off between the bandwidth and power of any MOSFET for moderate to high speed operation. Fig. 2.10 (b) shows that SPE GaSb/Si HJ VTFET has higher TFP than that GaSb/Si HJ VTFET structure due to its higher f_T and higher device efficiency. Devices with higher TFP are required for high-speed circuit design. The high TFP of any MOSFET also implies a good linearity of the device. The simulated results of our proposed VTFETs with and without pocket have been listed and compared with some recent reported data in Table-2.2. It is observed that the proposed VTFET with a source pocket (i.e. SPE GaSb/Si HJ VTFET) has better DC and RF performance parameters over other TFET devices.

2.4 SPE GaSb/Si HJ VTFET Verses SPE All-Si VTFET: Performance Comparison

Now we will compare the device level performance of vertically grown GaSb/Si heterojunction TFET with source pocket to that of vertically grown All-Si TFET with source pocket. Since silicon based TFET has garnered significant attention in past years because of all CMOS based technology is more compatible for all-Si based devices, an insight into device level performance analysis requires utmost attention to verify how the devices are performing for different RF applications. For simplicity we are naming the vertically grown GaSb/Si heterojunction TFET with source pocket as SPE GaSb/Si HJ VTFET and vertically grown all-Si TFET with source pocket as SPE All-Si VTFET for further analysis. Fig. 2.12(a) and (b) shows schematic diagram of SPE All-Si VTFET and SPE GaSb/Si HJ VTFET and their cross sectional view is shown in Fig.

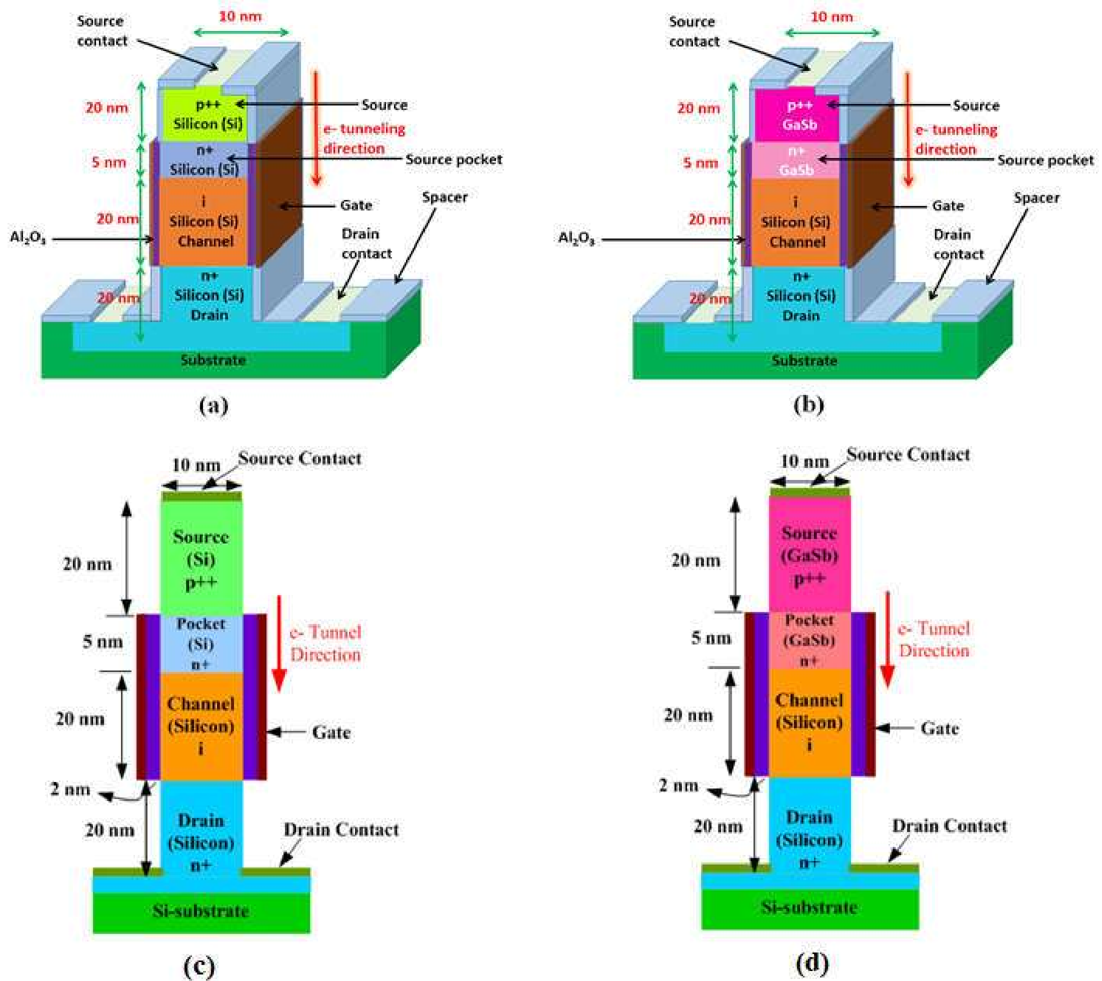

Fig. 2.12: Schematic diagram of (a) source pocket engineered all-Si vertical TFET (SPE All-Si VTFET) and (b) source pocket engineered GaSb/Si heterojunction vertical TFET (SPE GaSb/Si HJ VTFET); and cross sectional view of (c) SPE All-Si VTFET and (d) SPE GaSb/Si HJ VTFET.

2.12(c) and (d) respectively. Various optimized device design parameters along with optimized doping concentration for the device simulations using SILVACO ATLAS^{TM} TCAD simulation tool are given in Table-2.3. The models which are included for simulation using the TCAD tool are same as discussed in the earlier in the beginning of TCAD simulation framework section. All the choosen models for device simulations been calibrated with experimental results as stated earlier at the starting of this section. To start the device level performance analysis, energy band (E-B) distibution is

TABLE 2.3

DEVICE PARAMETERS WITH OPTIMIZED VALUE FOR THE PRESENTED VERTICAL TFETS

Parameters	**SPE All-Si VTFET**	**SPE GaSb/Si HJ VTFET**
Source region doping (N_A)	2×10^{19} cm^{-3}	$2\times10^{19}cm^{-3}$
Pocket layer doping (N_D)	7×10^{18} cm^{-3}	7×10^{18} cm^{-3}
Channel region doping (N_A)	5×10^{16} cm^{-3}	5×10^{16} cm^{-3}
Drain region doping (N_D)	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
Gate metal work function (Φ_m)	4.2 eV	4.2 eV
Gate dielectric (Al_2O_3 (ε)) permittivity	9.3	9.3
Gate region length (L_G)	25 nm	25 nm
Source region length (L_S)	20 nm	20 nm
Drain region length (L_D)	20 nm	20 nm
Hole tunnel mass of GaSb (m_{htGaSb})	-	$0.4m_o$
Electron tunnel mass of Gasb (m_{etGaSb})	-	$0.0410m_o$
Hole tunnel mass of Si (m_{htSi})	$0.24m_o$	$0.24m_o$
Electron tunnel mass Si(m_{etSi})	$0.20m_o$	$0.20m_o$
Lattice constant of GaSb	-	6.09 ^{0}A
Lattice constant of Si	5.43 ^{0}A	5.43 ^{0}A
Bandgap energy GaSb	-	0.70 eV
Bandgap energy Si	1.12 eV	1.12 eV
Electron affinity GaSb	-	4.06 eV
Electron affinity Si	4.05 eV	4.05 eV

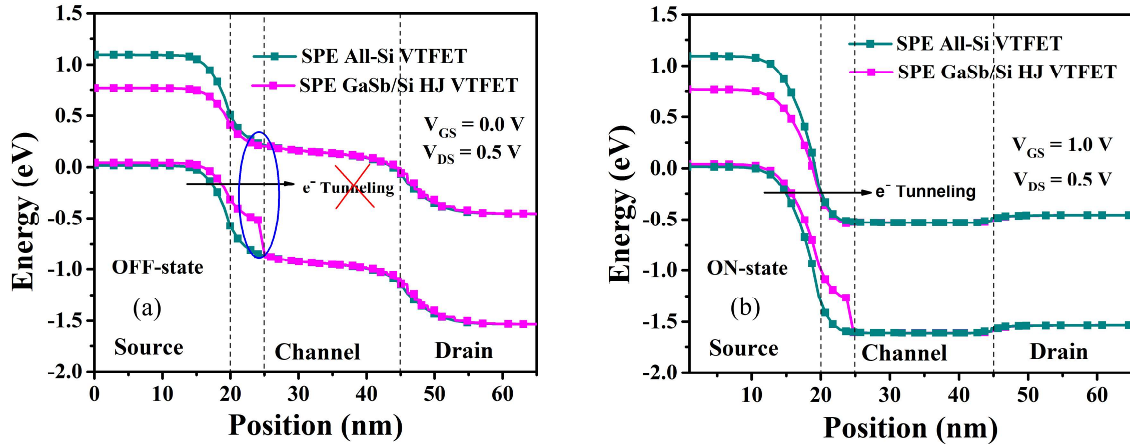

Fig. 2.13: (a) OFF-state energy band diagram of SPE All-Si VTFET and SPE GaSb/Si HJ VTFET and (b) ON-state energy band diagram of SPE All-Si VTFET and SPE GaSb/Si HJ VTFET.

considered as most important analysis to predict the behavior of the proposed VTFET. Fig. 2.13(a) and (b) shows the E-B diagram of the presented VTFETs in OFF-state and ON-state is shown in respectively. When zero gate voltage is applied across gate to source terminal, the conduction band of the channel and the valence band of source are not properly aligned as shown in Fig. 2.13(a) and it is called OFF-state. Therefore, electrons cannot be transported through source-channel junction. However, with the application of positive gate voltage, a tunneling path is created due to the lowering of conduction band of the channel which makes suitable alignment between source of the valence band with the channel in conduction band. This in turns inhibits the tunneling phenomena where electrons tunneling process can take place as shown in Fig. 2.13(b). This state is known as ON-state. Tunneling barrier width of the proposed SPE GaSb/Si HJ VTFET is lesser than SPE All-Si VTFET which leads to higher carriers tunneling for the SPE GaSb/Si HJ VTFET. Lower tunneling width of the SPE GaSb/Si HJ VTFET in comparison to SPE All-Si VTFET can be attributed to the use of narrow band gap material like GaSb in the source region. Due to lower tunneling width, the electric field

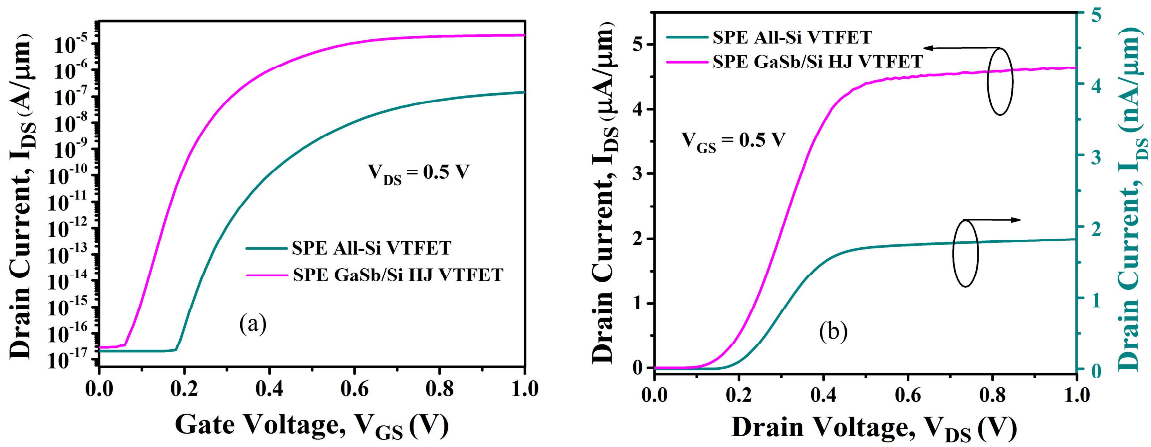

Fig. 2.14: Comparison of (a) transfer characteristics, and (b) output characteristics for SPE All-Si VTFET and SPE GaSb/Si HJ VTFET.

at source-channel junction increases. This in turn minimizes the subthreshold swing as well as potential drop at the tunneling junction. This leads to higher ON-current in the GaSb/Si HJ VTFET than All-Si counterpart.

The transfer and output characteristics of all the VTFETs under study are compared in Fig. 2.14 (a) and (b) respectively. To obtain transfer characteristics, the drain voltage is fixed at 0.5 V whereas the gate voltage is varied from 0 V to 1 V. In contrary, the output characteristics are obtained for a fixed gate voltage of 0.5 V but with a varying drain voltage over 0V to 1 V. The results in Fig. 2.14(a) shows that the OFF-state currents are nearly same for both the VTFETs under study. It may be noted that, in general, the OFF-state currents in Ge/Si and InAs/Si heterojunction TFETs are higher than that of all-Si based TFETs [89]. The OFF-state current in our proposed SPE GaSb/Si HJ VTFET is smaller than the commonly used Ge/Si and InAs/Si heterojunction TFETs [89]. The results in Fig 2.14(b) gives the output current of GaSb/Si VTFET WP in the μA range whereas the output current of SPE All-Si VTFET is in nA range. The reason behind high ON-current in SPE GaSb/Si HJ VTFET is

attributed to lower effective mass of carriers (electrons) in GaSb which are considered as source material in our proposed TFETs. In addition to this, lower tunneling width of III-V/Si based TFETs is also significantly improves the ON-current.

The parameters like I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, average SS and threshold voltage (V_T) of both the devices are listed in Table-2.4 at the end this sub-section. To calculate threshold voltages of respective devices, constant current (10^{-7} A) method is adopted [55]. The I_{ON}/I_{OFF} ratio is found to be in the order of 10^{11} in our proposed staggered heterojunction-based SPE GaSb/Si HJ VTFET whereas it is in the order of 10^{9} for SPE All-Si VTFET. Clearly, SPE GaSb/Si HJ VTFET has higher ON-current than that of SPE All-Si VTFET under similar operating conditions. The sub-threshold swing of SPE All-Si VTFET and SPE GaSb/Si HJ VTFET are 67 mV/dec, and 26 mV/dec respectively. The results in Fig. 2.14 demonstrates that SPE GaSb/Si HJ VTFET device outperforms SPE All-Si VTFET.

As electrical performance parameters such as SS and I_{ON}/I_{OFF} ratio are temperature dependent [74], the temperature reliability study is further performed for both the TFETs under study i.e SPE All-Si VTFET and SPE GaSb/Si HJ VTFET at various operating temperatures ranging from 250 K to 450 K. Fig. 2.15(a) shows variation in SS for SPE All-Si VTFET and SPE GaSb/Si HJ VTFET at different temperatures ranging from 250 K to 450 K by keeping the drain and gate voltage constant. It is clearly evident from the figure that the variation in SS for SPE All-Si VTFET is significantly increasing at higher temperature above 350 K compared to SPE GaSb/Si HJ VTFET. The average SS remains below 40 mV/dec for SPE GaSb/Si HJ VTFET even at temperature 450 K opens avenues for performing better at higher temperature too whereas SS of more than 100 questions the credibility of the device SPE All-Si

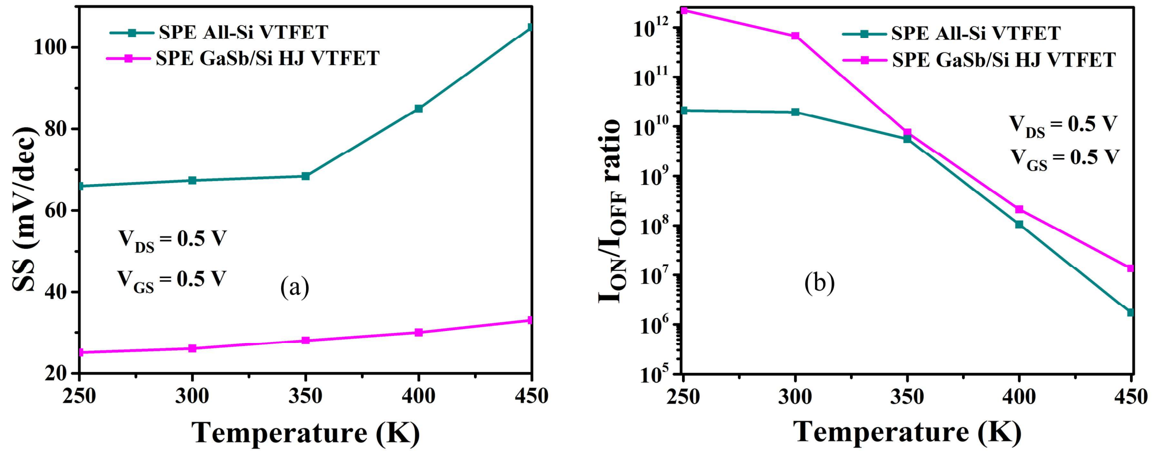

Fig. 2.15: Comparison of (a) SS, and (b) I_{ON}/I_{OFF} ratio for SPE All-Si VTFET and SPE GaSb/Si HJ VTFET with respect to temperature varying from 250 K to 450 K.

VTFET to operate at higher temperature node.Figure 2.15(b) depicts the variation of I_{ON}/I_{OFF} ratio for both the TFETs at various temperatures starting from 250 K to 450 K. This figure reveals that at higher temperature more than 350 K the I_{ON}/I_{OFF} ratio is significantly decreasing for both the TFETs including the heterojunction devices SPE GaSb/Si HJ VTFET. The decrease in I_{ON}/I_{OFF} ratio with increased temperature is attributed to the exponential increase in I_{OFF} due to the Shockley–Read–Hall (SRH) generation–recombination in the reverse-biased gated p^{++}-i-n^{+} diode structure of the TFETs [74]. Due to significant increase in I_{OFF} with increase in temperature, I_{ON}/I_{OFF} ratio decreases rapidly. It is here to note that the I_{ON} also increases with increase in temperature. However, the order at which I_{OFF} increases is much higher than I_{ON} which leads to make an overall decrease in I_{ON}/I_{OFF} ratio with increase in temperature.

A detail comparison study is made for various analog/RF figure of merits (FOMs) as discussed earlier in this section for SPE All-Si VTFET and SPE GaSb/Si HJ VTFET. Figure 2.16 compares the transconductance (g_m) and output conductance (g_d) characteristics as a function of gate voltage under ON-state operation of SPE All-Si

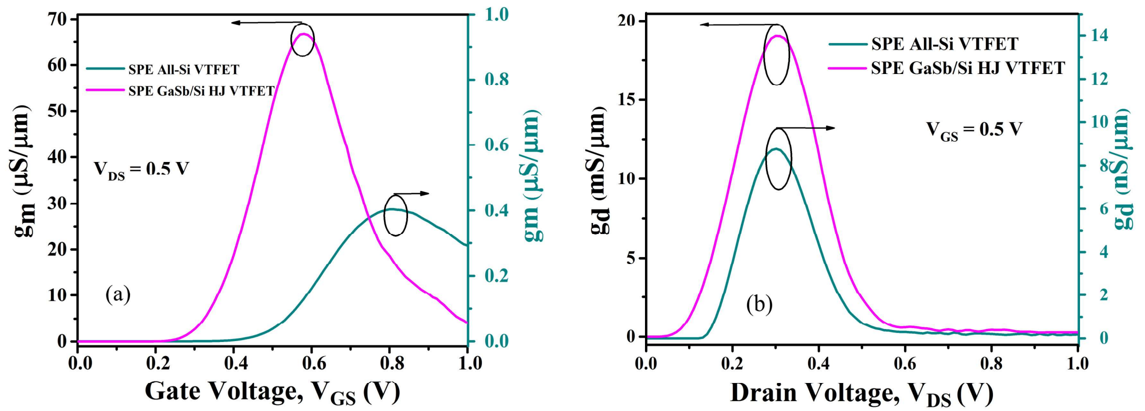

Fig. 2.16: Comparison of (a) transconductance, and (b) output conductance of SPE All-Si VTFET and SPE GaSb/Si HJ VTFET.

VTFET and SPE GaSb/Si HJ VTFET. As discussed earlier in this section that the transconductance (g_m) is an important parameter of any FET since g_m represents the convertion capability of gate voltage (V_{GS}) to drain current (I_D) of the device. The higher the value of $g_{m,}$ the better performance of the device at high frequency. The results shown in Fig. 2.16(a) demonstrate that SPE GaSb/Si HJ VTFET has the higher value of g_m (~66 µS/µm) while the maximum values of g_m of SPE All-Si VTFET is 0.4 µS/µm respectively. The reason for the higher value of g_m of SPE GaSb/Si HJ VTFET over SPE All-Si VTFET can be attiributed to higher drain current in the former VTFET. The output conductance (g_d) of both the devices under study are shown in Fig. 2.16(b). The parameter g_d signifies the rate of conversion of drain voltage (V_{DS}) to drain current (I_D).The maximum value of g_d of 19 µS/µm is obtained in SPE GaSb/Si HJ VTFET whereas the maximum values of g_d of SPE All-Si VTFET is 8.25 nS/µm respectively. As gate drain intrinsic capacitance (C_{gd}) and gate source intrinsic capacitance (C_{gs}) are also important RF parameters of any MOS transistor, we will find out how the intinsic capacitances are varying for both the VTFETs under consideration. Unlike MOSFETs, C_{gd} is considerably higher than C_{gs} in TFETs [71], and it is considered as parasitic or

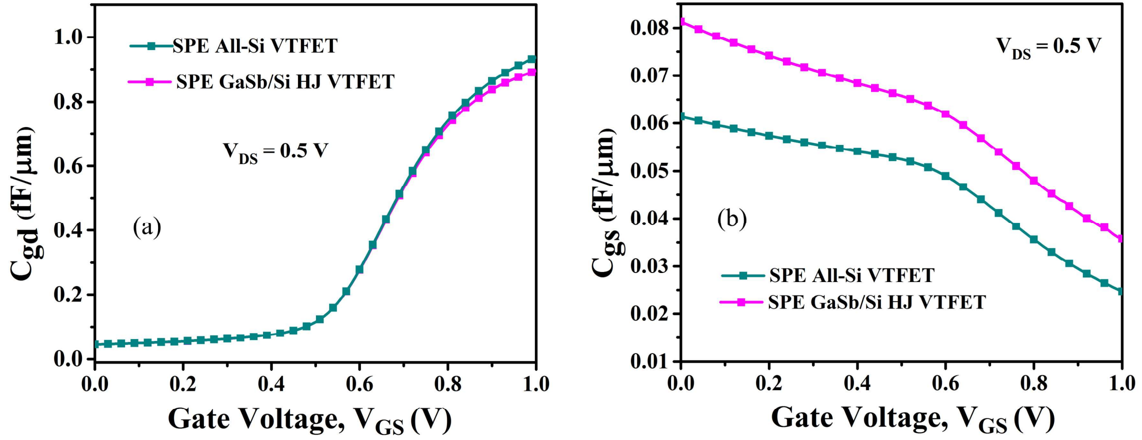

Fig. 2.17: Comparison of (a) gate to drain intrinsic capacitance (C_{gd}), and (b) gate to source intrinsic capacitance (C_{gs}) for SPE All-Si VTFET and GaSb/Si VTFET WP.

Miller capacitance of the device. Figure 2.17 (a), and (b) shows the comparison of the gate-drain intrinsic capacitance (C_{gd}), and gate-source intrinsic capacitance (C_{gs}) respectively. The magnitude of C_{gs} is noted to be very small as compared to C_{gd} for both devices under study.The results in Figs. 2.17(a) and (b) show that SPE GaSb/Si HJ VTFET has lower value of C_{gd} than the corresponding value in SPE All-Si VTFET. However, C_{gs} value is comparatively higher for SPE GaSb/Si HJ VTFET than SPE All-Si VTFET. But as the magnitude of C_{gs} is much lesser than C_{gd}, overall high value of intrinsic gate capacitances are observed for SPE All-Si VTFET than SPE GaSb/Si HJ VTFET. Higher intrinsic capacitances in SPE All-Si VTFET hampers the circuit-level performance as it increases the propagation delays. The cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}) are also considered as important RF figures of merit (FOMs). The cut-off frequency (f_T) is defined as the frequency at which short circuit current gain becomes unity as given in equation (2.1) which has been discussed earlier. Since C_{gs} is very small as compared to C_{gd} in both the VTFETs, the value of f_T is mainly determined by g_m and C_{gd} of the devices. The larger value of f_T as shown in Fig.

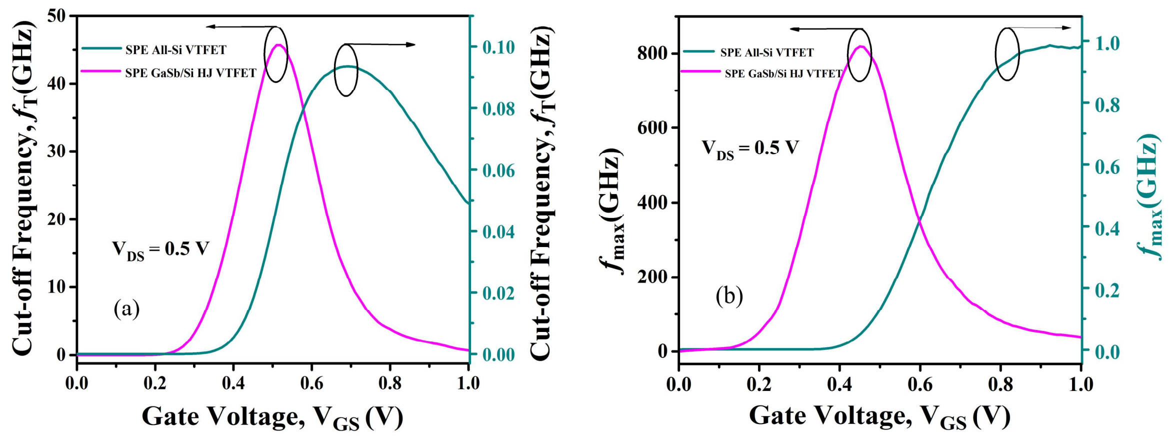

Fig. 2.18: Comparison of (a) cut-off frequency (f_T), and (b) maximum frequency of oscillation (f_{max}) for SPE All-Si VTFET and SPE GaSb/Si HJ VTFET.

2.18(a) by SPE GaSb/Si HJ VTFET than that of SPE All-Si VTFET is attributed to larger value of g_m and lower values of intrinsic gate drain capacitance (C_{gd}) in the SPE GaSb/Si HJ VTFET than that of SPE All-Si VTFET. It is also shown in Fig. 2.18(a) that f_T is initially increased with V_{GS} in both the TFETs. However, it starts to decrease when V_{GS} exceeds a certain value possibly due to the reduction in g_m owing to the mobility degradation at higher V_{GS} [135] as discussed earlier. The values of f_T in SPE All-Si VTFET and SPE GaSb/Si HJ VTFET are 0.09 GHz and 46 GHz respectively. The maximum frequency of oscillation (f_{max}) is the frequency at which the unilateral power gain drops to unity as given in Eq. (2.3). To extract all the Y parameter from Eq. (2.4), f_0 (applied frequency) considered as 1 MHz. Fig. 2.18(b) shows that f_{max} follows the same trend as that of f_T. The SPE GaSb/Si HJ VTFET has the higher value of f_{max} (~800 GHz) than SPE All-Si VTFET (~1 GHz). Gain bandwidth product (GBP) and transit time are also considered as essential RF parameters. The GBP is calculated for a DC gain of 10 as given in Eq. (2.2). GBP indicates the constant gain region of operation of any FET. Fig. 2.19(a) shows that the GBP in SPE GaSb/Si HJ VTFET has the higher value between the two VTFETs under study is because of larger value of g_m and lower

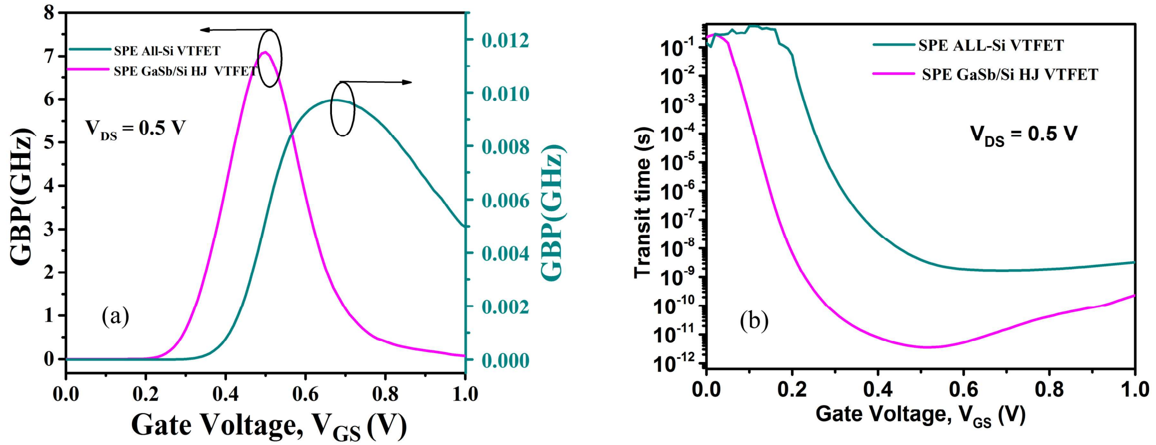

Fig. 2.19: Comparison of (a) gain bandwidth product (GBP), and (b) transit time for SPE All-Si VTFET and SPE GaSb/Si HJ VTFET.

values of C_{gd} in SPE GaSb/Si HJ VTFET than SPE All-Si VTFET. The transit time (τ) represents the time required for the charge carriers to travel from source region to drain region in any MOS transistor. It is expressed in terms of f_T as given in Eq. (2.4) [135]. It can be noted from the above equation that it is inversely proportional to f_T as shown in Fig. 2.19(b) for SPE GaSb/Si HJ VTFET than SPE All-Si VTFET. Clearly, SPE GaSb/Si HJ VTFET is having lower transit time than SPE All-Si VTFET and can be considered for faster switching applications.

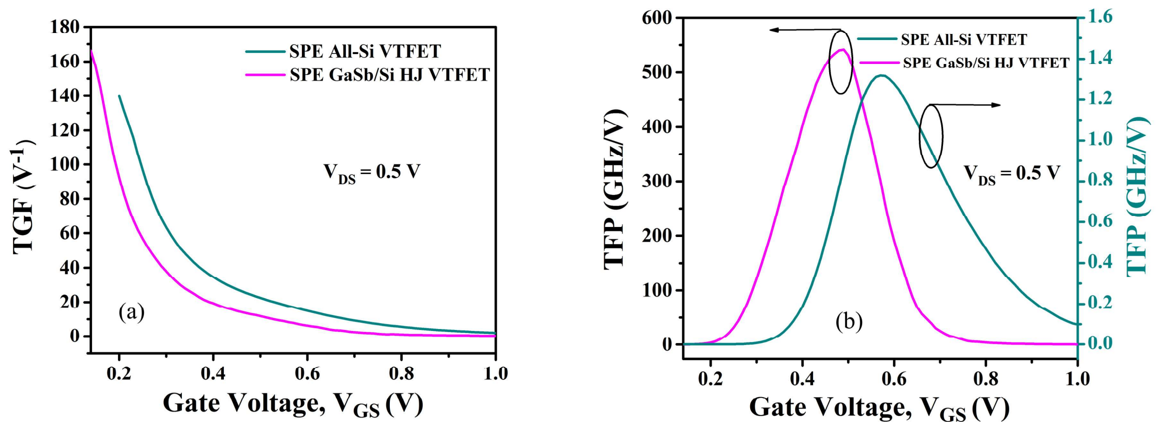

Fig. 2.20: Comparative plot of (a) TGF, and (b) TFP with respect to gate to source voltage(V_{GS}) for SPE All-Si VTFET and SPE GaSb/Si HJ VTFET.

TABLE 2.4

COMPARISON OF DEVICE LEVEL PERFORMANCE PARAMETERS OF THE PRESENTED VTFETS

Parametes	SPE All-Si VTFET	SPE GaSb/Si HJ VTFET
I_{ON} (A/µm)	1.45×10^{-7}	2.068×10^{-5}
I_{OFF} (A/µm)	1.84×10^{-17}	$3.11\text{x}10^{-17}$
I_{ON}/ I_{OFF}	$7.8\text{x}10^{9}$	$6.7\text{x}10^{11}$
Avg. SS (mV/dec)	67	26
V_T (V)	0.8	0.31
g_m (µS/µm)	0.41	66
g_d (µS/µm)	0.009	19
C_{gs} (µS/µm)	0.0248	0.0357
C_{gd} (µS/µm)	0.936	0.895
f_T (GHz)	0.09	46
GBP(GHz)	0.010	7
f_{max}(GHz)	1	800
TGF (V^{-1})	139	165
TFP(GHz)	1.3	541

The transconductance generation factor (TGF) or device efficiency is defined as the capability of a device to convert the current into transconductance. It is a trade-off between power and high-speed operation of any MOS transistors. Fig. 2.20(a) shows the TGF for the presented VTFETs. The formulation related to TGF is given in Eq. (2.5). similarly, TFP which is the product of TGF and f_T as given in Eq. (2.6). The TFP

parameter shown in Fig. 2.20(b) gives a trade-off between bandwidth and power for moderate to high speed operation of both the TFETs under study. Fig. 2.20 reveals that TGF and TFP are higher for SPE GaSb/Si HJ VTFET than SPE All-Si VTFET. The simulated performance parameters of both the vertically grown TFETs under study have been listed in Table-2.4. It is observed that the proposed GaSb/Si staggered heterojunction based vertical TFET (SPE GaSb/Si HJ VTFET) have better DC and RF performance characteristics over the conventional all-Si vertical TFET (SPE All-Si VTFET).

2.5 Conclusion

In this chapter, first device-level performance parameters has been investigated for GaSb/Si heterojuction based vertical TFETs with and without a source pocket. The rigorous TCAD based simulation results show that SPE GaSb/Si HJ VTFET has lower SS (~26 mV/dec), smaller threshold voltage (~0.31 V) and higher I_{ON}/I_{OFF} ratio (7.5×10^{11}) than their corresponding values (of 43 mV/dec, 0.45V and 6.87×10^{11}) of the GaSb/Si HJ VTFET. Both the proposed VTFETs have better I_{ON}/I_{OFF} ratio in the order of 10^{11} than the other staggered heterojunction based TFETs because of a very low OFF state current. The proposed SPE GaSb/Si HJ VTFET has better temperature stability than the GaSb/Si HJ VTFET. The analog/RF analysis shows that the SPE GaSb/Si HJ VTFET has 1.22× g_m, 3.5× f_T, 3.5× f_{max}, 4.3× GBP, 1.79× TGF and 3.6× TFP with respect to g_m, f_T, f_{max}, GBP, TGF and TFP of the GaSb/Si HJ VTFET structure. Our proposed SPE GaSb/Si HJ VTFET device is also shown to have better analog/RF performance parameters than some recently reported results for some non conventional TFET structures. As it has been observed from the results that GaSb/Si heterojunction vertical TFET with source pocket (SPE GaSb/Si HJ VTFET) outperforms the GaSb/Si

heterojunction vertical TFET without source pocket (GaSb/Si HJ VTFET), performance comparison at device-level has been made for SPE GaSb/Si HJ VTFET with an all-Si vertical TFET with source pocket (SPE All-Si VTFET). The comparison based study has been made for SPE GaSb/Si HJ VTFET with SPE All-Si VTFET because of abudant availability of all-Si TFET in IC industry for their fabrication compatibility. Again all the electrical parameters related to device-level performance parameters such as sub-threshold swing (SS), I_{ON}/I_{OFF} ratio, ON-current (I_{ON}), transconductance (g_m), output conductance (g_d), gate to drain intrinsic capacitance (C_{gd}), gate to source intrinsic capacitance (C_{gs}), cut-off frequency (f_T), maximum frequency of oscillation (f_{max}), gain bandwidth product (GBP), transit time (τ), transconductance generation factor (TGF) and transconductance frequency product (TFP) characteristics have been thoroughly investigated for SPE GaSb/Si HJ VTFET with SPE All-Si VTFET. The proposed SPE GaSb/Si HJ VTFET has better SS (below 30 mV/dec), higher I_{ON}/I_{OFF} ratio (in the order of 10^{11}) and lower threshold voltage (below 0.4 V) than the all-Si VTFET structure. The RF figures of merit also shows improved performance for SPE GaSb/Si HJ VTFET than SPE All-Si VTFET. Thus, the superiority in performance of GaSb/Si heterojunction vertical TFET with a highly doped source pocket (SPE GaSb/Si HJ VTFET) over SPE all-Si VTFET earns the avenues for low power and high frequency applications like other III-V/Si heterojunction TFETs.