5

CHAPTER

THREE-PHASE MULTI AC QUASI-Z-SOURCE SERIES-PARALLEL HYBRID CONVERTER TOPOLOGIES FOR MICROGRID APPLICATIONS

5.1 Introduction

As discussed in previous chapter, the idea of the AC/DC hybrid microgrid systems (HMGS) is emerging fast which contains various entities such as distributed renewable resources, energy storage systems and local loads within certain areas. A systematic approach is needed to properly interconnect these entities for proper utilization of the renewable sources and fulfilling the load demand. The concept of diode assisted switched LC quasi-Z-source (q-ZS) series parallel hybrid converters (QSPHCs) are presented in the previous chapter, which is helpful in that interconnections in single-phase HMGS. However, with the expansion of the microgrid it may be required to handle high power applications and three phase load along with DC load. Furthermore, to deal high power application itself will require three-phase supply. In view of that, three-phase system with various level of voltages becomes a mandatory part of hybrid microgrid system. Therefore, the hybrid converters presented in previous chapter cannot meet the requirements, as they are able to supply only single-phase voltages. Many conventional hybrid multi output converters (HMOCs) are in literature addressing these purpose. However, these conventional HMOCs are having several disadvantages such as size, efficiency, shoot through problems etc., which will be discussed in next section.

To cope up the above-mentioned problems, three-phase topologies for diode-assisted switched LC network based multi AC quasi-Z-source series parallel hybrid converters (QSPHCs) are proposed in this chapter to cater three phase load/network for hybrid three-phase microgrid application. The concept of the proposed converters is evolved by an extension of the converters presented in the previous chapter. The proposed topologies have the inherent properties of q-ZS inverter and are capable of giving multiple regulated three-phase AC outputs with one boost DC outputs. The closed loop operations, mathematical modelling, switching stress analysis, steady state and dynamic behavior are presented and discussed in this chapter. The concept is also validated by hardware results of the 2.18 kW and 2.02 kW laboratory

prototypes for parallel and series version of the proposed converters.

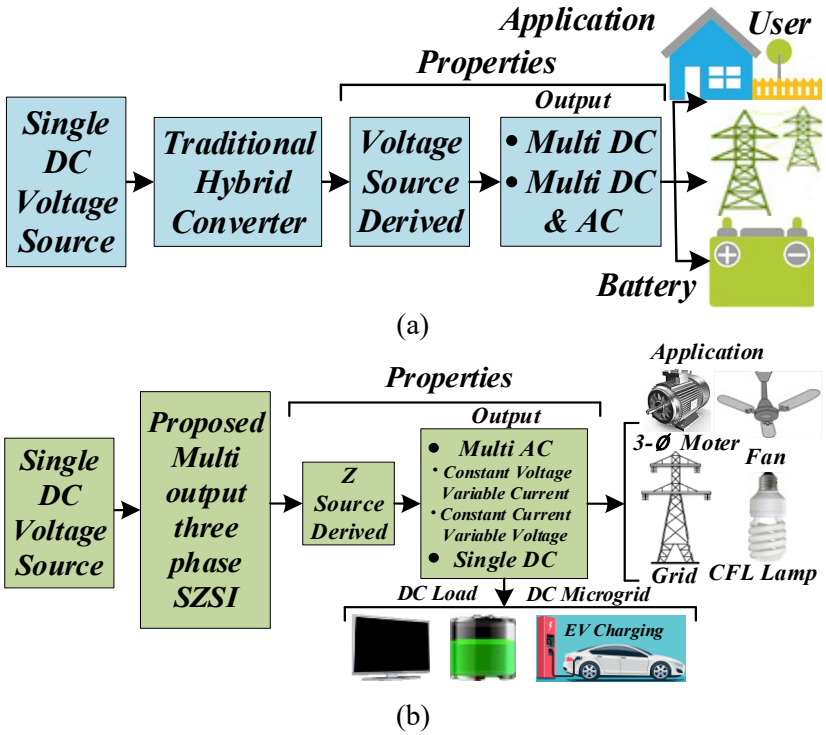


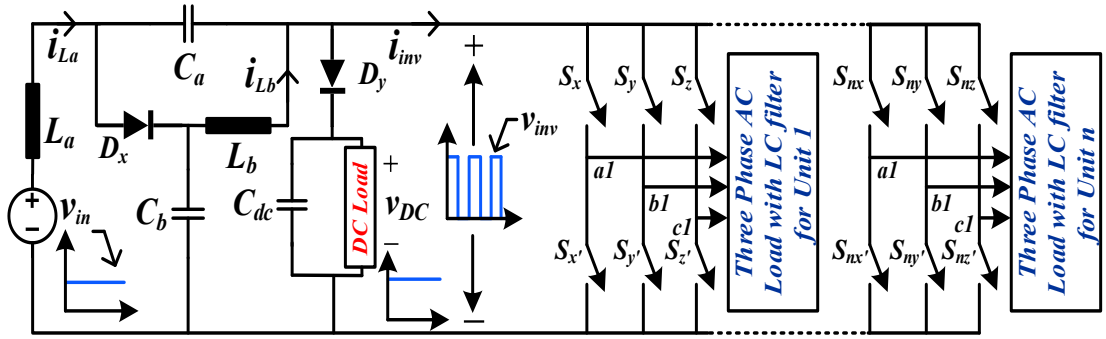
Figure 5.1: Block diagram representation (a) conventional hybrid multi-output converter and (b) proposed topologies.

5.2 Proposed Series-Parallel Topologies

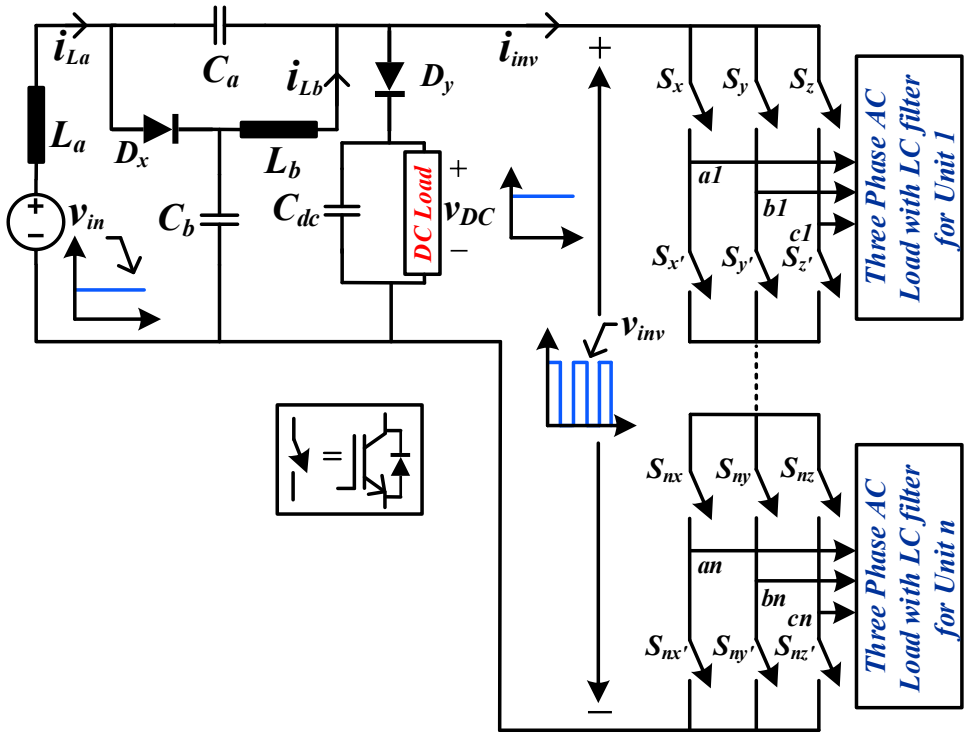
Figure 5.1 (a) and (b) show the representative block diagram for conventional HMOCs and the proposed QSPHC topologies, respectively. As conventional HMOCs are derived from the voltage source inverters, they have only voltage buck capability. In addition, they have inherent shoot-through problem due to the misgating of the switches. It can be observed from Fig. 1(b) that the proposed QSPHCs are able of supplying multiple three-phase AC and one boost DC outputs and as they are evolved from the quasi impedance network and have all the properties of the q-ZSI inherited in them. The proposed QSPHCs can give buck as well as boost AC outputs and have inherent shoot-through protection capability. All the outputs of proposed QSPHCs can be independently regulated to achieve the desired load voltages. The proposed QSPHCs can be used for DC-DC and DC-AC conversions in hybrid microgrids, renewables, uninterrupted power supplies, and residential AC/DC loads.

Figures 5.2(a) and (b) show the circuit diagrams of the proposed topologies in parallel

and series versions. By replacing the inverter switch of q-ZSI by *n* number of parallel or series connected three-phase inverters, the proposed parallel or series version converter topologies are formed. The Z-source network of the proposed topologies of both versions (i.e. parallel and series) use the same number of components (three capacitors, two inductors and two diodes). Figure 5.2(a) depicts the proposed parallel version converter, capable of supplying *n* number of three-phase AC outputs with constant voltage and variable currents along with one boost DC simultaneously. Similarly, the series version can give *n* number of three-phase AC outputs with constant load current along with one boost DC as shown in Figure 5.2(b). In addition, a circuit modification is done by inserting a parallel branch with a filter capacitor (C_{dc}) in series with a diode (D_y) across the switch node voltage of the q-ZS network to obtain the DC output. The proposed topologies are validated for two inverter units ($n = 2$) and one boost DC in this work. All the outputs can be independently regulated as they are working in voltage control mode.



(a)



(b)

Figure 5.2: Shows Proposed topologies in (a) parallel version and (b) series version.

5.3 Operating Principle, Circuit Analysis and Boost Factor of the Proposed QSPHC Topologies

The proposed topologies operate with similar states as traditional ZSIs, shoot-through (ST) and non-shoot-through states.

5.3.1 Shoot-Through State

The operation of proposed parallel and series version and their equivalent circuits during ST state are shown in Figures 5.3(a) and (b), respectively. To illustrate the circuit behaviour during the ST state, the circuit is simplified by replacing inverter units with short circuit switches, as shown in Figure 5.3(c). All the power switches of all the legs are turned ON at the same time, and the inverter bridge operates in the short circuit mode, consequently, the switch node voltage v_{inv} is zero. Diodes D_x and D_y, are reverse-biased and currents through them are zero. The reverse-biased diode D_y prevents a short circuit across the capacitor C_{dc}, and thus protects it against damage in ST condition. The source voltage v_{in} and capacitors C_a and C_b discharge the energy to inductors L_a and L_b. The time interval of this mode is D_sT_s,

where D_s is the ST duty ratio during one switching period T_s. By applying KVL and KCL to Figure 5.3(c), the derived expressions are given in as follows.

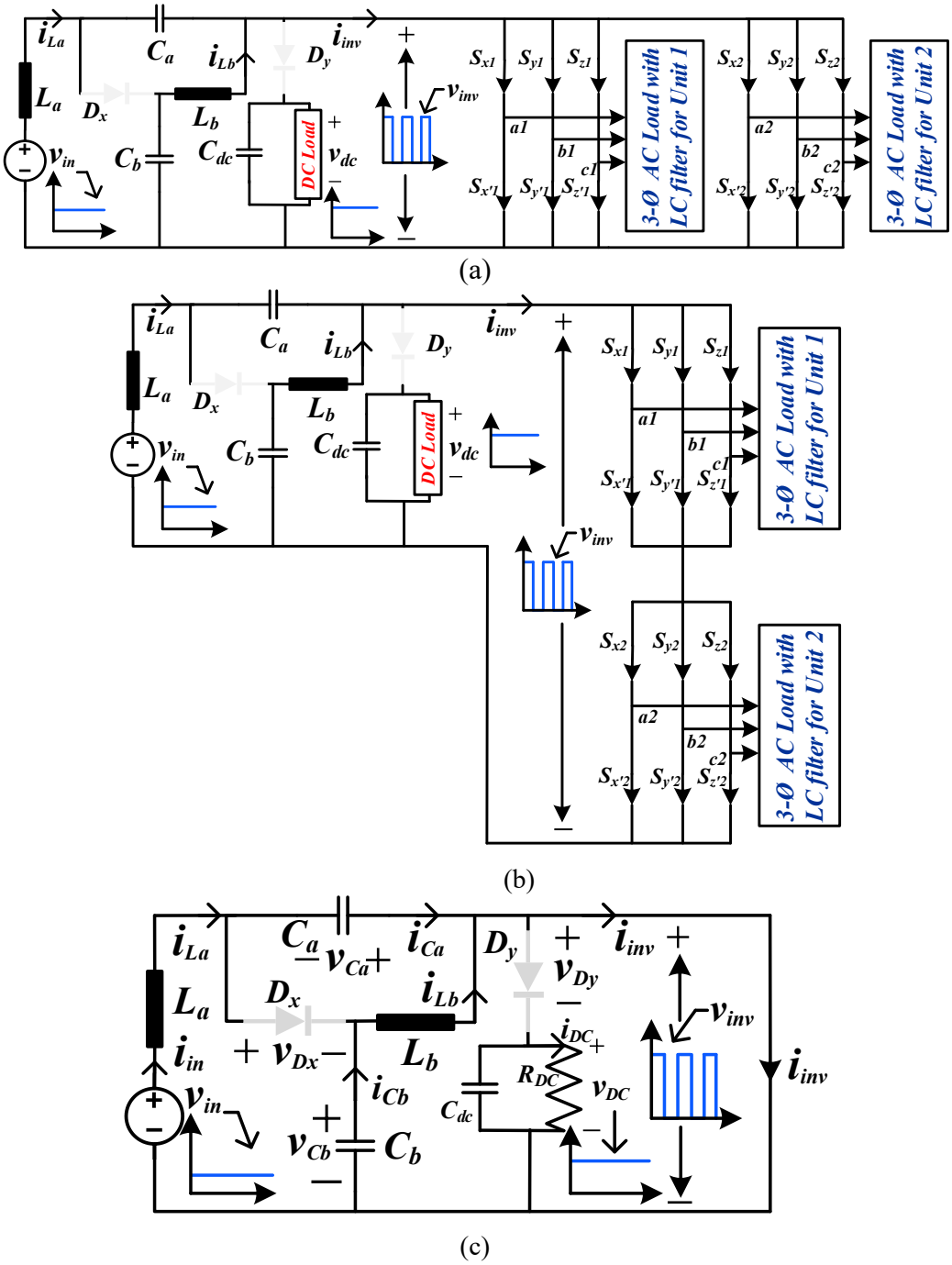
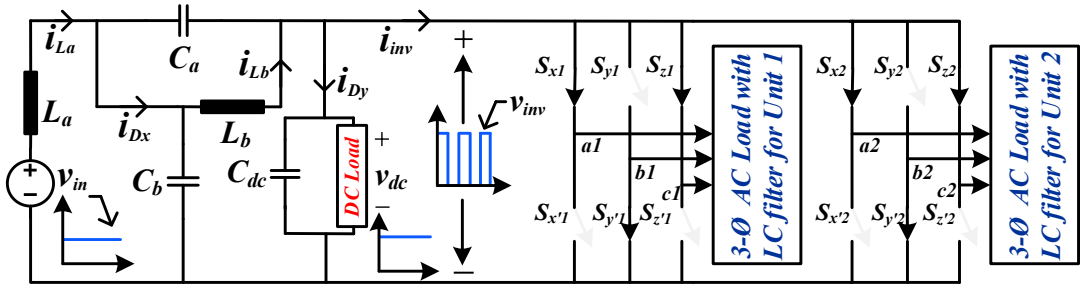


Figure 5.3: Shows the schematic of the (a) proposed parallel, (b) series version converters and (c) equivalent circuit in ST state.

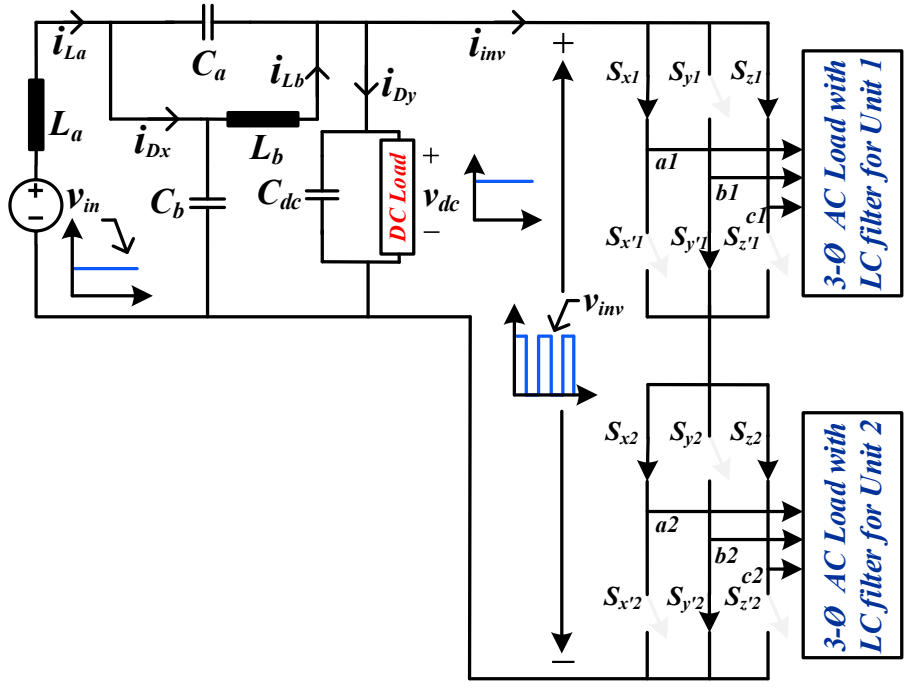
$$\left.\begin{aligned} L_a\frac{di_{La}}{dt} = v_{in} + v_{ca}\,; \quad C_a\frac{dv_{ca}}{dt} = -i_{La}; \\ L_b\frac{di_{Lb}}{dt} = v_{cb}\,; \quad C_b\frac{dv_{cb}}{dt} = -i_{Lb}\,; \\ v_{inv} = 0\,; \quad C_{dc}\frac{dv_{cdc}}{dt} = -i_{DC} = -\frac{v_{DC}}{R_{DC}}\,; \\ v_{Dx} = v_{ca} + v_{cb}\,; \quad i_{Dx} = i_{Dy} = 0\,; \end{aligned}\right\} \tag{5.1}$$

5.3.2 Non-Shoot-Through State

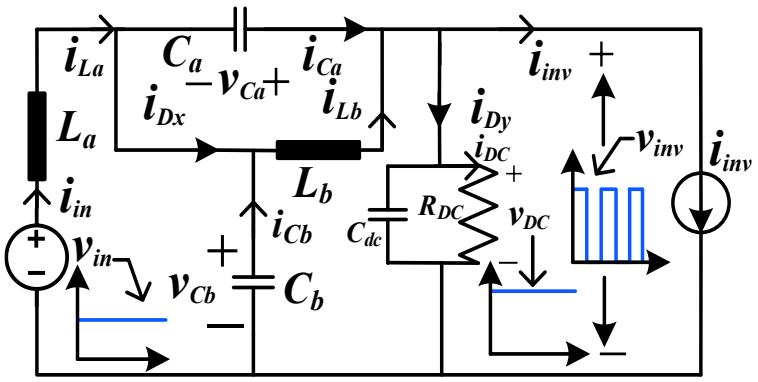
The operation of the proposed parallel and series version topologies, and their equivalent circuits during non-shoot-through (NST) state which is the power state of the three-phase QSPHCs are displayed in Figures 5.4(a) and (b), respectively. Figure 5.4(c) depicts the corresponding circuit diagram in the NST state. The current source (i_{inv}) with a potential v_{inv} represents the three-phase inverter units. The voltages across the diodes D_x and D_y are zero since they are forward biased. In this state, the inductors L_a and L_b discharge energy and capacitors C_a and C_b store it, and the dc-link voltage v_{inv} is not zero. This operating mode's time interval is $(1\text{-}D_s)T_s$. The following expression are derived by applying KVL and KCL in Figure 5.4(c).



(a)



(b)



(c)

Figure 5.4: Show the schematic of the (a) proposed parallel, (b) Proposed series version converters and (c) equivalent circuit in NST state.

$$\left.\begin{aligned} L_a \frac{di_{La}}{dt} = v_{in} - v_{cb}\ ;\ C_a \frac{dv_{ca}}{dt} = i_{La} - i_{dx}\ ; \\ L_b \frac{di_{Lb}}{dt} = -v_{Ca}\ ;\quad C_b \frac{dv_{cb}}{dt} = i_{Lb} - i_{dx}\ ; \\ v_{inv} = v_{Ca} + v_{cb}\ ; C_{dc} \frac{dv_{cdc}}{dt} = i_{Dy} - i_{DC}\ ; \\ v_{Dx} = v_{Dy} = 0\ ;\ i_{Dx} = i_{La} + i_{Dy} - i_{inv}\ ; \end{aligned}\right\} \tag{5.2}$$

Based on the flux balance property of L_a and L_b, the average inductors voltage in steady state over one switching period T_s is zero. Thus, from (5.1) and (5.2) we have

$$\left.\begin{aligned} D_s(v_{in} + v_{Ca}) + (1 - D_s)(v_{in} - v_{Cb}) = 0 \\ D_s(v_{Cb}) + (1 - D_s)(-v_{Ca}) = 0 \end{aligned}\right\} \tag{5.3}$$

Solving (5.3), the capacitor voltage v_{Ca}, v_{Cb} and the peak switch node voltage v_{inv} of the proposed topology can be derived as

$$\left.\begin{aligned} v_{Ca} = \frac{D_s}{1-2D_s} v_{in}\ ;\ v_{Cb} = \frac{1-D_s}{1-2D_s} v_{in}\ ; \\ v_{inv} = v_{DC} = \frac{1}{1-2D_s} v_{in}\ ; \end{aligned}\right\} \tag{5.4}$$

Similarly, according to the charge balance principle, the average capacitor currents of C_a and C_b in steady-state over one switching period T_s is zero. Therefore, from (5.1) and (5.2)

$$\left.\begin{aligned} D_s(-i_{La}) + (1 - D_s)(i_{La} - i_{dx}) = 0 \\ D_s(-i_{Lb}) + (1 - D_s)(i_{Lb} - i_{dx}) = 0 \end{aligned}\right\} \tag{5.5}$$

From (5.5), the inductor currents i_{La} and i_{Lb} are obtained as

$$i_{La} = \frac{(1-D_s)}{(1-2D_s)} i_{dx}\ ;\ i_{Lb} = \frac{(1-D_s)}{(1-2D_s)} i_{dx} \tag{5.6}$$

From (5.4), the DC boost factor (B) is expressed as

$$B = \frac{\hat{v}_{inv}}{v_{in}} = \frac{1}{1-2D_s}. \quad (5.7)$$

From (5.7), as the shoot-through duty ratio (D_s) increases, the denominator term (1-2D_s) decreases and consequently the boost factor B increases in a rectangular hyperbolic manner (Figure 5.5(a)) and finally becomes infinite at D_s = 0.5.

The peak-phase output voltage ($\hat{v}_{AC}$) of the three-phase inverter is

$$\widehat{(v_{AC})}_{fundamental} = \hat{v}_{AC} = \frac{m_a}{2} v'_{inv} = \frac{m_a}{2}\left(\frac{1}{1-2D_s}\right) v_{in} \quad (5.8)$$

$$\widehat{(v_{AC})}_{fundamental} = \hat{v}_{AC} = \frac{m_a}{2} v'_{inv} = \frac{m_a}{2}\left(\frac{1}{2m_a-1}\right) v_{in} \quad (5.9)$$

where v'_{inv} is the input voltage of each converter unit and is equal to v_{inv} and $v_{inv}/2$ for parallel and series versions respectively, and m_a is the modulation index of the inverter.

The modulation index (m_a) controls the inverter output voltage. The ratio of peak output voltage ($\hat{v}_{AC}$) to the DC input voltage (v_{in}) is known as gain (G) of the three-phase inverter in terms of m_a and D_s are given by

$$G = \frac{\widehat{(v_{AC})}_{fund}}{v_{in}} = \frac{m_a}{2}\left(\frac{1}{1-2D_s}\right) \quad (5.10)$$

$$G = \frac{\widehat{(v_{AC})}_{fund}}{v_{in}} = \frac{m_a}{2}\left(\frac{1}{2m_a-1}\right) \quad (5.11)$$

From (5.10) it is clear that the AC gain (G) is directly proportional to modulation index (m_a) and inversely proportional to D_s. The value of G increases as m_a increases at constant D_s. The value of D_s must be less than 0.5, because at D_s = 0.5, G becomes infinite. The gain of the proposed topologies is the same as the gain of conventional q-ZSI. The expression given in (5.11) represents the relation between G and m_a; and as m_a increases, G also increases. The value of m_a cannot be equal to 0.5, because at m_a = 0.5, G becomes infinite. For better performance, high efficiency and ripple-free sinusoidal AC output of the proposed topologies, the value of D_s should be small and m_a should be large.

In the hybrid PWM used in the proposed topologies, m_a and D_s are related as follows.

$$D_s + m_a \leq 1 \quad (5.12)$$

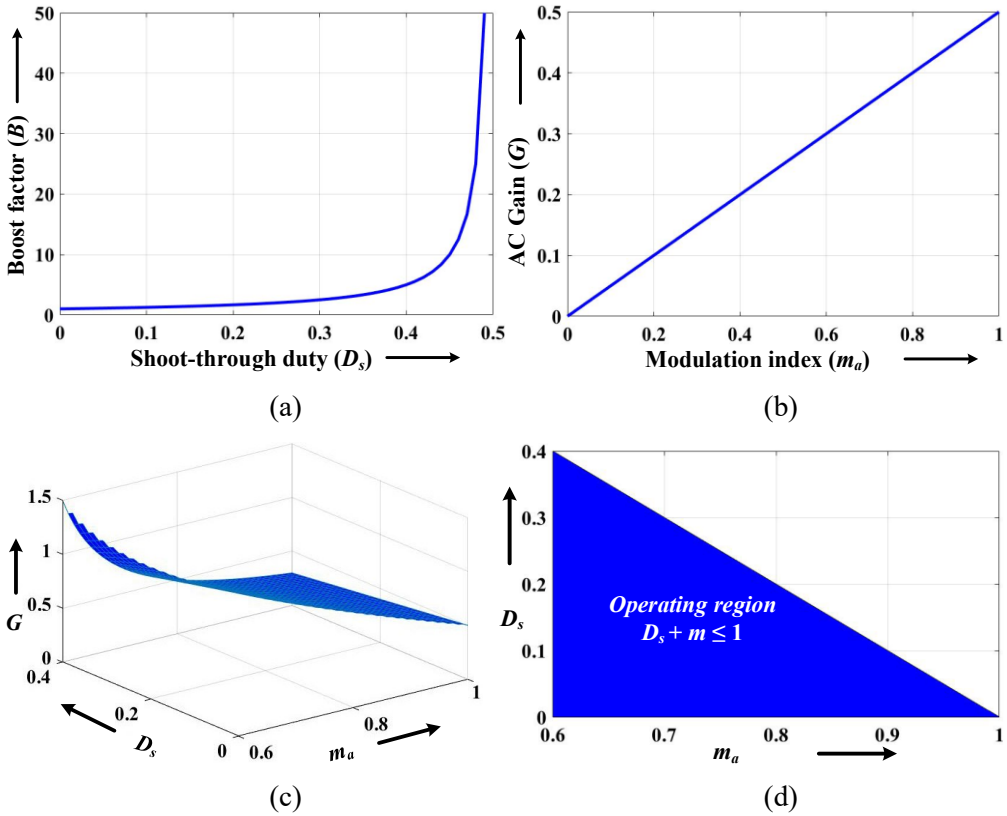


Figure 5.5: Plots among B, D_s, m_a and G. (a) the plot between G and m_a, (b) graph between B and D_s, (c) 3d-plot between AC voltage gains (G), D_s and m_a and (d) operating region of the proposed converter topologies.

5.4 AC and DC Power Expression of the Proposed Topologies

The following subsections give the AC and DC power expressions for the parallel and series versions of the proposed topologies with two inverter modules.

5.4.1 Proposed Parallel Version Topology

The input voltage for both the inverter units in the parallel version are same and equal to v_{inv}. For the same reference voltages (v_{ref}), the peak AC voltages ($\hat{v}_{AC1}$ and $\hat{v}_{AC2}$) are equal, as v_{inv} for both inverter units are equal and expressed by (5.8). The peak AC voltages $\hat{v}_{AC1}$ and $\hat{v}_{AC2}$ are different for different v_{ref} to the inverter modules. Reference voltage v_{ref} is the peak value of the inverter unit's required AC output voltage ($\hat{v}_{AC}$). For both the converters, the gain G is same and expressed by (5.10) and (5.11).

From (5.8), the rms AC output voltage is given as

$$v_{AC,rms} = \frac{\hat{v}_{AC}}{\sqrt{2}} = \frac{GV_{in}}{\sqrt{2}} = \frac{m_a}{2\sqrt{2}}\left(\frac{1}{1-2D_s}\right)v_{in} \tag{5.13}$$

The three-phase AC power output ($P_{3\text{-}\emptyset}$) of both units at the same v_{ref} is

$$P_{3-\emptyset} = 6\frac{v_{AC,\text{rms}}^2}{R_{\text{AC}}} = 6\frac{{m_a}^2\, B^2\, v^2 in}{8\, R_{\text{AC}}} \tag{5.14}$$

Similarly, the three-phase AC power output $P_{3\text{-}\emptyset}$ of both units at different v_{ref} is

$$P_{3-\emptyset} = 3\frac{({m_{a1}}^2 + {m_{a2}}^2\ )\, B^2\ v^2 in}{8\, R_{\text{AC}}} \tag{5.15}$$

where m_{a1} and m_{a2} are the modulation indices of inverter units 1 and 2, respectively and R_{AC} is the AC load resistance.

The DC output power P_{DC} of the proposed topology in parallel version is

$$P_{DC} = \frac{v_{DC}^2}{R_{DC}} = \frac{v_{in}^2}{R_{DC}(1-2D_s)^2} \tag{5.16}$$

where R_{DC} is the DC load resistance of the proposed topologies. It is clear from (5.15) and (5.16) that three-phase power outputs ($P_{3\text{-}\emptyset}$) depend on both m_{a} and D_{s}, whereas the DC output power P_{DC} depends on D_{s} only.

5.4.2 Proposed Series Version Topology

In a series version with two units, the dc-link voltage (v_{inv}) is equally divided across the inverter units for a balanced AC load. The peak AC voltages ($\hat{v}_{\text{AC1}}$ and $\hat{v}_{\text{AC2}}$) are equal for the same reference (v_{ref}) and from (5.8) is given as

$$\hat{v}_{\text{AC1}} = \hat{v}_{\text{AC2}} = \frac{m_a}{2}\frac{v_{\text{inv}}}{2} = \frac{m_a}{4}\left(\frac{1}{1-2D_s}\right) v_{in} \tag{5.17}$$

The rms AC voltage ($v_{\text{AC, rms}}$) for both the units is expressed as

$$v_{\text{AC,rms}} = \frac{\hat{v}_{\text{AC}}}{\sqrt{2}} = \frac{m_a}{4\sqrt{2}}\left(\frac{1}{1-2D_s}\right) v_{in} \tag{5.18}$$

The three-phase AC power output $P_{3\text{-}\emptyset}$ of a single unit is given by the following expression

$$v_{\text{AC,rms}} = \frac{\hat{v}_{\text{AC}}}{\sqrt{2}} = \frac{m_a}{4\sqrt{2}}\left(\frac{1}{1-2D_s}\right) v_{in} \tag{5.19}$$

The three-phase AC power output ($P_{3-\emptyset}$) of both the units is given as

$$P_{3-\emptyset} = 6\frac{v_{\text{AC},\text{rms}}^2}{R_{\text{AC}}} = 6\frac{{m_a}^2\, B^2\, v^2 in}{32\, R_{\text{AC}}} \tag{5.20}$$

The DC output power P_{DC} expression of the series mode converter is the same as that of the parallel mode as expressed in (5.16).

The peak AC output voltage $\hat{v}_{AC}$ is directly proportional to m_a of the inverter and equal to a peak value of v_{ref} in voltage control mode. As the reference voltage v_{ref} is increased, m_a increases due to which output power increases and vice-versa.

5.5 Voltage/Current Stresses of the Components and Cost Analysis of the Proposed QSPHC Topologies

The voltage and current stresses of each component of the proposed topologies are given in Table 5.1, which helps in deciding the criteria to select the rating of the components according to the modes (series or parallel) and the number of inverter AC output units in the converter.

For the parallel mode, as the number of inverter units increases, current stresses on inductors L_a, L_b and diode D_x increase because the input and switch node currents (i_{in} and i_{inv}) increase. However, the voltage stresses on capacitors C_a, C_b and diodes depend upon ST duty ratio D_s. Hence, for constant dc-link voltage operation, the ST duty ratio D_s is constant and subsequently the voltage stresses are constant.

TABLE 5.1
VOLTAGE AND CURRENT STRESSES OF THE PROPOSED CONVERTERS

Parameters	Voltage Stresses	Parameters	Current Stresses
C_a	$\frac{(D_s)\, v_{in}}{(1-2D_s)}$	L_a	i_{in}
C_b	$\frac{(1-D_s)\, v_{in}}{(1-2D_s)}$	L_b	$\frac{(1-D_s)\, i_{inv}}{(1-2D_s)}$
C_{DC}	$\frac{v_{in}}{(1-2D_s)}$	D_x	$\frac{i_{pn}}{(1-2D_s)}$
D_x , D_y	$\frac{v_{in}}{(1-2D_s)}$	D_y	$\frac{i_{dc}}{(1-D_s)}$

In case of series mode, as the number of inverter units increases, i_{in} and i_{inv} are same for all the inverter units. Hence, the current stresses remain constant. However, as v_{inv} increases according to number of inverter units, ST duty ratio D_s also increases. Consequently, voltage stresses of capacitors and diodes increase.

Figures 5.6(a) and (b) show the variation of voltage and current stress with respect to D_S. From (5.21), as D_S increases, the voltage stresses across the capacitors (C_a and C_b) and diodes (D_x and D_y) increase. Similarly, the current stresses of inductors (L_a and L_b) increase according to (5.6). The voltage across C_a, C_b, V_{Dx} and V_{Dy} are given as

$$V_{Ca} = \frac{(D_S)\, v_{in}}{(1-2D_S)},\ V_{Cb} = \frac{(1-D_S)\, v_{in}}{(1-2D_S)},\ V_{Dx} \text{ and } V_{Dy} = \frac{v_{in}}{(1-2D_S)} \tag{5.21}$$

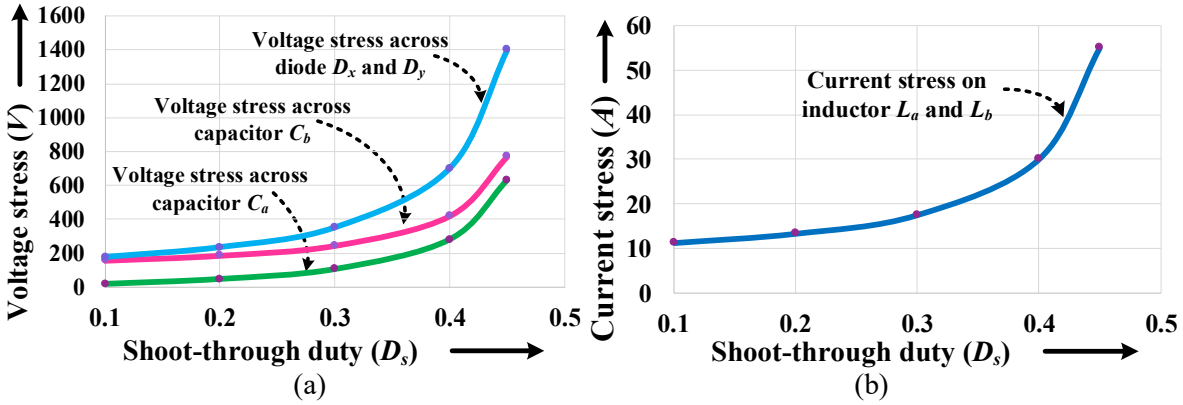


Figure 5.6: Shows (a) diodes, capacitors voltage and (b) inductors current stresses with respect to ST duty cycle (D_s) of the proposed series and parallel topology.

With the increase in the stress of the front-end components (inductors and capacitors of the impedance network), the rating increases, and therefore cost of the individual component increases. However, as the front-end component counts are fixed irrespective of the number of units, the overall cost of the proposed topologies for more number of units is less in comparison to the same number of converters connected independently, even for a three-phase loads. Therefore, it is justified to use the proposed topologies with multiple units for practical applications.

Cost analysis of two single unit individual converters and the proposed converters with two units connected in parallel for same power ratings of 2.18 kW are carried out as shown in

Tables 5.2 and 5.3, respectively. The total number of components (passive elements and switches) is 26 and the cost is $130.36 in case of two single unit individual converters.

TABLE 5.2
COST OF TWO SINGLE UNIT INDIVIDUAL CONVERTERS

Component Name	Item No/ Rating	Price per component	No of components required	Total price (in $)
Inductors	3.5 mH, 15 A	7.15	4	28.6
Capacitors	470 µF, 250 V	4.66	6	27.96
Diodes	40EPF06	4.56	4	18.24
Inverter switches	FGH40T65UPD	4.63	12	55.56
Total number of components			26	---
			Total Cost	130.36

TABLE 5.3
COST OF PROPOSED CONVERTERS WITH TWO UNITS

Component Name	Item No/Rating	Price per component	No of components required	Total price (in $)
Inductors	5.3 mH, 20 A	12.66	2	25.32
Capacitors	470 µF, 400 V	8.28	3	24.84
Diodes	DWD10G120C5 XKSA1	5.51	2	11.02
Inverter switches	FGH40T65UPD	4.63	12	55.56
Total number of components			19	---
			Total Cost	116.74

However, in the case of proposed converter with two units, the number of components is 19 and the cost is $116.74. The number of components are less in the proposed topologies with two units, because the front-end passive components are fixed. It is clear from Tables 5.2 and 5.3 that for proposed converters with two units, the price per component is high due to increased stress/rating. However, the overall cost is less as compared to its counterparts, i.e. two single unit individual converters.

5.6 Comparative Analysis Amongst Existing Topologies and Proposed QSPHC Topologies

The proposed topologies are compared with the closely related topologies in Table 5.4. The table demonstrates some meaningful merits of the proposed topologies in comparison to the existing converter topologies.

TABLE 5.4

COMPARISION AMONG PREVIOUSLY REPORTED AND PROPOSED TOPOLOGIES

Reference	No. of Outputs	Advantages	Disadvantages
[31]	3 (Extendable)	✓ Multiple DC outputs ✓ One step-up DC output ✓ Other outputs are step down DC	× Unable to produce AC × Not suitable for high power application
[39]	2	✓ Produces more than one DC outputs ✓ Uses only one power switch to achieve high efficiency ✓ Soft switching and voltage clamping used to reduce switching and conduction losses	× Unable to produce AC output × High number of passive elements- four inductors, four diodes and three capacitors for two DC outputs × Power density is low
[43]	2	✓ Simultaneous two buck and boost DC outputs ✓ Less voltage stress across the switches due three level structure	× No AC output × Number of switches are high- for two DC outputs, four switches are required
[44]	2	✓ Zero voltage switching ✓ Less switching loss ✓ One buck and one boost DC outputs simultaneously	× No AC output × Large no of components-four inductors, three switches four capacitors and two diodes for two DC outputs × Low power density
[49]	2	✓ High step up voltage gain converter ✓ Produces two DC outputs at different voltage level ✓ Continuous input current with low ripple due to use of interleaved connection	× No AC output × Large number of inductor, coupled inductor and capacitors are used- four inductor, four coupled inductors and nine capacitors are used for two DC outputs. × Low power density
[60]	2	✓ Inherent ST protection ✓ Continuous input current ✓ Two simultaneous DC and AC outputs	× No multiple AC output × Only single phase AC output. × Not suitable for high power application
[64]	2	✓ Inherent ST protection ✓ Two simultaneous DC and AC outputs ✓ Can operate for condition (D+M) ≥ 1, M is AC modulation index, D is duty ratio	× No multiple AC output × Only single phase AC output. × Closed loop control is not implemented × Not suitable for high power application
[65]	2	✓ Minimum phase converter ✓ Continuous input current ✓ Two simultaneous AC and boost DC outputs	× No multiple AC output × No three-phase output × Due to damping resistance losses are increased
Proposed Topologies	3 (Extendable)	✓ Multiple three-phase AC with one boost DC outputs simultaneously ✓ Less no of passive component (two	Remark: The limitations given above in the previous topologies have been taken

		inductors and two capacitors) irrespective of number of AC outputs ✓ Higher power density ✓ Suitable for high power application. ✓ Inherent ST protection ✓ All the outputs are independently regulated	care of in the proposed converters.

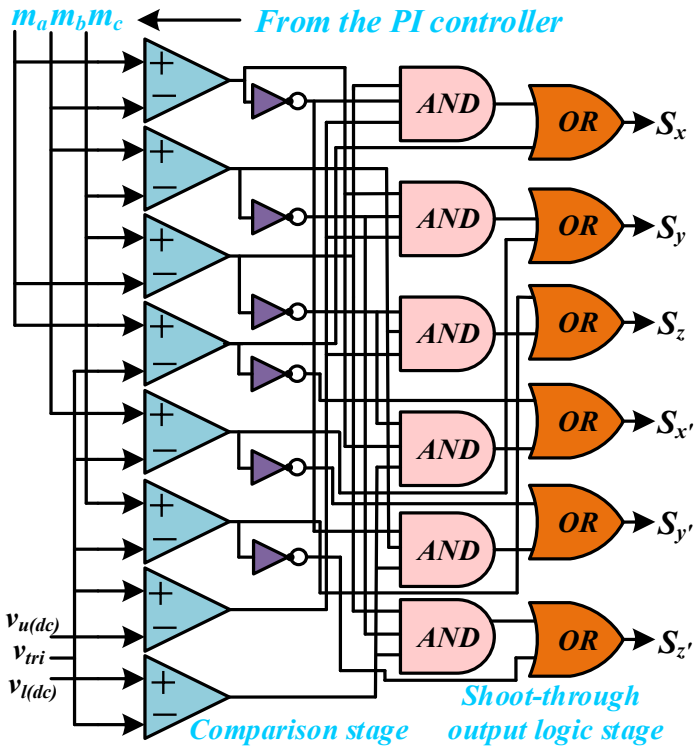
5.7 Control Strategy for the Proposed Topologies

For the proposed topologies, the control strategy to control the DC/AC power flow is explained in the following subsections.

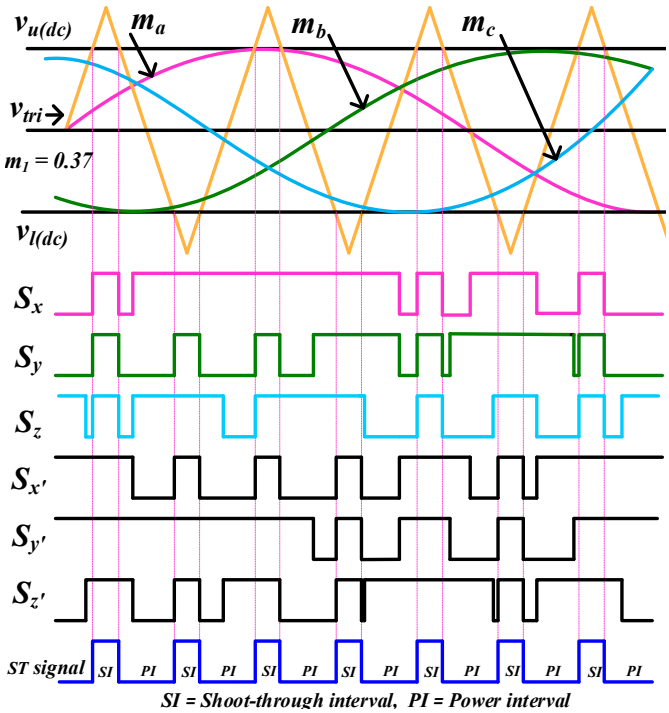
5.7.1 Hybrid PWM Scheme for the Proposed Topologies

A hybrid sinusoidal pulse width modulation (SPWM) scheme with constant frequency shoot-through is implemented on the DSP board to control the proposed topologies. Using the hybrid PWM modulation method, the switching signals for NST and ST states. The complete modulation scheme of the proposed switching signal topology is shown in Figure 5.7. The modulation scheme's logic diagram is shown in Figure 5.7(a) and the corresponding switching signals are shown in Figure 5.7(b). For switch 1 to 6 of unit 1, s_x to $s_{z'}$ are the corresponding switching signals. By comparing the reference triangular waves with three-phase modulating sinusoidal signals (m_a, m_b and m_c) and their complementary signals, the switching signals are generated. The magnitudes of the modulating sinusoidal signals are as per the reference AC output voltages. The ST periods are decided by comparing the reference triangular waves with two constant *dc* signals (upper $v_{u(dc)}$ and lower $v_{l(dc)}$), the magnitudes of which are decided by the required DC output voltage. When the triangular carrier wave is higher than the upper constant *dc* signal $v_{u(dc)}$ or less than the lower *dc* signal $v_{l(dc)}$, ST signals are generated. In the ST condition, switches of all the legs are ON at the same time. The signal for the first leg of the inverter is produced by comparing m_a and its complement with the triangular carrier wave. With the addition of the ST switching signals, signals s_x and $s_{x'}$ are generated for the upper and lower first leg switches, respectively. Comparing the carrier wave with m_b and m_c, respectively, as well as *dc* modulating signals, produces switching signals for the second and third legs (s_y,

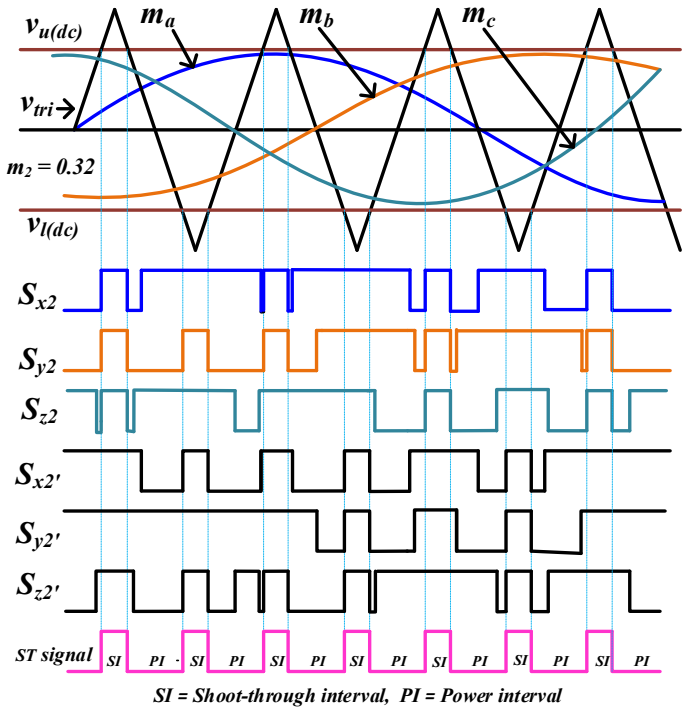
$s_{y'}$) and (s_z, $s_{z'}$). Figure 5.7(b) shows the PWM signals with the modulation index m_a = 0.3684 and D_s = 0.3158 for inverter unit 1 (Figure 12(d)) with v_{ref} = 70 V and v_{dcref} = 380 V. The PWM signals with m_a = 0.2631 and D_s = 0.3158 for inverter unit 2 with v_{ref} = 50 V and v_{dcref} = 380 V are shown in Figures 5.7(c) and 15(a).



(a)



(b)



(c)

Figure 5.7: Modulation scheme for the proposed topologies (a) PWM control logic, (b) PWM signals of unit 1 with v_{ref} = 70 V (m_1 = 0.37) and (c) unit 2 with v_{ref} = 60 V (m_2 = 0.32).

From (5.8), $\hat{v}_{AC}$ is directly proportional to m_a and in the voltage mode control, the $\hat{v}_{AC}$ is equal to v_{ref}. Therefore, by varying v_{ref}, m can be varied and consequently the output power can be varied. If the proposed topologies use two inverter units, it is possible to operate both units independently by giving them separate switching signals with a single DSP kit as shown in Figures 5.7(b) and (c).

5.7.2 Closed-loop Control Strategy for the Proposed Topologies

The block diagram of the closed-loop control strategy for the proposed topologies is shown in Figure 5.8. The three-phase output voltages (v_a, v_b and v_c) of the inverter units are controlled by a PI compensator using *d-q* control mode. Using the Parks and Clarks transformations, the sensed AC output voltages are transformed into their *d-q* components and then compared with the *d-q* components of the reference voltage. Finally, from the controller, sinusoidal modulating signals (m_a, m_b and m_c) are obtained. The required DC voltage (v_{dcref}) is compared with the actual DC voltage and the error is passed through the PI controller.

Consequently, DC modulating signals are obtained for ST cycles. By using these modulating signals with a triangular signal for PWM operation, the switching signals are produced.

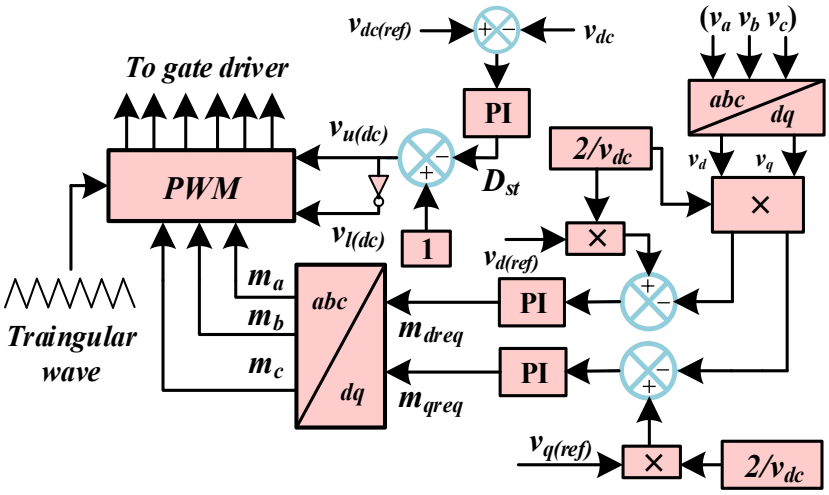


Figure 5.8: The control scheme for the proposed topologies.

5.7.3 PWM Signals and Operation of the Proposed Topologies with Multiple Units for Different Voltages and Frequencies

The proposed topologies provide full flexibility in the operation of the multiple converter units. The converter units operate in the same fashion in the proposed scheme as if they are operating individually at different voltages and frequencies. Figure 4.9 shows the switching signals for a sample case where, the requirement of DC output voltage is 380 V, inverter unit 1 voltage is 70 V (peak), 50 Hz and inverter unit 2 voltage is 60 V, 60Hz. To obtain 380 V DC output, the shoot-through duty ratio (D_s = 0.3289) is kept same for both the units. The output voltage of 70 V (peak), 50 Hz for unit 1 is obtained by comparing the reference triangular signals with the three-phase sinusoidal modulating signals of m = 0.37 and frequency = 50 Hz. On the other hand, for the unit 2, the output voltage of 60 V (peak), 60 Hz is obtained by comparing the reference signal with the sinusoidal modulating signals of m = 0.32 and frequency = 60 Hz. In this way, the converters are operated at different voltages and frequencies.

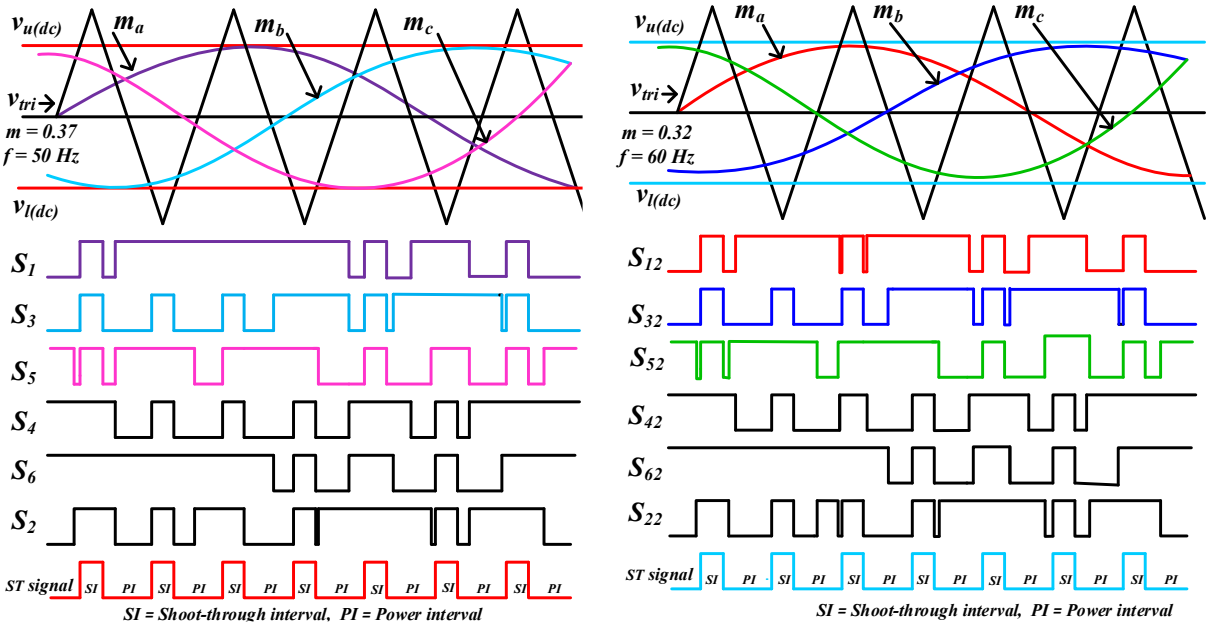


Figure 5.9: Switching signals for (a) unit 1 with output voltages 70 V (peak), 50 Hz (b) unit 2 with output voltage 60 V (peak), 60 Hz.

5.8 Verification of the Proposed QSPHC Topologies

To check the effectiveness of the proposed topologies, they are validated experimentally for n = 2 (i.e., for two simultaneous AC and one DC outputs). Figure 5.10 depicts a block diagram of the overall implementation of the proposed topologies. A hardware prototype is fabricated using the parameters given in Table 5.5. The hybrid PWM signals to control the switches of the proposed topologies are generated by a 32 bit TMS320F28335 DSP operating with a clock frequency of 150 MHz. The full steady-state and dynamic results of the proposed parallel and series version topologies are shown in subsequent subsections 5.8.1 and 5.8.2. Figure 5.11 provides a photograph of the experimental setup developed in the laboratory to test proposed topologies. The three-phase AC outputs are loaded with six 20 Ω loads in a Y-connection and DC output is loaded with 100 Ω.

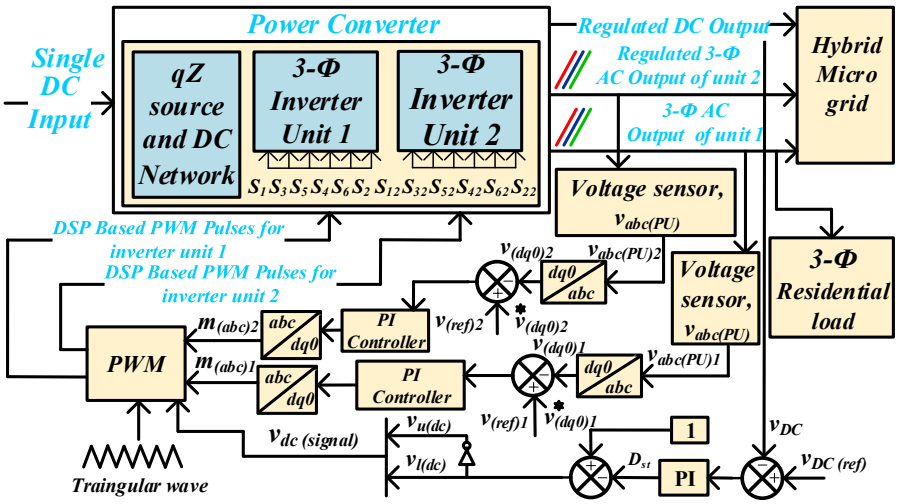


Figure 5.10: Overall implementation of the proposed topologies.

TABLE 5.5 COMPONENTS LIST OF THE PROPOSED TOPOLOGIES

Parameter	Rating
Power (P)	2.18 kW (for parallel)
	2.02 kW (for series)
Input voltage (v_{in})	140 V (for parallel)
	140 V (for series)
Inductor ($L_1 = L_2$)	5 mH
Capacitor ($C_1 = C_2 = C_{DC}$)	470 μF
Switching frequency (f_s)	10 kHz
DC load resistance (R_{DC})	100 Ω
AC load resistance (R_{AC})	20 Ω
Filter inductor (L_f)	2 mH
Filter capacitor (C_f)	10 μF

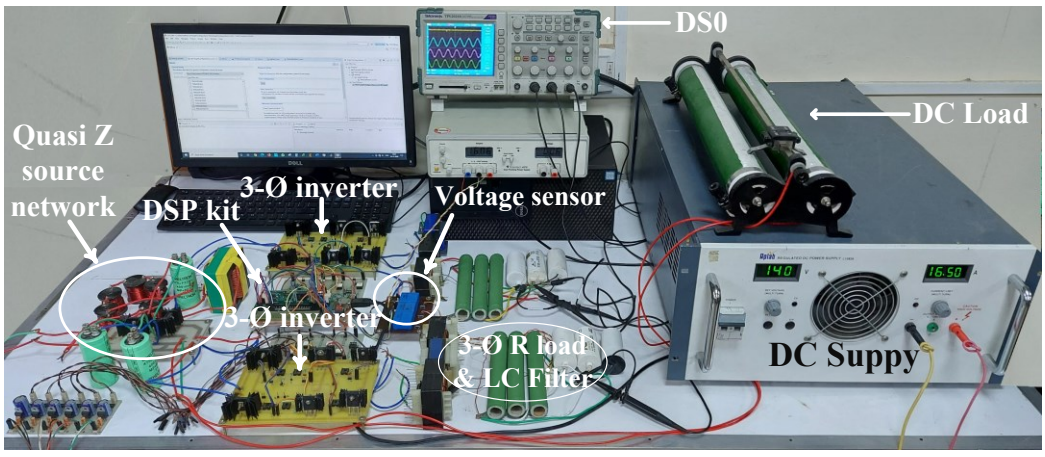


Figure 5.11: Photograph of the experimental setup.

5.8.1 Verification of Proposed Parallel Version Converters (Regulated Dual AC and Single DC Outputs)

In the parallel version, the proposed topology is tested for 2.18 kW with DC power P_{DC} = 1444 W and three phase AC power P_{AC} = 735 W.

5.8.1.1 Steady-State Results of the Proposed Parallel Version Converter

Figure 5.12 shows the simulation results and Figures 5.13, 5.14 and 5.15 show the hardware results for the steady-state response of the parallel version of the proposed topologies for AC and DC voltage reference v_{ref} = 70 V (peak AC for both units) and v_{dcref} = 380 V, respectively**.** The DC load resistance is 100 Ω and the AC load resistance for both the inverter

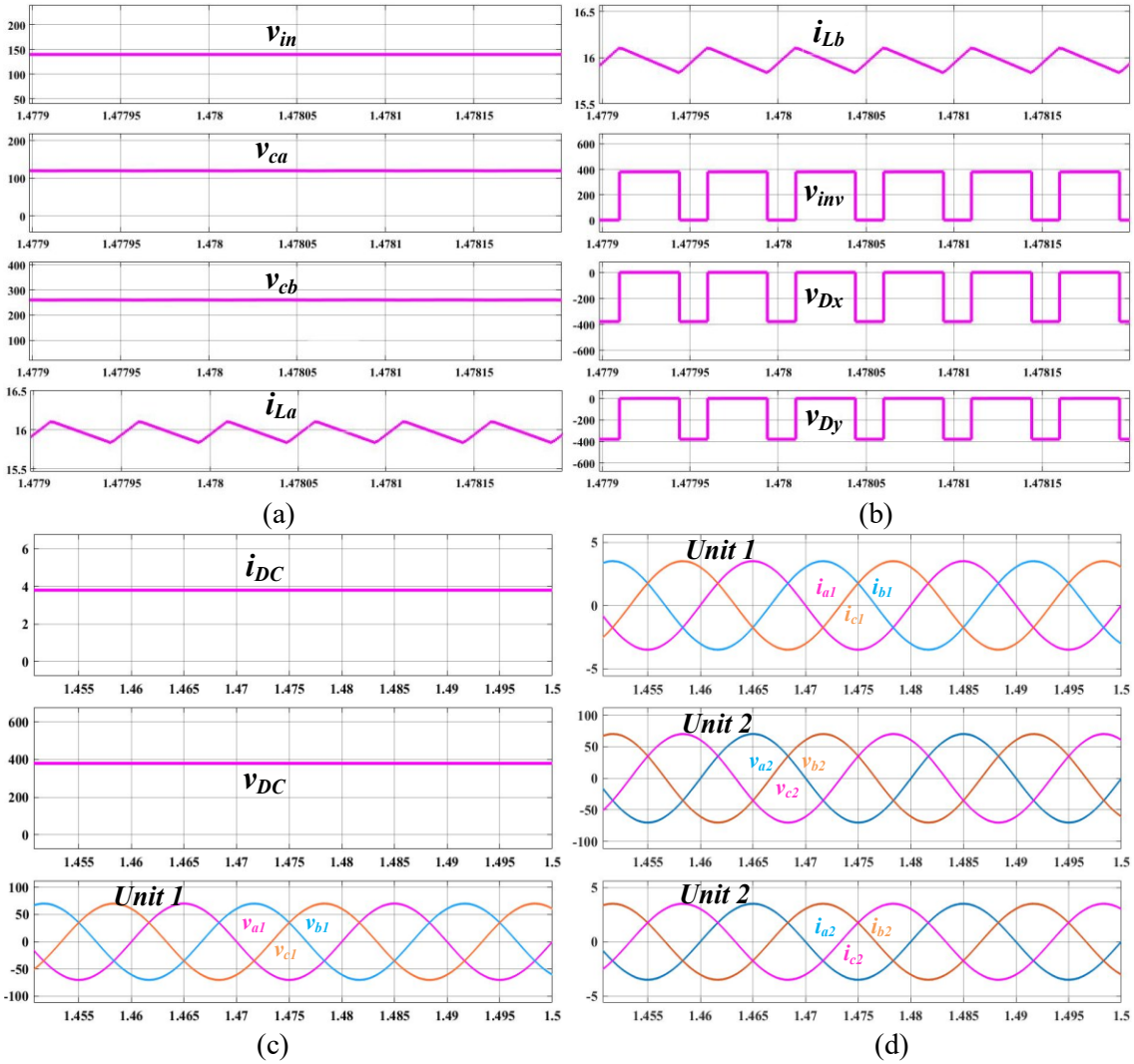


Figure 5.12: Steady-state simulation result of the proposed parallel version converters. (a) input voltage, capacitor voltages, and inductor current i_{La}, (b) inductor currents i_{Lb}, switch node voltage v_{inv} and diode voltages, (c) output DC current and voltage along with three-phase voltage of unit 1 and (d) three-phase currents of Unit 1, three-phase voltages and currents of unit 2 while v_{dcref} = 380 V and v_{ref} = 70 V.

units are 20 Ω. Figure 5.12(a) shows the input voltage (v_{in} = 140 V), capacitors voltages (v_{Ca} = 125 V and v_{Cb} = 255 V) and inductor L_a current (i_{La} = 16 A). Figure 5.12(b) shows inductor (L_b) current (i_{Lb} = 16 A), dc-link voltage (v_{inv} = 380 V) and diode voltages (v_{Dx} = 380 V and v_{Dy} = 380 V). Figure 5.12(c) shows DC output current and voltage (i_{DC} = 3.8 A and v_{DC} = 380 V) along with three-phase voltages (140 V peak-peak) of unit 1. Figure 5.12(d) shows three-phase currents (7 A peak-peak) of unit 1, three-phase voltages (140 V peak-peak) and currents (7 A peak-peak) of unit 2. All the values are approximately equal to the respective theoretical values.

Figure 5.13(a) shows input voltage (v_{in} = 140 V), voltage (v_{inv}) 380 V and inductor currents i_{La} , i_{Lb}. The values of i_{La} and i_{Lb} are approximately equal to the input current i_{in}= 16.5 A. Figure 5.13(b) shows input voltage**,** voltage across the capacitor C_a (v_{Ca} =125 V) and C_b (v_{Cb} =255 V) and DC output voltage (v_{DC} = 380 V). Figure 5.13(c) shows the input voltage, capacitor voltage (v_{Ca} =125 V), DC output voltage (v_{DC} = 380 V) and DC output current (i_{DC} = 3.8 A) with DC load resistance of 100 Ω. Hence, the DC power (P_{DC}) output is equal to 1444 W. Figure 5.13(d) shows the switch node voltage, DC output voltage and current with v_{in}. As v_{inv} and DC network are in parallel, hence $\hat{v}_{inv} = v_{DC}$ = 380. Figure 5.13(e) shows the diodes voltages v_{Dx}, v_{Dy} and capacitor voltage v_{Ca} along with the input voltage v_{in}. The diodes D_x and D_y are forward biased during the NST state, therefore the voltage across it (v_{Dx} and v_{Dy}) is zero. Further, during the ST state, both D_x and D_y are reverse biased, and consequently v_{Dx} and v_{Dy} are negative (-380 V). Figure 5.13(f) shows v_{in} = 140 V, DC output voltage (v_{DC} = 380 V), switch node voltage (v_{inv} = 380 V) and the voltage waveform v_{Dy}. The diode D_y is also forward biased during the NST state, therefore the voltage across v_{Dy} is zero and at the same time the switch node voltage v_{inv} = 380 V. Further, during the ST state, D_y is reverse biased and the v_{Dy} is negative (v_{Dy} = -380 V).

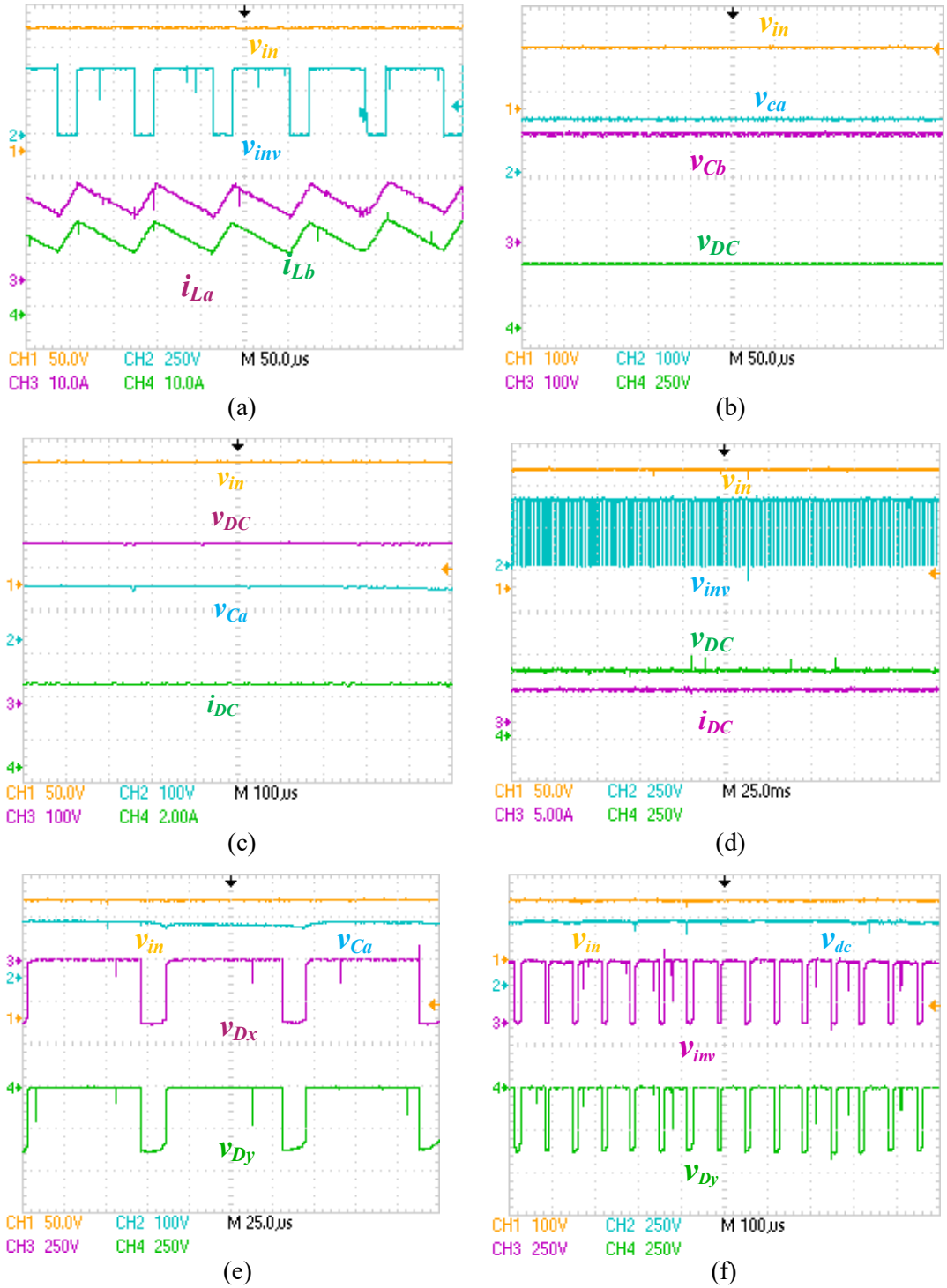


Figure 5.13: Steady state result of the proposed parallel version converters. (a) inductors current and switch node voltage v_{inv} (b) capacitors voltages, output DC voltage (v_{DC}) (c) v_{DC} and current (i_{DC}), (d) switch node voltage (v_{inv}) and v_{DC}, (e) diode voltages (v_{Dx} and v_{Dy}) and (f) v_{inv}, v_{DC} and v_{Dy} with v_{dcref} = 380 V.

Figure 5.14 (a) shows the input voltage v_{in}, switch node voltages of converter units 1 and 2, i.e., $v_{inv1} = v_{inv2} = 380$ V, which are equal to the output of the impedance source network (i.e. v_{inv}) as the inverter units are connected in parallel. Figures 5.14(b) and (c) show input

voltage v_{in} = 140 V and three-phase output voltages of converter units 1 and 2 with magnitude of 140 V (peak-peak), while the reference voltage v_{ref} is 70 V. Figure 5.14 (d) shows v_{in}, output DC voltage (v_{DC} = 380 V with v_{dcref} = 380 V), phase *a* voltage (140V peak-peak) of converter

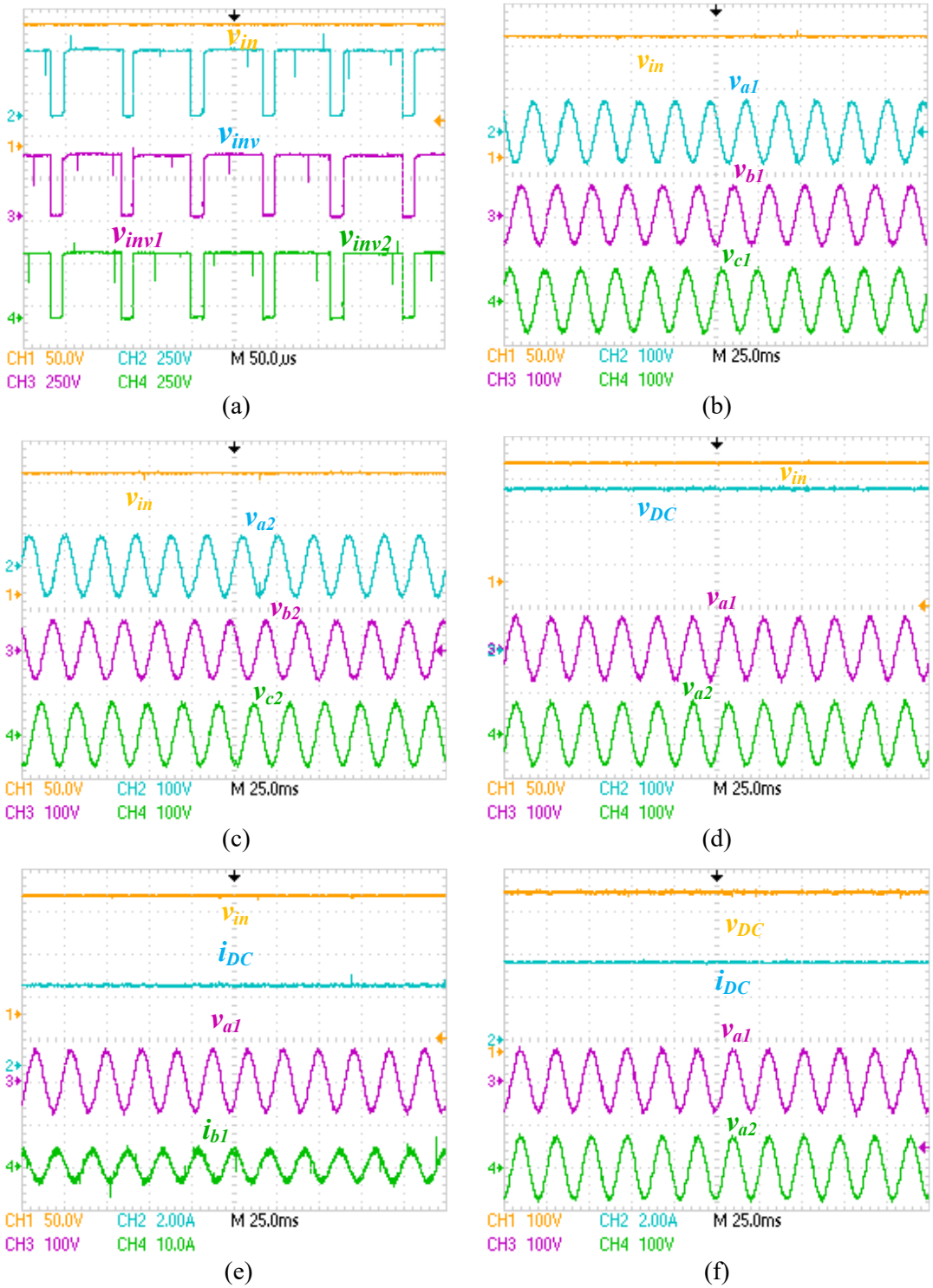
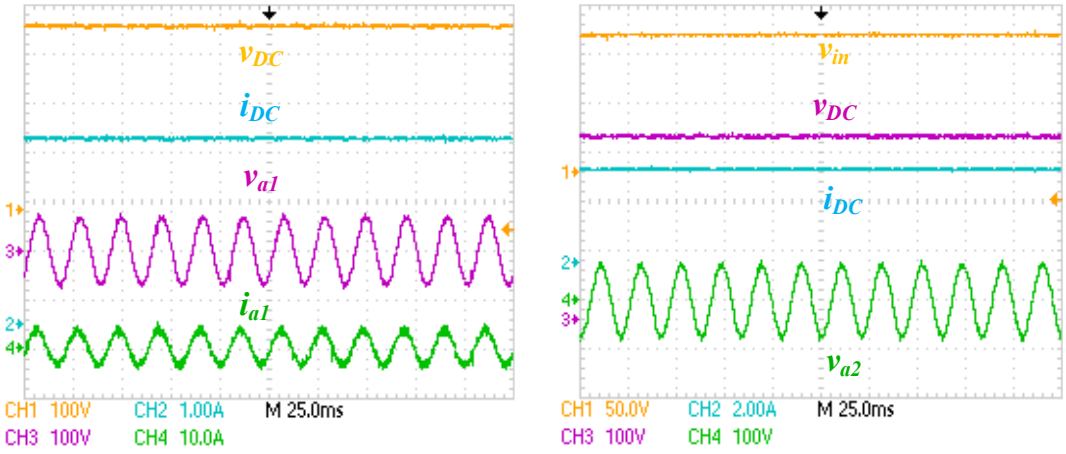


Figure 5.14: Steady state hardware results of the proposed topologies (a) dc-link voltages, (b) three-phase voltages of unit 1, (c) three-phase voltages of unit 2, (d) v_{DC} with phase *a* voltages v_{a1} and v_{a2} of inverter unit 1 and 2, (e) i_{DC} with v_{a1} and phase *b* current (i_{b1}) and (f) i_{DC}, v_{a1} and v_{a2} of units 1 and 2 while v_{dcref} = 380 V and v_{ref} = 70 V.

units 1 and 2 for a reference voltage (v_{ref}) of 70 V for both units. Figure 5.14(e) shows output DC currents i_{DC} =3.8 A, phase *a* voltage (140 V peak-peak), phase *b* current i_{b1} = 7 A (peak-peak) of converter unit 1 along with v_{in}. Figure 5.14(f) shows the output DC voltage, DC current (i_{DC} = 3.8 A as the DC load resistance is 100 Ω) and phase *a* voltage (140 V peak-peak) of inverter units 1 and 2, respectively. For v_{ref} = 70 V, all the three-phases have the same magnitude (i.e. 140 V peak-peak) and 120^0 phase difference showing the balanced system.

Figure 5.15(a) shows output DC voltage v_{DC} = 380 V, output DC currents i_{DC} = 3.8 A, phase *a* voltage (140 V peak-peak) and phase *a* current (7 A peak-peak) for the AC load resistance is 20 Ω of the converter unit 1, while v_{dcref} = 380 V and v_{acref} = 70 V. Phase *a* voltage and current are in the same phase. Output DC voltage, current and phase *a* voltage of unit 2 for the input voltage (v_{in} = 140 V) is shown in Figure 5.15(b), which is approximately equal to the theoretical value.



(a) (b)

Figure 5.15: Steady state hardware results during parallel version of the proposed topologies. (a) Output DC voltage (v_{DC}), currents (i_{DC}) with v_{a1} and phase *a* current (i_{a1}) of the inverter unit 1, (b) DC output voltage (v_{DC}) and i_{DC} with v_{a2} of the inverter unit 2.

Figures 5.16(a) and (b) show the hybrid PWM switching signals of upper switches (S_x, S_y, S_z) and lower sides switches ($S_{x'}$, $S_{y'}$, $S_{z'}$) for the converter unit 1. Figures 5.16(c) and (d) show the hybrid PWM switching signals of upper switches (S_{x2}, S_{y2}, S_{z2}) and lower sides switches ($S_{x'2}$, $S_{y'2}$, $S_{z'2}$) for the converter unit 2 during the parallel mode of operation. It may be observed, that switching signal of unit 1 of upper side S_x, S_y, S_z are complement to the lower

signal $S_{x'}$, $S_{y'}$, $S_{z'}$. It is shown here that during ST period, all the switches of converter units 1 and 2 are ON at the same time.

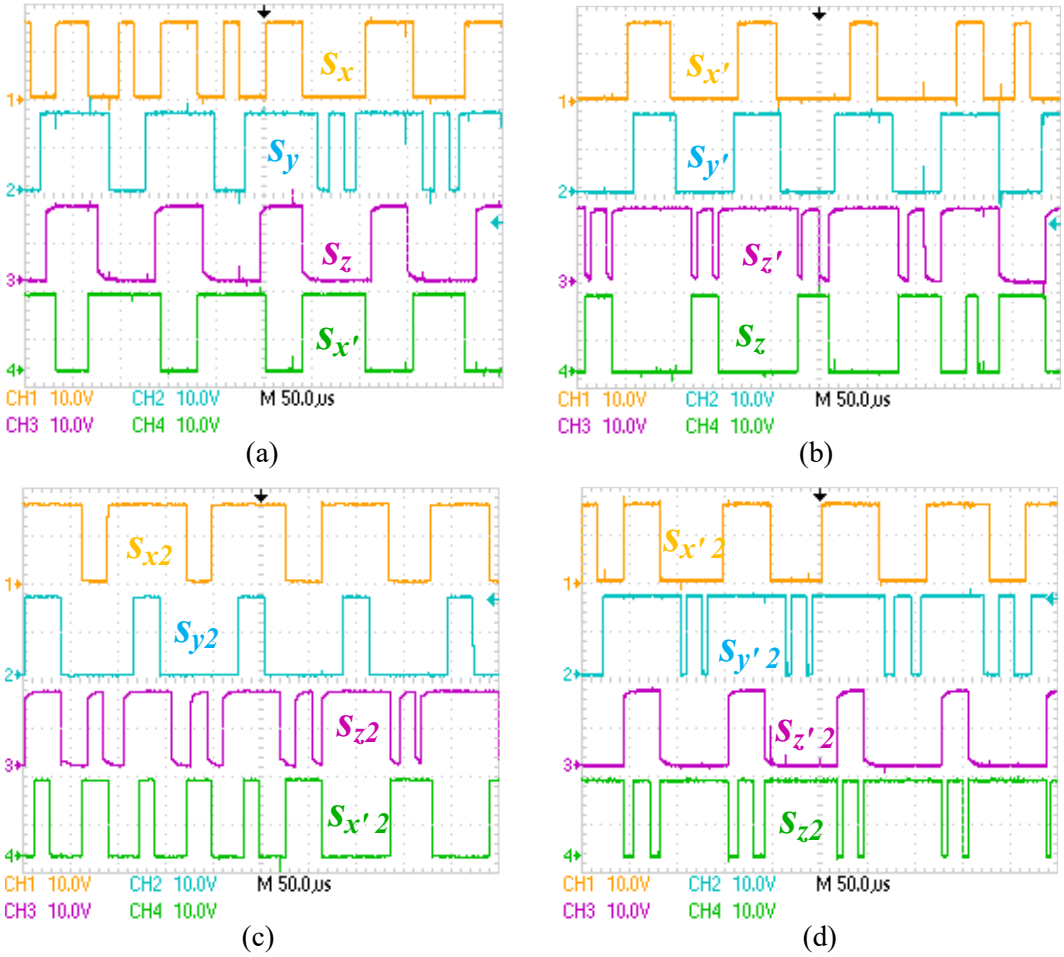


Figure 5.16: Hybrid PWM signals of (a) upper and (b) lower switches of unit 1 (c) upper and (d) lower switches of converter unit 2.

5.8.1.2 Dynamic Response of the Proposed Parallel Version Converters

Figure 5.17 shows the dynamic response of the proposed topologies for DC and AC load transients with same AC reference voltages. Figures 5.17(a) and (b) show step-up and step-down DC load change in DC network with phase *a* voltage (140 V peak-peak) for converter unit 1, while the reference voltages are v_{ref} = 70 V and v_{dcref} = 380 V, respectively. As the DC load current is changed from 3.8 A to 7.6 A, the switch node peak voltage $\hat{v}_{\text{inv}}$ slightly decreases and finally it restores its original value very quickly (within one cycle) and vice-versa. Figures 5.17(c) and (d) show the step-up and step-down load changes in DC network with DC output voltages (v_{dc}). As the DC load current is changed from 3.8 A to 7.6 A,

v_{dc} slightly decreases and finally it restores to its original value within a short time (within one cycle) and vice-versa. Figures 5.17(e) and (f) show step-up and step-down AC load change in converter unit 1. In Figure 5.17(e), the load current of converter unit 1 changes from 7 A to 14 A (peak-peak).

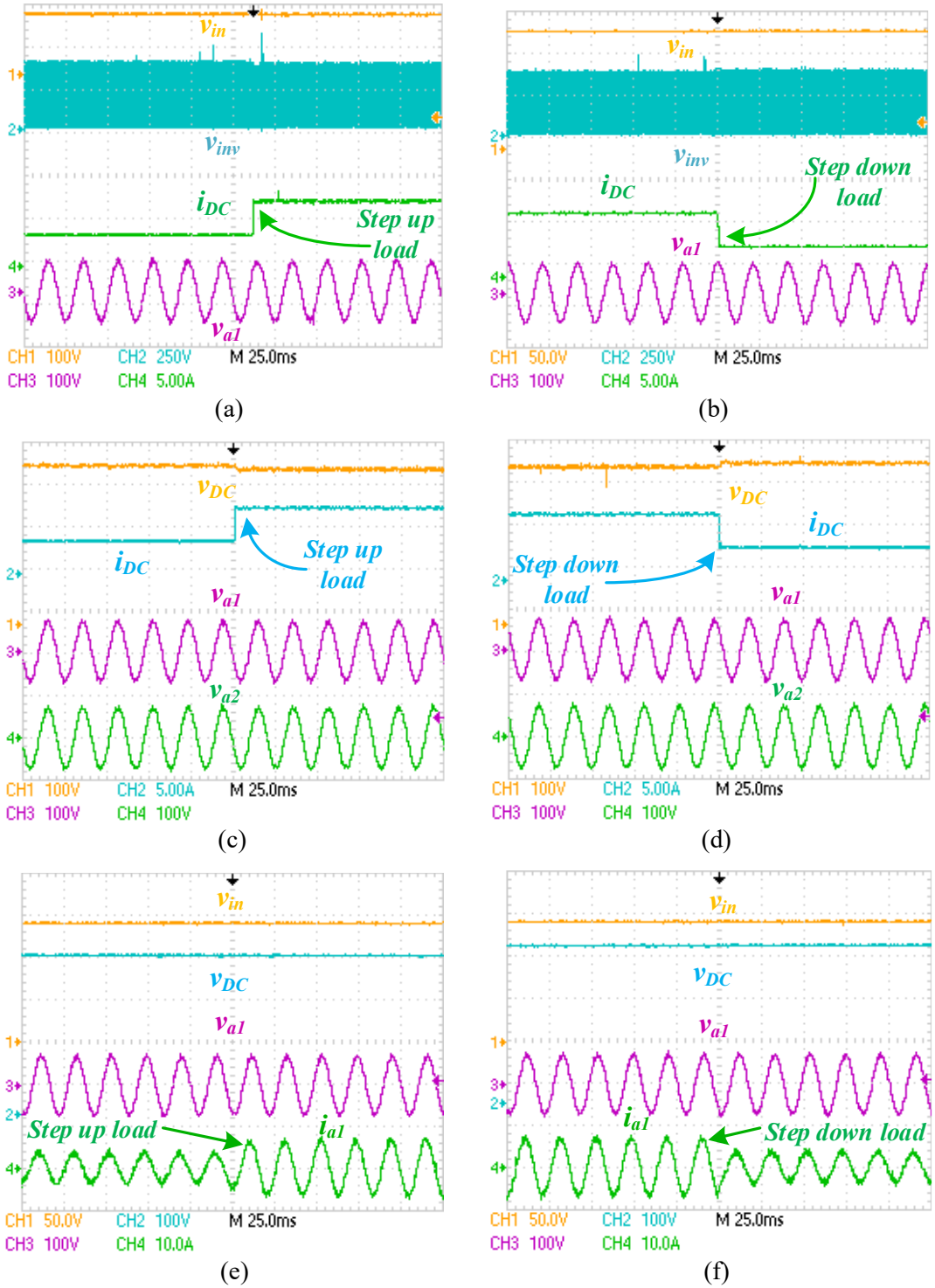


Figure 5.17: Dynamic result of the parallel version topology. (a) step up load change with v_{inv} and v_{a1}, (b) step-down load change with v_{inv} and v_{a1}, (c) step-up dynamics with v_{DC}, v_{a1} and v_{a2}, (d) step-down load change with v_{DC}, v_{a1} and v_{a2}, (e) step-up load change with v_{a1} and v_{DC} and (f) step-down load change with v_{a1} and v_{DC} while v_{dcref} = 380 and v_{ref} = 70 V.

As the load current increases the corresponding voltage of phase *a* (v_{a1}) slightly decreases and it restores its original value within a short time. The DC output voltage (v_{DC}) remains unaffected. Similarly, in Figure 5.17(f), the load current of converter unit 1 changes from 14 A to 7 A (peak-peak). As the load, current decreases, the corresponding voltage of phase *a* (v_{a1}) slightly increases and it restores its original value within a short time (in one cycle) and the DC output voltage (v_{DC}) remains unaffected. It indicates that the system with the proposed converter topology is has a good dynamic response.

5.8.1.3 Dynamic Response of the Proposed Parallel Version Converters with the Different AC Reference Voltages

Figure 5.18 shows the dynamic response of the proposed converter topologies for DC and AC load transients at different AC reference voltages. Figures 5.18(a) and (b) show step-up and step-down DC load change in the DC network with phase *a* voltage 140 V and 100 V (peak-peak) for converter units 1 and 2, and v_{dcref} is 380 V. As the DC load current is changed from 3.8 A to7.6 A, the DC output voltage slightly decreases and finally it restores its original value within a short time and vice-versa. During the DC load change, the AC output voltages (v_{AC}) remains unaffected.

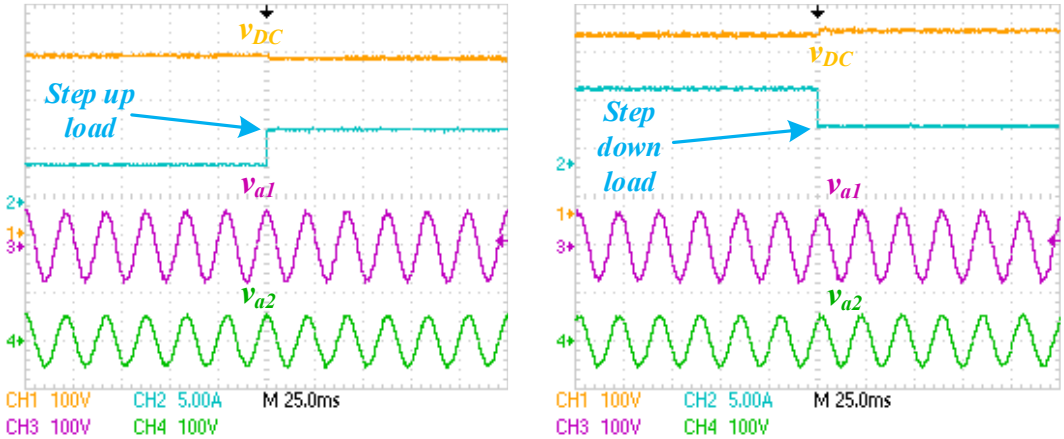


Figure 5.18: Dynamic result of the proposed parallel version topology with different AC reference voltages. (a) step-up load dynamics with v_{DC}, v_{a1} and v_{a2} and (b) Step-down load dynamics with v_{DC}, v_{a1} and v_{a2}.

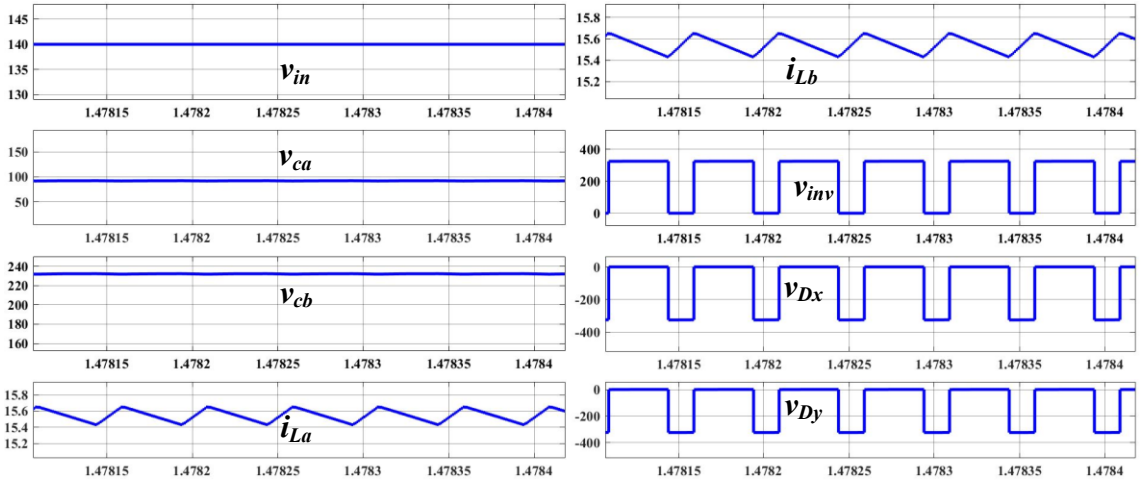
5.8.2 Verification of Proposed Series Version Converters (Regulated Dual AC and Single DC Outputs)

The proposed series version is verified for 2.02 kW with DC power P_{DC} = 1056 W and AC power P_{AC} = 960 W power output.

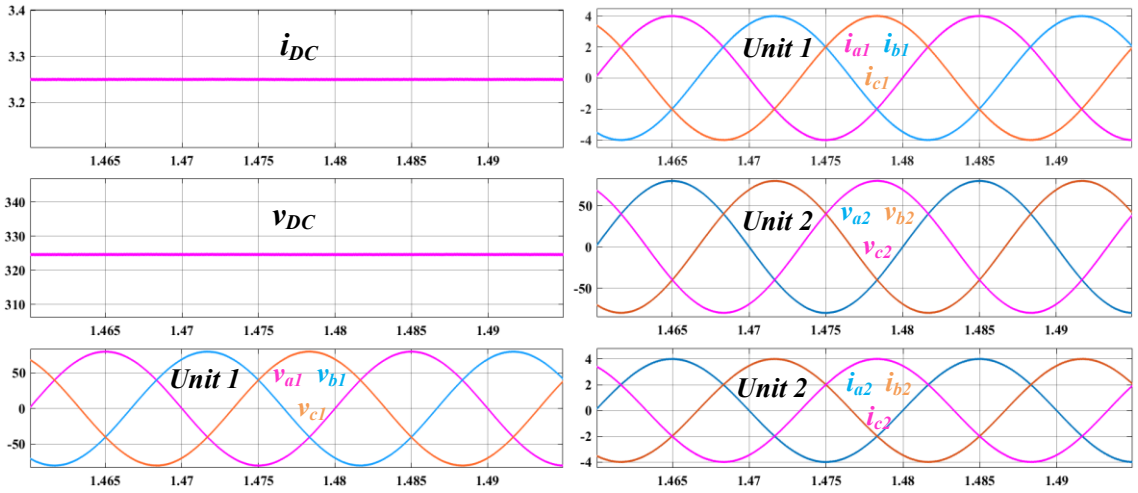
5.8.2.1 Steady State Response of the Series Version Converters

Figures 5.19 and 5.20 show the steady-state simulation and hardware results of the proposed series version HMOCs, respectively. The DC and AC reference voltages for both the inverter units are 325 V and 80 V. The input voltage is v_{in} = 140 V, the DC load resistance is 100 Ω and the AC load resistance for both the inverter units are 20 Ω.

Figure 5.19(a) shows the input voltage (v_{in} = 140 V) capacitors voltages (v_{Ca} = 97 V and v_{Cb} = 228 V) and inductor current i_{La} = 15.5 A. Figure 5.19(b) shows inductor current i_{Lb} = 15.5 A, switch node voltage ($\hat{v}_{inv}$ = 325 V) and diode voltages (v_{Dx} = 325 V and v_{Dy} = 325 V). Figure 5.19(c) shows DC output current and voltage (i_{DC} = 3.25 A and v_{DC} = 325 V) along with three-phase voltages (160 V peak-peak) of unit 1. Figure 5.19(d) shows three-phase currents (8 A peak-peak) of unit 1, three-phase voltages (160 V peak-peak) of unit 2 and currents (8 A peak-peak) of unit 2. All the values are approximately equal to the respective theoretical values.



(a) (b)



(c) (d)

Figure 5.19: Steady-state simulation result of the proposed series version topology. (a) input voltage, capacitor voltages, inductor current i_{La}, (b) inductor current i_{Lb}, switch node voltage v_{inv} and diode voltages, (c) output DC current and voltage along with three-phase voltages of unit 1 and (d) three-phase currents of unit 1 and three-phase voltage and currents of unit 2 while v_{dcref} = 325 V and v_{acref} = 80 V.

Figure 5.20(a) shows the hardware results with the input voltage v_{in} = 140 V, switch node voltage $\hat{v}_{inv}$ = 325 V, inductor currents i_{La} = i_{Lb} = 16.1 A, which is also input current (i_{in}). Since i_{La} = i_{Lb}, charging and discharging nature of both inductor currents are same. Figure 5.20(b) shows v_{in} = 140 V, capacitor voltages v_{Ca} = 97 V and v_{Cb} = 228 V and diode switching voltage v_{Dx} = 325 V. Figure 5.20 (c) gives input voltage v_{in}, DC output current i_{DC} = 3.25 A, DC output voltage v_{DC} = 325 V and switch node voltage v_{inv} = 325 V. Here v_{inv} is equally divided between both the units 1 and 2. Figure 5.20(d) shows the switch node voltage (v_{inv} = 325 V), diode voltages (v_{Dx} = v_{Dy} = 325 V) along with input voltage (v_{in} = 140 V). It is noticed that diodes are reversed biased during ST state and forward biased during NST state. Figures 5.20(e) and (f) show the three-phase voltages (v_{a1}, v_{b1}, v_{c1}) and (v_{a2}, v_{b2}, v_{c2}) of the inverter units 1 and 2 with v_{DC} and phase *c* currents i_{c2}. All the phases of inverter units 1 and 2 have the same voltage magnitudes of 160 V (peak-peak) at v_{acref} = 80 V. All the three-phase voltages are 120^0 phase apart from each other and balanced.

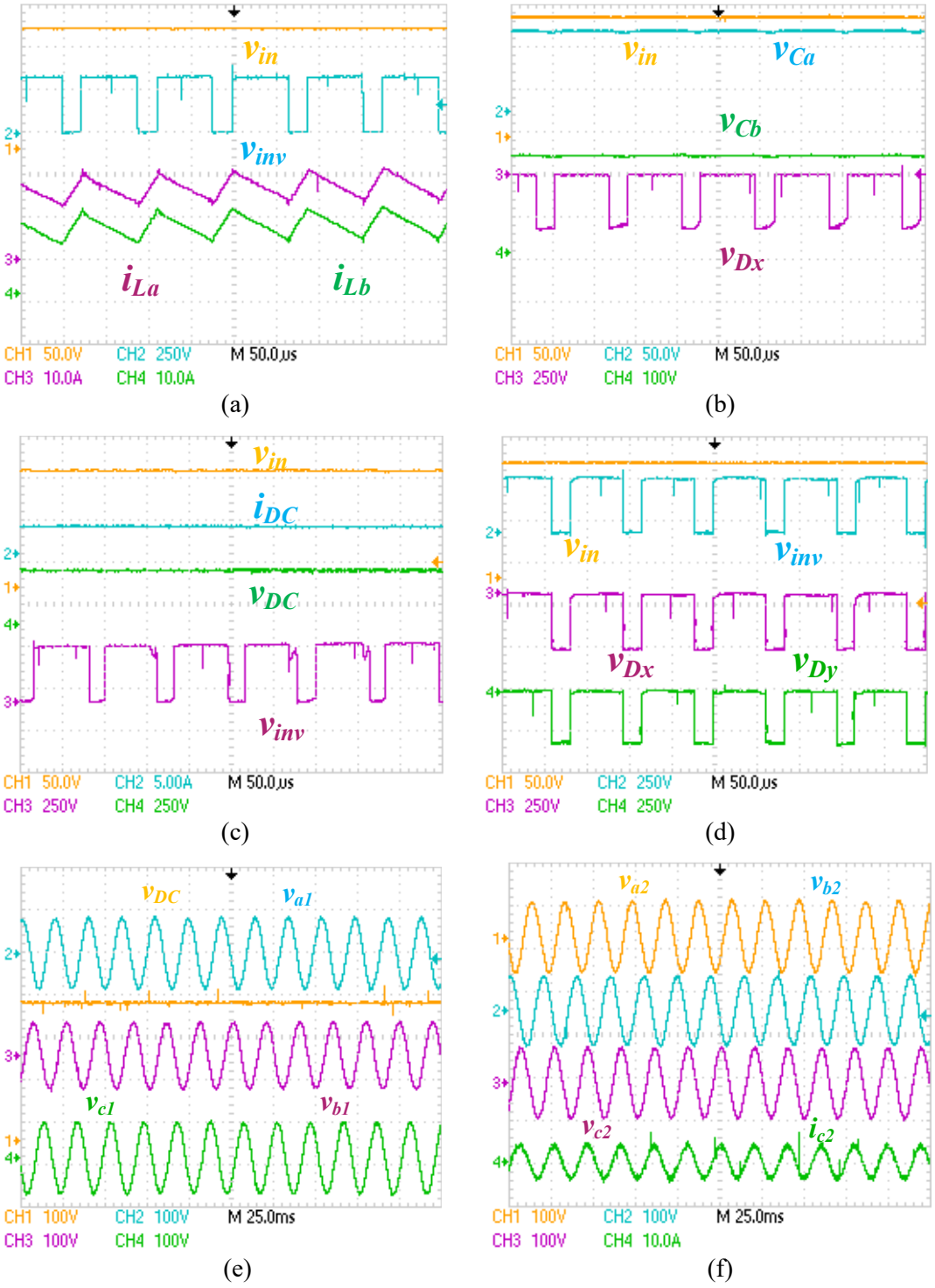


Figure 5.20: Steady-state result of the proposed series version topology. (a) inductor currents with v_{inv}, (b) capacitor voltages with diode voltage (v_{Dx}), (c) DC output voltage (v_{DC}) and current (i_{DC}) with v_{inv}, (d) diode voltages (v_{Dx} and v_{Dy}) with v_{inv}, (e) three-phase voltages of unit 1 with v_{DC} and (f) three-phase voltages of unit 2 with phase c current i_{c2}.

5.8.3 Efficiency and Power Loss Analysis of the Proposed Topologies

Figures 5.21 and 5.22 show the experimental efficiency of both the parallel and series version topologies. Figure 5.21(a) shows the efficiency versus total power output curve during

parallel version, when AC power is constant and DC power variable. In Figure 5.21(b), AC power is variable and DC power is constant. From Figures 5.21(a) and (b), it can be observed that the measured efficiency of the proposed parallel version topology is 90.01% at 2.18 kW load power.

Similarly, Figure 5.22(a) shows the efficiency versus total power output curve during the series version, when the AC power is constant and DC power is variable. In Figure 5.22(b), the AC power is variable and DC power is constant. It can be seen from Figures 5.22(a) and (b) that the efficiency of the proposed series version topology is 89.95% at a load power of 2.02 kW. It is necessary to mention that the efficiency of the proposed topologies can be further improved by optimizing the passive components, printed circuit boards and semiconductor devices.

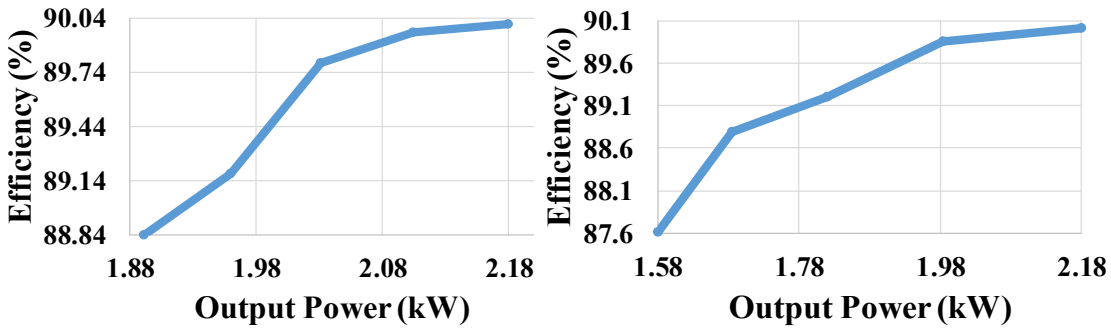


Figure 5.21: Measured efficiency versus total output power curve for parallel version. (a) variable DC and constant AC power and (b) variable AC and constant DC power.

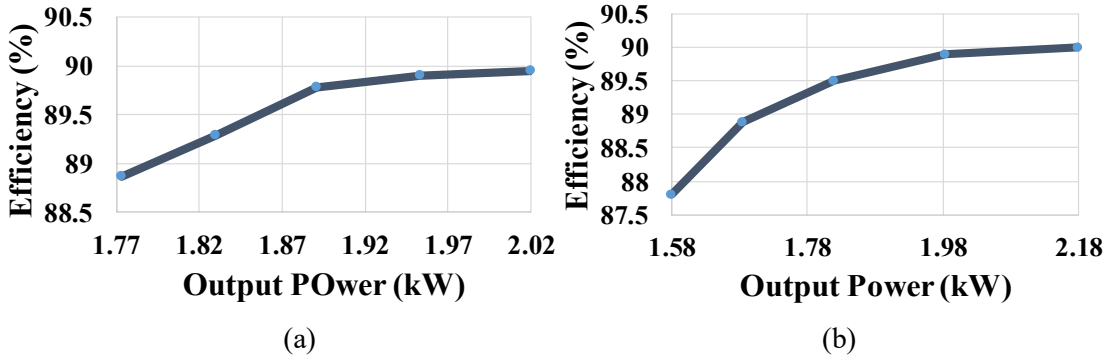
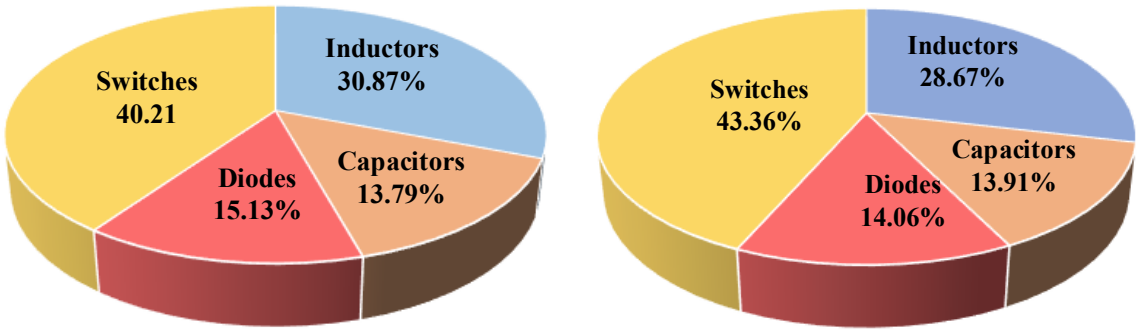


Figure 5.22: Measured efficiency versus total output power curve for series version. (a) variable DC and constant AC power and (b) variable AC and constant DC power.

The power loss distribution of elements of the proposed parallel and series version are shown in Figures 5.23(a) and (b) and calculated as discussed in [119]. This is achieved by calculating the non-idealities, voltages and currents of the elements of the proposed topologies. Power losses in the proposed topologies are due to conduction and switching states in semiconductor devices and due to losses in the passive components [120]-[121].



(a) (b)

Figure 5.23: Power loss distribution for (a) parallel and (b) series version topologies.

For calculating the power losses, the following assumptions are taken:

1) The switches are modelled by an ideal switch having a forward resistance (r_S) and a collector to emitter saturation voltage ($v_{CE(on)}$).
2) The diodes are modelled by an ideal switch having a forward series resistance (r_D) and a forward voltage drop (v_{FD}).
3) The winding dc resistance (DCR) of inductors (r_L) and equivalent series resistance (ESR) of capacitors (r_C) are considered.
4) The collector to emitter current of switches (i_{CE}), anode to cathode current of diodes (i_D), the current through inductors (i_L) and the current through capacitors (i_C) are considered.
5) The inductor current ripples are ignored.

Losses in switches (IGBTs):

The conduction loss of switches in the inverter bridge is calculated as

$$P_{Cond\_S} = \frac{1}{T_s}\int_0^{T_s}\left(v_{CE(on)}i_{C(avg)} + r_S i_{C(rms)}^2\right)dt \quad (5.22)$$

The switching loss is calculated as

$$P_{Switch\_S}^{on,off} = \frac{1}{T_s}\int_0^{t_{on}+t_{off}}(v_{CE}(t)i_C(t))dt \quad (5.23)$$

Total power losses of the inverter switches are calculated as

$$P_{Total\_S} = 12\left(P_{Cond\_S} + P_{Switch\_S}^{on,off}\right) \quad (5.24)$$

Losses in Diodes:

The conduction losses of diodes are calculated as

$$P_{Cond\_D} = \frac{1}{T_s}\int_0^{T_s}\left(v_{FD}i_{D(avg)} + r_D i_{D(rms)}^2\right)dt \quad (5.25)$$

Generally, turn-on switching losses of diodes are negligible. The turn-off switching losses of diodes are calculated as

$$P_{Swicth\_D}^{off} = \frac{2}{T_s}\int_0^{t_{off}} v_D(t)\, i_D(t)dt \quad (5.26)$$

Losses in inductors:

The power losses of inductors include core losses and winding losses. Generally, the core losses are negligible for pulse width modulated converters. The winding losses depend on the resistances of the windings (r_L) of inductors and are calculated as

$$P_{wind\_L} = r_L i_{L(rms)}^2 \quad (5.27)$$

Losses in capacitors:

The power losses of the capacitors depend on the equivalent series resistances (r_C) and are calculated as

$$P_{rC} = \frac{1}{T_s}\int_0^{T_s} r_C i_C^2 dt \quad (5.28)$$

The overall loss is theoretically calculated by the addition of the above break-up of losses.

To compare the efficiencies of the proposed QSPHC topologies with other topologies, a comparison table (Table 5.6) among the proposed topologies and some closely related similar

hybrid converter topologies are prepared. It is found that the efficiencies of the proposed topologies are quite high as compared to reported topologies. Table VI shows that the efficiencies of BDHC [60], CFSI [63] and hybrid buck-boost converter [70] are less than that of the proposed topologies. Two converters IHC [64] and minimum phase dual output converter [65] show a little higher efficiency than that of the proposed topologies. However, there are some advantages of the proposed topologies over these converters. The converters of [64] and [65] have only one DC and one single-phase AC output. In contrast, the proposed QSPHC topologies are capable of providing simultaneous multiple series or parallel three-phase AC along with one DC output. Figure 5.24 shows the efficiency comparison curve of the proposed parallel version topology with the other topologies [60], [64], [65] and [70].

TABLE 5.6

EFFICIENCY OF THE VARIOUS HYBRID CONVERTERS

Hybrid Converter	Maximum Efficiency
BDHC [60]	88.1%
CFSI [63]	82.45%
Hybrid buck-boost converter [70]	88.5%
IHC [64]	91.32%
Minimum phase dual output converter [65]	91.4%
Proposed parallel QSPHC topology	90.01%
Proposed series QSPHC topology	89.95%

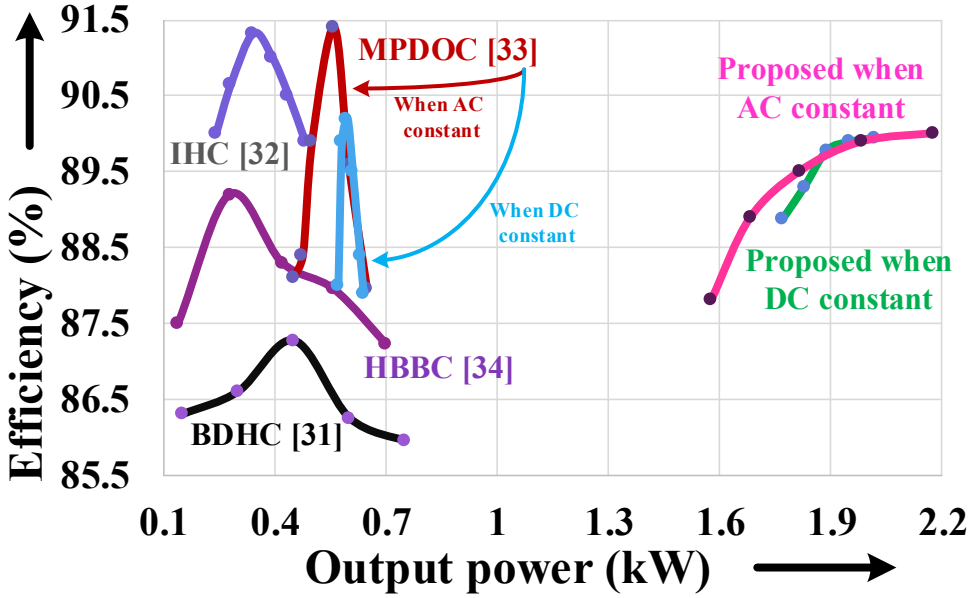


Figure 5.24: Efficiency comparison curve of the different converters.

5.9 Conclusion

This chapter presents two versions of diode-assisted switched LC Three-phase Multi AC quasi-Z-source series-parallel hybrid converter (QSPHC) topologies with *n* number of three-phase AC and one boost DC outputs simultaneously. The proposed parallel version topology is capable of giving *n* number of three-phase AC outputs and one boost DC output with constant voltage and variable load current. Likewise, the series version gives *n* number of three-phase AC outputs and one boost DC output with constant load current. All the outputs of the proposed topologies can be independently regulated and can be fed directly to feed three-phase microgrids and multiple three-phase loads without using extra local adapter/regulator. The proposed topologies are operated using a hybrid PWM technique. Detailed mathematical modeling, steady-state cost analysis, and efficiency analysis are carried out for the proposed topologies in this chapter. In the cost analysis, the cost of the proposed QSPHCs with two parallel inverter units is compared with that of two single unit individual converters is done for same power (2.18 kW). The number of components are less in the proposed QSPHC topologies with two units, as the front end passive components are fixed. Therefore, for proposed QSPHCs with two units, though the price per component is higher due to increased stress/rating, the overall cost come out to be less as compared with its counterparts i.e. two single unit individual converters. Finally, laboratory prototypes of 2.18 kW and 2.02 kW are developed to validate the performance of the proposed converters for parallel and series versions, respectively. The measured efficiency of the parallel and series version of the proposed topologies are 90.01% and 89.95%, respectively.