

Modified grey wolf optimisation based reduced device count 17-level hybrid multilevel inverter

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Abstract

A 17-level hybrid multilevel inverter (HMLI) using modified grey wolf optimisation (MGWO) is proposed here. The proposed HMLI requires only a single dc source and a lesser number of circuit elements to obtain a multilevel voltage level. The proposed HMLI can also enhance the input voltage and has reverse current carrying capability. The selective harmonic elimination pulse width modulation technique is implemented through MGWO for determining the optimal switching angles of the proposed HMLI to eliminate lower order harmonics. The MGWO algorithm gives improved results as compared to other existing optimisation algorithms in terms of fitness value, convergence speed and harmonic profile of the output voltage. The proposed HMLI is also compared with some of the other existing HMLIs in terms of the number of circuit elements, peak inverse voltage and total blocking voltage to exhibit its advantages. Finally, a 550 W prototype is fabricated in the laboratory to evaluate the effectiveness of the proposed HMLI.

1 | INTRODUCTION

The requirement of high-power quality in industrial and renewable energy applications such as photovoltaic and wind has influenced the introduction of multilevel inverters (MLIs). In recent years, MLIs have drawn much attention in medium and higher power applications for their low switching frequencies and capability to resist higher voltages [1]. The principal benefits of MLIs are lower total harmonic distortion (THD), lower EMI, and higher efficiency. MLIs are categorised into diode-clamped [2], flying capacitor [3], and cascaded H-bridge topologies [3], [4] in general. Diodes and capacitors are used to obtain the voltage levels in diode clamped and flying capacitor MLIs. However, these MLIs need more number of power switches, capacitors and diodes to obtain voltage levels. In cascaded H-bridge (CHB) MLIs do not require capacitors or diodes but CHB-MLIs need more number of dc power supplies for obtaining a greater number of voltage levels.

The use of a greater number of input dc sources in cascaded H-bridge MLIs increases the cost of the overall system. In order to reduce the number of input dc sources and switches in cascaded H-bridge MLIs, hybrid cascaded H-bridge MLIs have been reported, where capacitors are used to reduce the number

of input dc sources [5–8]. As hybrid H-bridge MLI topologies use capacitors and dc sources, the voltage balance of capacitors is an intrinsic problem. Different control methods are proposed for balancing the capacitor voltages in hybrid H-bridge MLIs. All the structures make these topologies more complicated and costly. In [9] and [10], coupled inductor-based MLIs are presented; however, more number of inductors are required to obtain higher voltage levels, which increases cost and make the overall system bulkier. Moreover, the possibility of extending the number of output voltage levels is also not feasible in these MLIs.

During the last decades, several modular multilevel converters (MMC) have been proposed [11–13]. Submodule (SM) is the basic component of MMC. The submodules are classified into two categories: two-level submodule topologies with a single source and multilevel submodule with multiple voltage sources. The half-bridge submodule is the popular configuration because it is simple among all the SM topologies [11]. However, the components in these topologies are high and capacitor balancing is one of the major issues, which also need voltage sensors. A new type of self-balancing submodule is proposed in [12] and [13]. It uses a half-bridge SM with an inductor and one diode. The component counts and the use of the inductor increase its cost.

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Switched-capacitor multilevel inverters (SC-MLIs) have emerging technology to solve the problems of capacitor voltage balancing and the required numbers of circuit components used in conventional MLIs. The topology presented in [14] uses battery cells to obtain the output. The proposed topology uses lesser passive devices but the required number of active devices is high. Several topologies of SC-MLIs have been reported in recent years [15–28]. In the topologies [15–18], single source is used. However, total blocking voltage (TBV) and peak inverse voltage (PIV) increase rapidly with the increased number of output voltage levels. The topologies presented in [20], [22] and [24] possess low PIV but they require more number of switches. Topologies in [19] and [25] possess low TBV, but the required number of switches in these MLIs are very high. The topology presented in [28] has low TBV and PIV, and it also requires lesser number of capacitors. However, its boosting ability is restricted. Thus, it has been observed that for increasing the output voltage levels in existing SC-MLIs, the number of active and passive elements increases, which makes the overall system voluminous and expensive.

Among the aforementioned issues, a number of dc voltage sources and switch count are identified as one of the most important issues in the implementation of a hybrid multilevel inverter (HMLI), since each switch requires an extra gate driver, protection unit, and voluminous heat sink which adds up to the cost and volume of the overall system. In order to take care of these issues, a new 17-level self-voltage balanced SC-MLI is proposed, which generates higher output voltages using a single dc voltage source and a lower number of switches along with the reduced TSV and PIV, thus lowering the rating of power devices used. The topology possesses reverse current capabilities. It can also be scaled to generate higher voltage levels as per necessity. The capacitors are periodically charged and discharged without any additional balancing mechanism. Output voltages higher than input voltage are achieved by the proposed HMLI, thus signifying the boosting property of the converter.

Different pulse width modulation (PWM) techniques used in HMLIs are categorised based on their switching frequencies. Sinusoidal pulse width modulation and space vector modulation (SVM) are the commonly used high-frequency switching techniques. In these switching techniques, losses will be more, and distortion in the output voltage is also high. The complexity in computation is one of the major disadvantages of SVM. Higher-order harmonics can be eliminated using low-pass filters, but lower-order harmonics cannot be completely eliminated using conventional PWM techniques. Selective harmonic elimination PWM (SHEPWM) is a popularly used PWM technique to determine optimal switching angles so as to eliminate lower order harmonics by solving non-linear transcendental equations. The iterative techniques such as Newton–Raphson and the theory of resultant methods are taken to solve the non-linear transcendental equations. However, the use of these methods is not practical for a large number of switching angles to be solved as the degree polynomials in the non-linear transcendental equations increase for higher number of harmonics and have to be removed. Evolutionary algorithms have been used to overcome

limitations of conventional iterative methods [29–37] such as genetic algorithm (GA) [29], ant-colony optimisation (ACO) [31], firefly algorithm (FA) [32], bee algorithm (BEE) [30], particle swarm optimisation (PSO) [33] and fish swarm optimisation (FSO) [34]. Genetic algorithm (GA) is one of the early developed evolutionary algorithms [19], which works on crossover and mutation. The early convergence, high computational time and weak local searching capability are the demerits of GA. GA has a slower convergence rate in comparison to BEE and ACO. Particle swarm optimisation (PSO) is another widely used bio-inspired evolutionary algorithm. It has been observed that for PSO outstrips ACO and BEE in terms of convergence, PSO does not possess any evolutionary criterion like mutation and crossover, but its convergence speed is less and it also fails to find global optima precisely. This problem can be solved by applying FA. It gives better convergence and less possibility of being trapped at local minima in comparison to PSO, but FA possesses lesser convergence speed as compared to PSO. Newly, PSO redeveloped fish swarm optimisation has been proposed [34]. It provides better performance as compared to FSO and PSO.

Grey wolf optimisation (GWO) algorithm is one of the recently developed meta-heuristic algorithms. GWO impersonates the hunting behaviour and ladder of grey wolves [36]. It uses four different stages to attain global optima such as searching, surrounding, stalking and attacking the prey. However, GWO agonises from poor convergence speed and infirm local searching capability because of its simple location updating strategy. To take care of this problem, a modified GWO (MGWO) algorithm-based switching technique is used in this work [37]. MGWO keeps the balance between exploitation and exploration of searching mechanism. MGWO avoids stagnation of local minima using the weighted sum of best locations in its position upgrade strategy. The rate of convergence of MGWO is faster as compared to GA, PSO and GWO. The present work investigates MGWO optimised reduce device count 17-level HMLI.

Section 2 delineates the proposed 17-level HMLI and its operation. Section 3 explains MGWO algorithm and its implementation for harmonic elimination in HMLI. The capacitor calculation of the HMLI is given in Section 4. The comparison of HMLI with other reported HMLIs is given in Section 5. In Section 6, the experimental verification of the proposed 17-level HMLI is deliberated. Finally, the conclusion of the paper is described in Section 7.

2 | PROPOSED 17-LEVEL HYBRID MULTILEVEL INVERTER

The structure of the proposed 17-level HMLI is depicted in Figure 1. It follows series–parallel combinations of capacitors and voltage source to obtain levels. It consists of a single dc source, four capacitors C_1 – C_4 , five diodes D_1 – D_5 and eleven switches S_1 – S_5 , M_1 – M_2 and Q_1 – Q_4 . The capacitor voltages of C_1 , C_2 and C_3 are maintained at the input voltage V_{DC} , whereas the capacitor voltage of C_4 is maintained at $V_{DC}/2$.

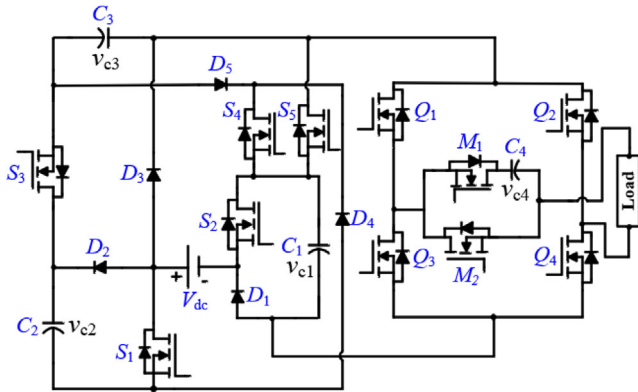


FIGURE 1 Circuit configuration of the proposed 17-level HMLI

TABLE 1 Switching patterns, diode and capacitor states at each voltage level

Output voltage	$S_1-S_5; Q_1-Q_4; M_1-M_2$	D_1-D_5	C_1-C_4
$+4V_{DC}$	11100100101	00000	DDDU
$+7V_{DC}/2$	11100100110	00000	DDDC
$+3V_{DC}$	10100100101	10000	UDDU
$+5V_{DC}/2$	10100100110	10000	UDDC
$+2V_{DC}$	01010100101	01111	DCCU
$+3V_{DC}/2$	01010100110	01111	DCCC
$+V_{DC}$	00001100101	10100	CUUU
$+V_{DC}/2$	00001100110	10100	CUUC
0	01010110001	01111	UCCU
$-V_{DC}/2$	00011110010	01111	UCCD
$-V_{DC}$	00001011001	10100	CUUU
$-3V_{DC}/2$	00001011010	10100	CUUD
$-2V_{DC}$	01010011001	01111	DCCU
$-5V_{DC}/2$	01010011010	01111	DCCD
$-3V_{DC}$	10100011001	10000	UDDU
$-7V_{DC}/2$	10100011010	10000	UDDD
$-4V_{DC}$	11100011001	00000	DDDU

1: turn ON; 0: turn OFF (switches), C: charging, D: discharging; U: unchanged (capacitors).

The voltage balancing mechanism of capacitor C_4 is given in the Appendix.

The switching and capacitor states for each voltage level of 17-level HMLI are given in Table 1. In the column of switches, 1 represents turn ON and 0 for turn OFF. In the column of diode, 0 and 1 represent reverse blocking and forward conduction, respectively. The direction of current of each positive voltage levels are depicted in Figures 2a–d and 3a–d. The dotted lines (blue): the charging path; the solid (red) lines: power flow path through the load and the dark (solid) lines: the reverse current path of HMLI.

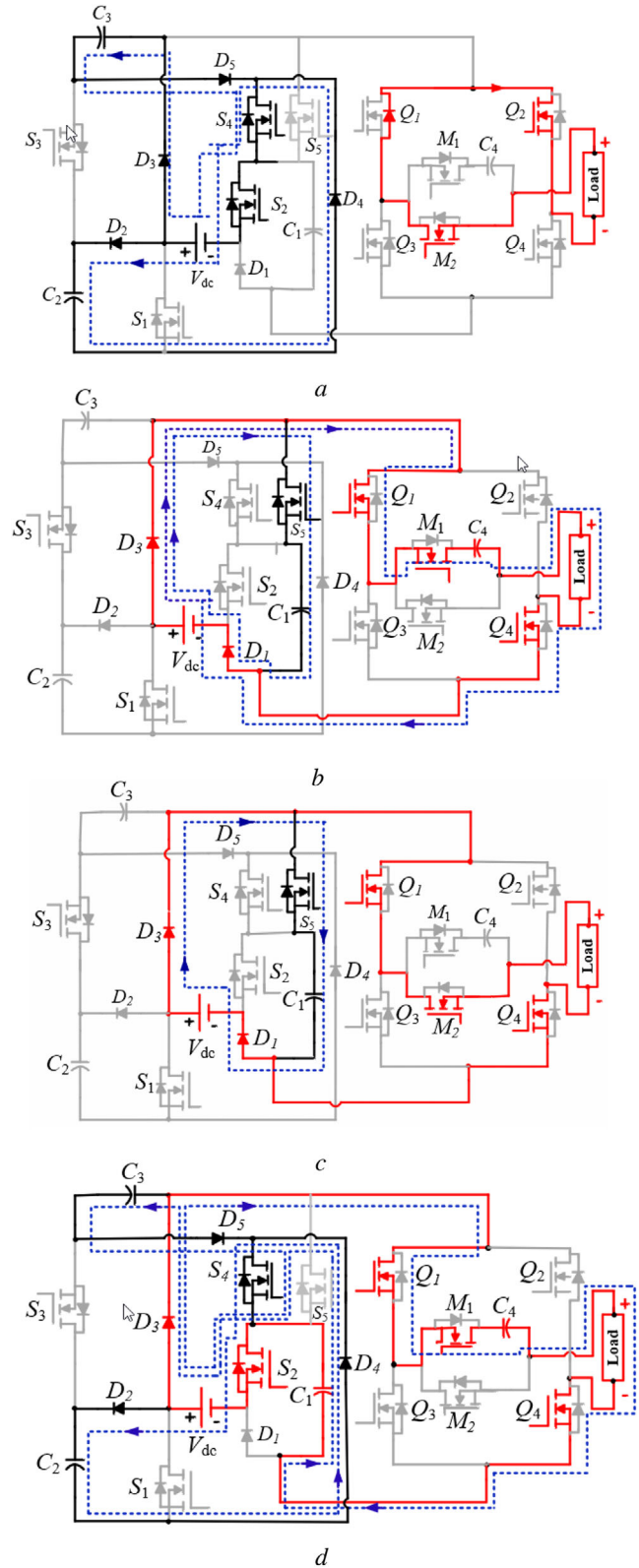


FIGURE 2 Current flow for positive output voltage levels of the proposed 17-level HMLI: (a) current flow at voltage level zero, (b) current flow at voltage level $V_{dc}/2$, (c) current flow at voltage level V_{dc} , (d) current flow at voltage level $3V_{dc}/2$

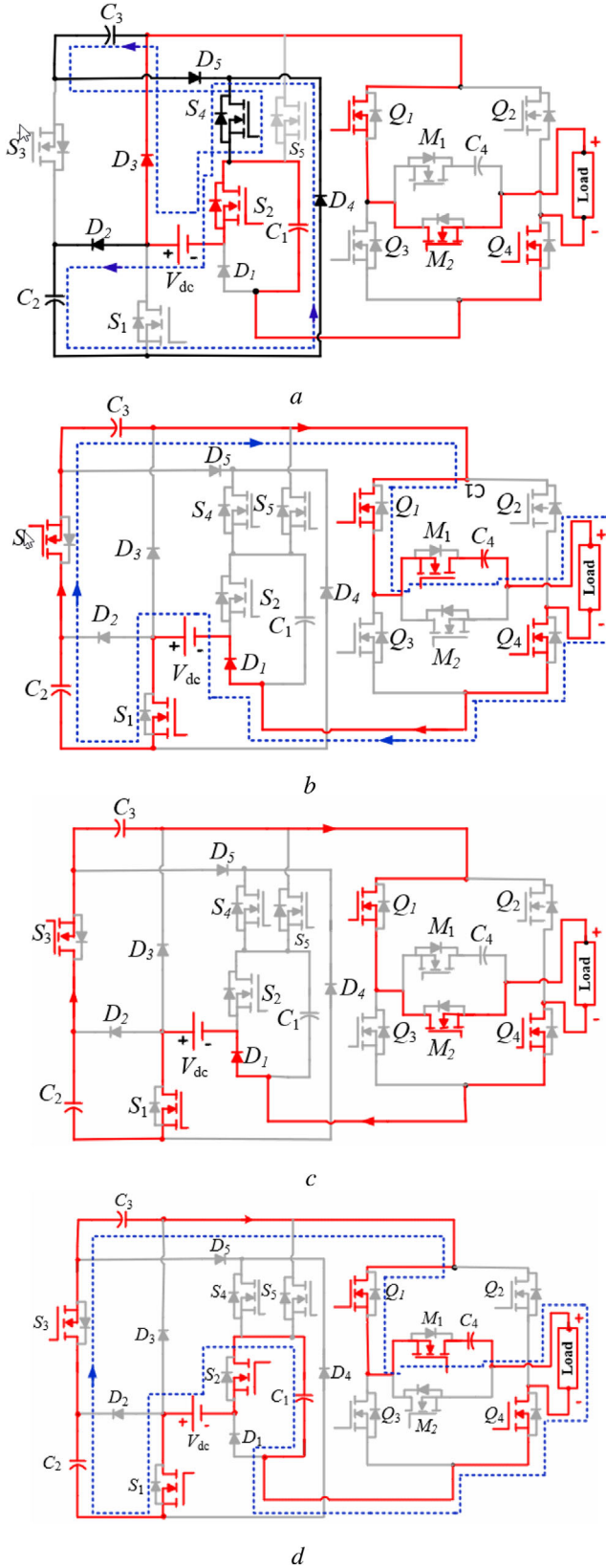


FIGURE 3 Current flow for positive output voltage levels of the proposed 17-level HMLI: (a) current flow at voltage level $2V_{dc}$, (b) current flow at voltage level $5V_{dc}/2$, (c) current flow at voltage level $3V_{dc}$, (d) current flow at voltage level $7V_{dc}/2$

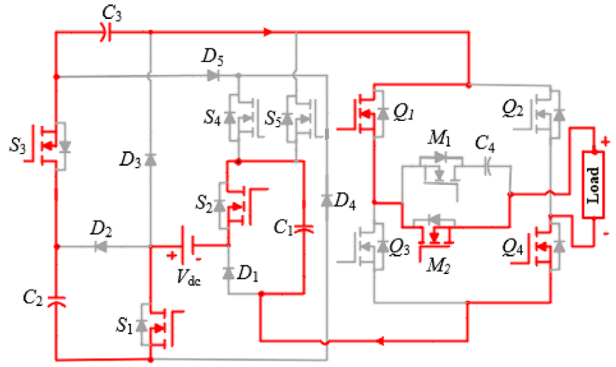


FIGURE 4 Current flow for voltage level $4V_{dc}$

Level zero, Figure 2a: This level is achieved by turning on switches Q_1 , Q_2 and M_2 . The capacitors C_2 and C_3 charge through switches S_2 , S_4 and diodes D_2 , D_3 , D_4 and D_5 in this interval.

Level $V_{dc}/2$, Figure 2b: It is achieved using voltage source V_{dc} , diodes D_1 , D_3 and switches Q_1 , M_1 and Q_4 . The capacitors C_1 and C_4 charge through D_3 , D_1 and S_5 in this voltage level.

Level V_{dc} , Figure 2c: This voltage level is obtained through voltage source V_{dc} , diodes D_1 , D_3 and switches Q_1 , M_2 , Q_4 . The capacitor C_1 also charges in this interval through D_3 , D_1 and S_5 .

Level $3V_{dc}/2$, Figure 2d: This level is achieved when the current flows through voltage source V_{dc} , diode D_3 and switches S_2 , Q_1 , M_1 and Q_4 . The capacitors (C_2 , C_3) and C_4 charge in this interval through (D_2 , D_4 , S_4 , S_2) and (D_3 , D_5 , S_4 , S_2 ; S_2 , Q_1 , M_1 , Q_4), respectively. The capacitor C_1 discharge through D_3 , S_2 , Q_1 , M_1 and Q_4 in this interval.

Level $2V_{dc}$, Figure 3a: It is achieved using voltage source V_{dc} diode D_3 , and switches S_2 , Q_1 , M_2 and Q_4 . The capacitors C_2 and C_3 charge in this interval through (D_2 , D_4 , S_4 , S_2) and (D_3 , D_5 , S_4 , S_2) and capacitor C_1 discharges through D_3 , S_2 , Q_1 , M_2 and Q_4 .

Level $5V_{dc}/2$, Figure 3b: This voltage level is achieved using diode D_1 and switches S_1 , S_3 , Q_1 , M_1 and Q_4 . The capacitors C_2 and C_3 are in series with source and discharge using D_1 , S_1 , S_3 , Q_1 , M_1 and Q_4 to obtain output. The capacitor C_4 gets charged in this interval.

Level $3V_{dc}$, Figure 3c: It is achieved using diode D_1 and switches S_1 , S_3 , Q_1 , M_2 , and Q_4 . The capacitors C_2 and C_3 are in series with dc source and discharge through path D_1 , S_1 , S_3 , Q_1 , M_2 and Q_4 to generate output voltage.

Level $7V_{dc}/2$, Figure 3d: It is achieved when the current flows in the diode D_1 and switches S_2 , S_1 , S_3 , Q_1 , M_1 and Q_4 . The C_1 , C_2 and C_3 are in series with dc source and they discharge using D_1 and switches S_1 , S_3 , Q_1 , M_1 and Q_4 to generate the required output voltage. The capacitors C_4 charges in this interval.

Level $4V_{dc}$, Figure 4: It is achieved using diode D_1 and switches S_2 , S_1 , S_3 , Q_1 , M_2 and Q_4 . The C_1 , C_2 and C_3 are in series with source and discharge using switches S_2 , S_1 , S_3 , Q_1 , M_2 and Q_4 to generate the required output voltage.

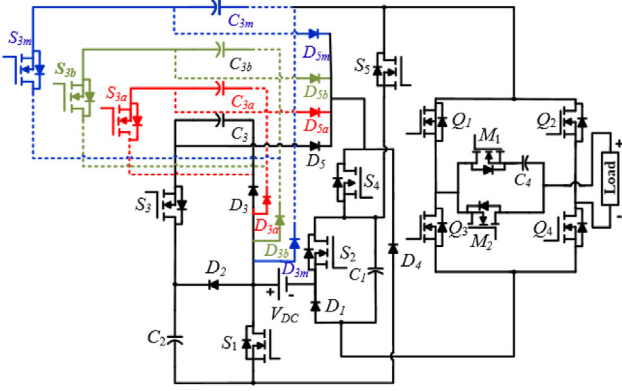


FIGURE 5 Generalised extended structure of the proposed 17-level HMLI

Similarly, other voltage levels can be obtained through switching patterns given in Table 1.

2.1 | Scaled structure of the proposed 17-level HMLI

The extended structure of the proposed HMLI is attained through the addition of another unit (m) which consists of a switch S_{3a} , one capacitor C_{3a} and two diodes D_{3a} , D_{5a} . Each such extended unit adds four voltage levels. The extended structure of the proposed HMLI (generalised; $17+4m$) is depicted in Figure 5. The voltage levels in the extended structure can be obtained by adding switches S_{3a} , S_{3b} , ..., S_{3m} ; capacitor C_{3a} , C_{3b} , ..., C_{3m} and diodes D_{3a} , D_{3b} , D_{3c} , ..., D_{3m} and D_{5a} , D_{5b} , D_{5c} , ..., D_{5m} . To obtain higher voltage levels (more than 17), the proposed 17-level HMLI does not need any extra dc voltage source or capacitor balancing mechanism.

2.2 | Generalised structure of the proposed 17-level HMLI

The number of circuit components for generating $4n+1$ (n = number of capacitors) voltage levels (N_i) in generalised 17-level HMLI is given as

$$\begin{cases} N_{switch} = n + 7 \\ N_{diode} = 2n - 3 \\ N_{source} = 1 \end{cases} \quad (1)$$

where N_{source} , N_{switch} and N_{diode} are the number of dc sources, switches and diodes, respectively. The total blocking voltage (TBV) across the switches of the proposed HMLI is calculated by summing the respective PIV of each switch. The PIV across each switch is given in Table 2. For the HMLI, the TBV can be derived as follows:

$$TBV = \sum_{s=1}^S PIV \quad (2)$$

TABLE 2 Maximum voltage stress across switches

Device	PIV	Device	PIV/blocking voltage
S	V_{DC}	Q_2	$n \cdot V_{DC}$
S_2	V_{DC}	Q_3	$n \cdot V_{DC}$
S_{3i} ($i=2, \dots, n-3$)	$i \cdot V_{DC}$	Q_4	$n \cdot V_{DC}$
S_4	$(n-2) \cdot V_{DC}$	M_1	$V_{DC}/2$
S_5	$(n-1) \cdot V_{DC}$	M_2	$V_{DC}/2$
Q_1	$n \cdot V_{DC}$	S_3	V_{DC}

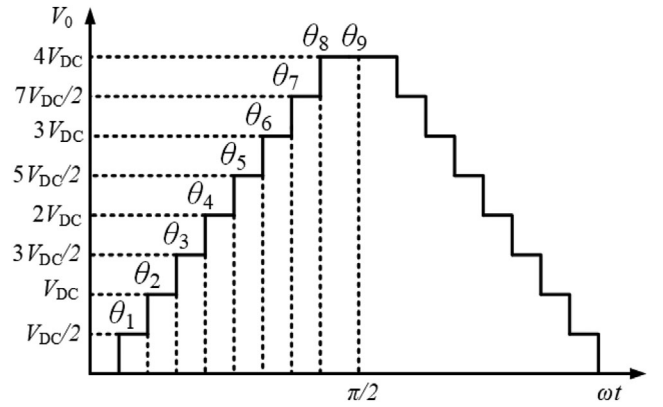


FIGURE 6 Switching angles of the proposed 17-level HMLI

Substituting the values as listed in Table 2 and generalising for HMLI with n capacitors:

$$TBV = \sum \left[V_{DC} + V_{DC} + \frac{(n-3)(n-2)V_{DC}}{2} + (n-2)V_{DC} + \frac{V_{DC}}{2} + (n-1)V_{DC} + 4nV_{DC} + \frac{V_{DC}}{2} + \frac{V_{DC}}{2} \right] \quad (3)$$

$$TBV = \left(\frac{n^2 + 7n + 6}{2} \right) \cdot V_{DC} \quad (4)$$

The per-unit TBV (TBV_{pu}) is derived as the ratio of TBV to maximum PIV across HMLI.

Substituting the values, TBV_{pu} is obtained as

$$TBV_{pu} = \left(\frac{n^2 + 7n + 6}{2n} \right) \cdot V_{DC} \quad (5)$$

3 | SWITCHING SCHEME

SHE switching method is applied using MGWO to obtain optimum switching angles for 17-level HMLI. Switching angles along with different voltage levels are shown in Figure 6.

The quasi-square output voltage waveform of the 17-level HMLI is given as

$$V_0 = \frac{V_{dc}}{2\pi} \sum_{k=1,3,\dots}^{\infty} \sum_{i=1}^8 \frac{\cos(k\theta_i)}{k} \sin k\omega t \quad (6)$$

where ω is the angular frequency.

The amplitude modulation index (M_{of}) is stated as

$$M_{of} = \frac{1}{8} \sum_{i=1}^8 \cos(\theta_i) \quad (7)$$

The switching angles for 17-level HMLI θ_i ($i = 1-8$) are obtained using

$$\begin{aligned} \cos \theta_1 + \cos \theta_2 + \cos \theta_3 + \cos \theta_4 + \cos \theta_5 + \cos \theta_6 + \cos \theta_7 \\ + \cos \theta_8 = 8M_{of} \cos(b\theta_1) + \cos(b\theta_2) + \cos(b\theta_3) \\ + \cos(b\theta_4) + \cos(b\theta_5) + \cos(b\theta_6) + \cos(b\theta_7) \\ + \cos(b\theta_8) = 0 \end{aligned} \quad (8)$$

where b is the number of harmonics to be eliminated from the output voltage. The harmonics such as 3rd, 5th, 7th, 9th, 11th, 13th and 15th are taken to obtain optimum switching angles.

3.1 | Modified GWO

In GWO, grey wolves are categorised into social ladders as α , β , δ and ω . In order to mathematically model the social hierarchy of wolves, α is considered as the fittest solution. Consequently, the second and third best solutions are named β and δ , respectively. The rest of the candidate solutions are assumed to be omega ω . The positions of grey wolves are updated using Equations (9) and (10), given as:

$$D = |\vec{C} \cdot \vec{X}_p(j) - \vec{X}(j)| \quad (9)$$

$$\vec{X}(j+1) = \vec{X}_p(j) - \vec{A} \cdot \vec{D} \quad (10)$$

where j is the current iteration; X : position vector of wolf; X_{pp} : position vector of prey, and A and C are coefficient vectors. The vector A is written as:

$$\vec{A} = 2\vec{a} \cdot \vec{r}_1 - \vec{a} \quad (11)$$

and vector C as:

$$\vec{C} = 2 \cdot \vec{r}_2 \quad (12)$$

where a is a coefficient vector; r_1 and r_2 are random vectors.

Generally, higher exploration of search space results in a lower probability of local optima stagnation. In order to further improve the convergence rate of the GWO algorithm, the

following modification (in co-efficient vector a) is employed to enhance the exploration–exploitation balance of GWO algorithm as follows:

$$a = \beta \cdot \exp(-\theta \times k) \quad (13)$$

where β and θ are two control parameters, which regulate the convergence behaviour of GWO algorithm over the iterations k for each point.

In addition, by converting the vector a to a random non-linear vector, both exploratory and accelerated convergence is achieved in the proposed MGWO algorithm.

Chaotic search technique is used for improved local search and stagnation of local minima [38]. Chaotic equation for local refinement is described as

$$x_{j+1} = \mu \cdot x_j (1 - x_j) \quad (14)$$

where x_j is a variable ($j = 0, 1, 2 \dots$) and μ is the control variable. The chaotic search is given as

$$cx_j^{n+1} = \mu \cdot cx_j^n (1 - cx_j^n) \quad (15)$$

where cx_j^n denotes the chaotic variable and n indicates iteration number.

The steps used for the searching mechanism is given as follows:

Step 1: The decision variables x_j^n ($x_{\min,j}, x_{\max,j}$) is mapped into chaotic variables cx_j^n using

$$cx_j^n = \frac{x_j^n - x_{\min,j}}{x_{\max,j} - x_{\min,j}} \quad (16)$$

Step 2: The chaotic variables cx_j^{n+1} are calculated for the next iteration using (14).

Step 3: The chaotic variables cx_j^{n+1} are converted to decision variables x_j^{n+1} using

$$x_j^{n+1} = x_{\min,j} + cx_j^{n+1} (x_{\max,j} - x_{\min,j}) \quad (17)$$

Step 4: New results are determined using the variable x_j^{n+1} .

Step 5: If the optimum result is obtained or maximum iterations are achieved, then the obtained optimum solution is taken as the final solution; or else, return to step 2.

To attain faster global optima, the position update equation is weighted in each iteration as given in Equation (20). The coefficient vectors are calculated using Equation (13) and A_1, A_2 and A_3 are obtained using Equation (11).

$$\begin{aligned} \vec{D}_\alpha &= |\vec{C}_1 \cdot \vec{X}_\alpha - \vec{X}| \\ \vec{D}_\beta &= |\vec{C}_2 \cdot \vec{X}_\beta - \vec{X}| \\ \vec{D}_\delta &= |\vec{C}_3 \cdot \vec{X}_\delta - \vec{X}| \end{aligned} \quad (18)$$

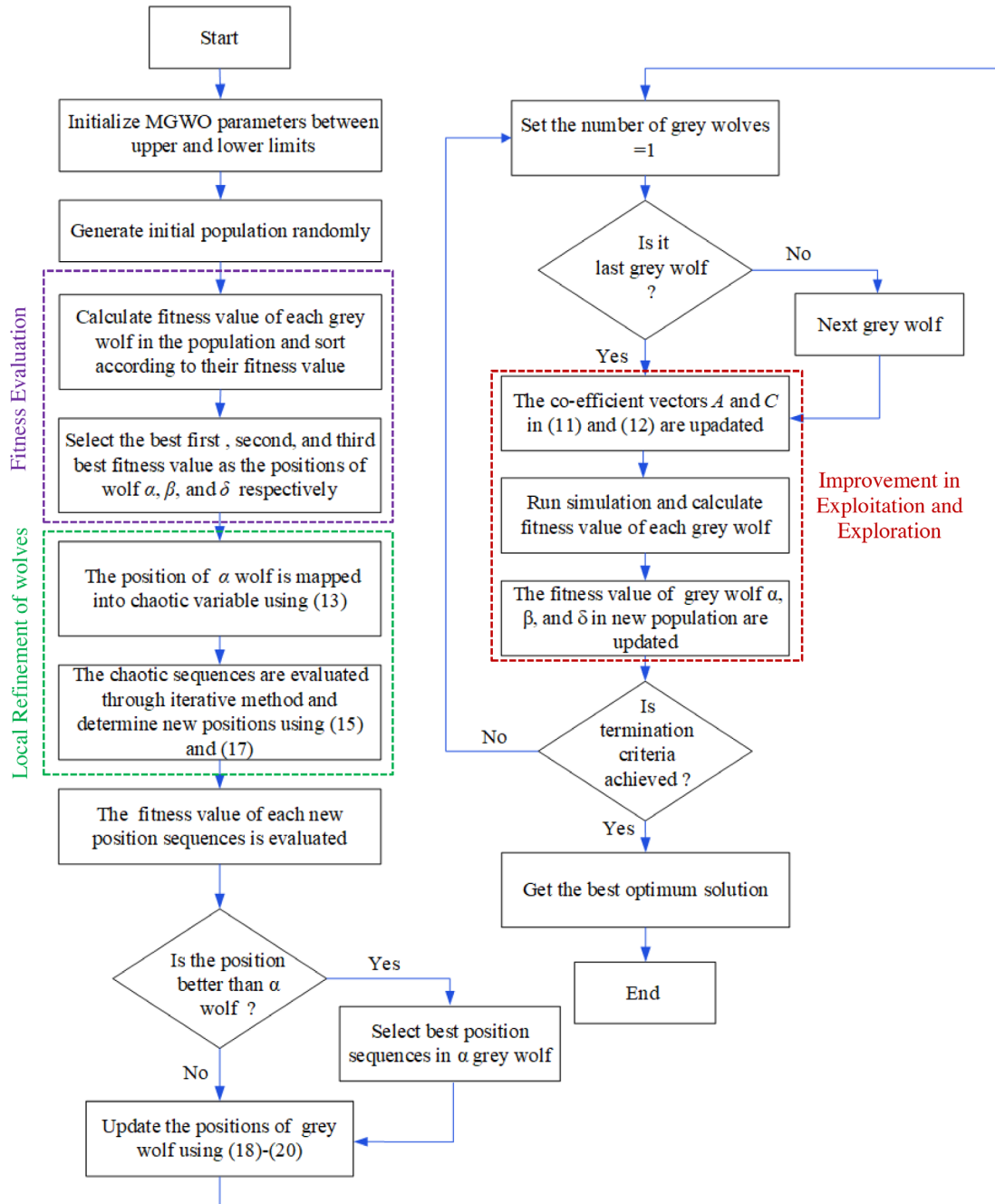


FIGURE 7 Flow chart of MGWO algorithm

$$\begin{aligned}\vec{X}_1 &= \vec{X}_\alpha - \vec{A}_1 \cdot \vec{D}_\alpha \\ \vec{X}_2 &= \vec{X}_\beta - \vec{A}_1 \cdot \vec{D}_\beta \\ \vec{X}_3 &= \vec{X}_\delta - \vec{A}_1 \cdot \vec{D}_\delta\end{aligned}\quad (19)$$

$$\vec{X}(j+1) = w_1 \cdot \vec{X}_1 + w_2 \cdot \vec{X}_2 + w_3 \cdot \vec{X}_3 \quad (20)$$

where w_1 , w_2 and w_3 are the corresponding weights.

The wolves update their position as an average of the three best grey wolves α , β and δ . This leads to premature conver-

gence. In order to overcome this demerit, the weighted distance criterion is employed to further improve the performance of the GWO algorithm. Therefore, Equation (20) is weighted in each iteration and is redefined as:

$$\begin{aligned}w_1 &= A_\alpha * C_\alpha, w_2 = A_\beta * C_\beta, w_3 = A_\delta * C_\delta \\ X(k+1) &= \frac{w_1 * X_1 + w_2 * X_2 + w_3 * X_3}{w_1 + w_2 + w_3}\end{aligned}\quad (21)$$

The weight of α , β and δ are denoted as w_1 , w_2 and w_3 . The weights should always satisfy $w_1 \geq w_2 \geq w_3$. Mathematically, the weight of α is changed from 1 to 1/3 during the searching

TABLE 3 Comparison at different parameters for $m_a = 0.7$

Parameter	MGWO	GWO	PSO	GA
Fitness value	6.4×10^{-33}	5.7×10^{-30}	4.3×10^{-28}	2.1×10^{-7}
Convergence rate	Very high	High	High	High

TABLE 4 Discharge interval (longest) for C_1

Interval	Current (i_0)
$\theta_3 \leq \theta \leq \theta_4$	$5V_{DC}/2R_L$
$\theta_4 \leq \theta \leq \theta_5$	$3V_{DC}/R_L$
$\theta_7 \leq \theta \leq \theta_8$	$7V_{DC}/2R_L$
$\theta_8 \leq \theta \leq \pi - \theta_8$	$4V_{DC}/R_L$

procedure. At the same time, the weights of the β and δ is increased to $1/3$ from 0. The complete flow chart of MGWO is depicted in Figure 7.

3.2 | Application of SHE using MGWO in the proposed 17-level HMLI

The objective function f used for SHE in the proposed HMLI is given as

$$f = \min \left\{ \left(100 \frac{V_1^* - V_1}{V_1^*} \right)^4 + \sum_{s=3}^{N_f-2} \frac{1}{b_s} \left(50 \frac{V_{b_s}}{V_1} \right)^2 \right\} \quad (22)$$

subjected to

$$0 \leq \theta_1 \leq \theta_2 \dots \theta_n < \frac{\pi}{2} \quad (23)$$

where b_s is the S_{th} harmonic order. V_1^* represents reference value of the fundamental component of output voltage. The population size = 100, iterations = 200 and parameters $\theta = 0.8$ and $\beta = 2.2$ are taken. MGWO is run in MATLAB/Simulink till the algorithm terminates. The graph of optimum all switching angles with modulation index (m_a) is depicted in Figure 8a. The plot of fitness value against different values of m_a for GA, PSO, GWO and MGWO algorithms are shown in Figure 8b. Cumulative distribution function (CDF) is determined for usefulness of reported algorithms [39]. The comparison CDF of reported optimisation methods is shown in Figure 8c. It can be concluded from Figure 8c that MGWO has a faster convergence rate as compared to GWO, PSO and GA for the same number of iterations and population size. Total harmonic distortion (%THD) of algorithms for different m_a is calculated considering harmonics order up to 20 and are shown in Figure 8d. MGWO optimised HMLI gives lesser harmonic content as compared to other reported algorithms discussed in this work. The fitness value and the rate of convergence of all algorithms are compared and given in Table 3. The convergence rate and fitness value of MGWO are better than GA, PSO and GWO.

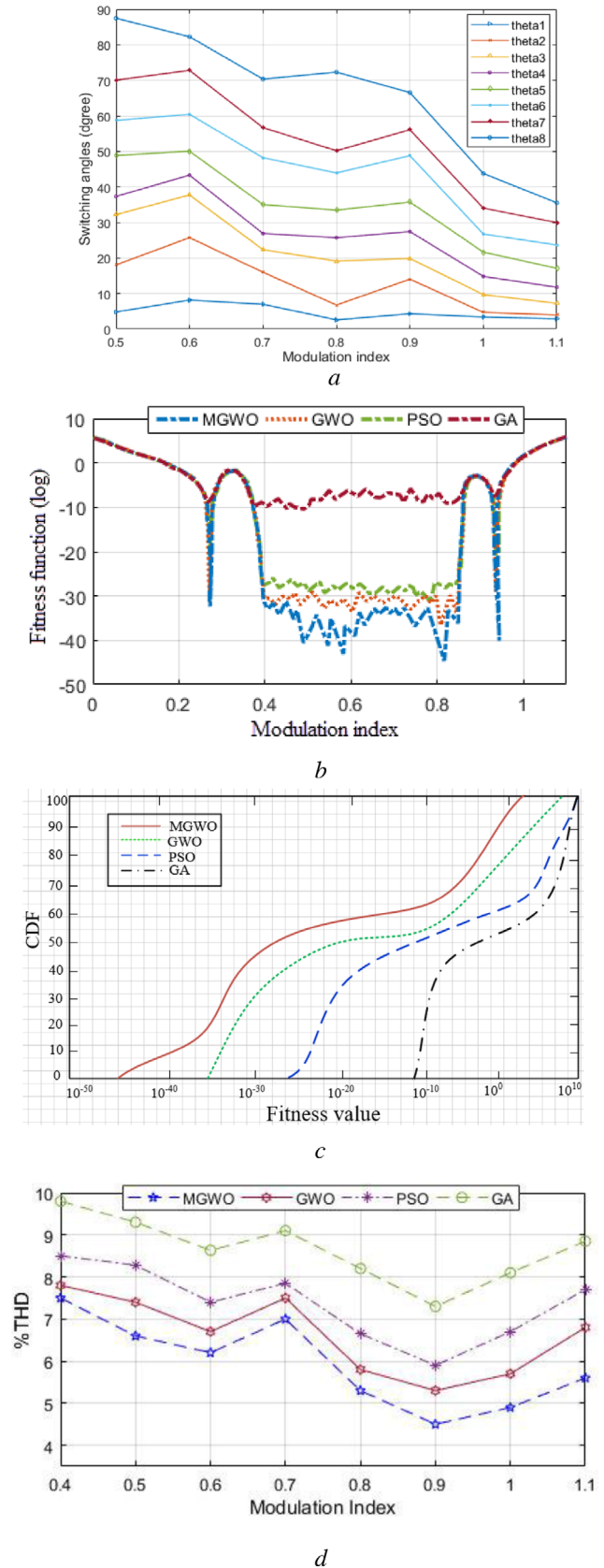


FIGURE 8 Obtained optimal switching angles, fitness value, CDF and %THD for MGWO, GWO, PSO and GA: (a) switching angles against m_a , (b) fitness values against m_a , (c) CDF with fitness values (probability of convergence), (d) %THD against m_a

4 | CAPACITOR CALCULATION

To calculate capacitances, the charge-discharge cycle of each capacitor is considered [16]. For demonstration, the largest discharge period is calculated for C_1 . The largest discharge interval and the corresponding currents through resistive load R_L for these intervals are calculated to define total charge and are given in Table 4.

The maximum discharging value Q_{C_1} of capacitor C_1 is calculated based on discharge cycles and is given as:

$$Q_{C_1} = \frac{1}{\omega} \left[\int_{\theta_3}^{\theta_4} i_o d\theta + \int_{\theta_4}^{\theta_5} i_o d\theta + \int_{\theta_7}^{\theta_8} i_o d\theta + \int_{\theta_8}^{\pi-\theta_8} i_o d\theta \right] \quad (24)$$

Similarly, the maximum discharging values Q_{C_2} , Q_{C_3} and Q_{C_4} of the capacitors C_2 , C_3 and C_4 can be obtained. The maximum allowable voltage ripples across the capacitor C_i is kV_{C_i} ($i = 1, 2, 3$ and 4), where k is the ripple factor. Using the derived values of Q_{C_1} , Q_{C_2} and Q_{C_3} , the values of capacitors C_1 , C_2 , C_3 and C_4 are obtained as:

$$C_1 \geq \frac{(4\pi - 3\theta_3 - \theta_4 + 4\theta_5 - 7\theta_7 - \theta_8)}{2\pi f_s k R_L} \quad (25)$$

$$C_2, C_3 \geq \frac{(4\pi - 5\theta_5 - \theta_6 - \theta_7 - \theta_8)}{2\pi f_s k R_L} \quad (26)$$

$$C_4 \geq \frac{(\theta_2 - \theta_1 - 3\theta_3 + 3\theta_4 - 5\theta_5 + 5\theta_6 - 7\theta_7 + 7\theta_8)}{2\pi f_s k R_L} \quad (27)$$

The function of load current, $I_L(t)$ for R - L loading condition is derived [16] as:

$$I_L(t) = I_{\max} \sin(\omega t - \phi) \quad (28)$$

here I_{\max} is maximum load current and ϕ is phase difference. The capacitances for inductive load are given as:

$$C_1 \geq \frac{2I_{\max} \left(\cos(\theta_3 - \Phi) + \cos(\theta_7 - \Phi) \right)}{2\pi f_s k V_{DC}} \quad (29)$$

$$C_2, C_3 \geq \frac{2I_{\max} \left(\cos(\theta_5 - \Phi) - \sin(\Phi) \right)}{2\pi f_s k V_{DC}} \quad (30)$$

$$C_4 \geq \frac{I_{\max} \left(\begin{array}{l} \cos(\theta_4 - \Phi) - \cos(\theta_3 - \Phi) + \cos(\theta_2 - \Phi) \\ - \cos(\theta_1 - \Phi) + \cos(\theta_6 - \Phi) - \cos(\theta_5 - \Phi) \\ + \cos(1.5\pi) - \cos(\theta_7 - \Phi) \end{array} \right)}{2\pi f_s k V_{DC}} \quad (31)$$

For voltage ripple $k = 0.05$ and 0.1 , the optimal capacitor values can be determined from Equations (29)–(31). The capacitor values are inversely varying with ripple factor and output frequency. The variations of C_1 , C_2 , C_3 and C_4 for several ranges of load values are depicted in Figure 9a to validate the effect of

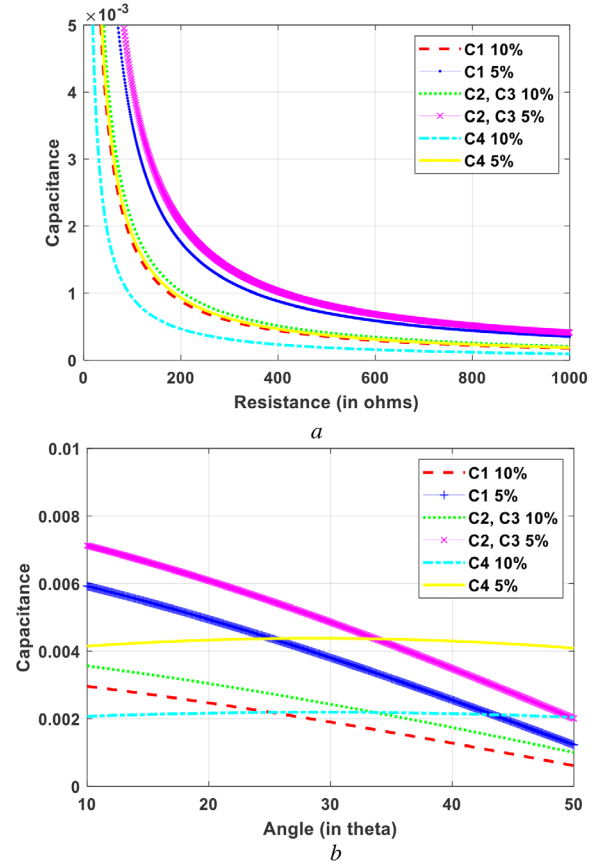


FIGURE 9 Optimal values of capacitance: (a) at changing load resistance, (b) at changing phase angles

TABLE 5 Comparison of HMLI with reported topologies for 17 output levels

Parameter	[15]	[16]	[17]	[20]	[22]	[24]	[25]	[13]	[14]	HMLI
N_{Switch}	12	25	25	39	29	26	16	64	32	11
N_{Cap}	7	7	7	7	8	8	6	32	16	4
N_{Diode}	14	0	0	0	0	1	6	32	0	5
TBV _{sw}	96	53	72	39	54	27	25	64	32	25.5
TBV _{diode}	49	0	0	0	0	0	4.5	32	0	6
TBV _{total}	145	53	72	39	54	96	29.5	96	32	31.5
PIV	8	8	8	1	4	4	4	4	4	4

load resistance on optimum capacitance. The optimum capacitor values are also determined for different values of phase angle as shown in Figure 9b.

5 | COMPARISON WITH REPORTED HMLIs

The proposed 17-level HMLI is compared with recently reported MLIs. The proposed HMLI is compared in terms of active and passive components, PIV and TBV to exhibit its merits as given in Table 5.

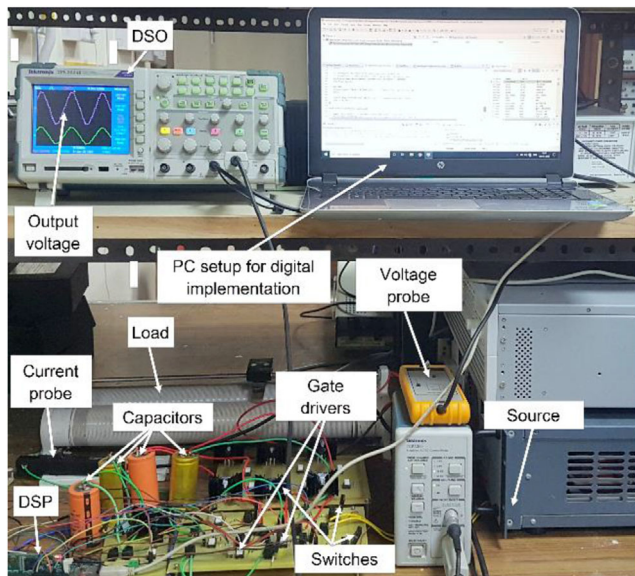


FIGURE 10 Experimental results of the proposed 17-level HMLI: (a) v_0 and i_0 for resistive load ($R = 45 \Omega$), (b) v_0 and i_0 for inductive load ($R = 45 \Omega$, $L = 90$ mH), (c) harmonic spectral analysis v_0

It can be observed from Table 5 that the proposed HMLI requires a lesser number of capacitors to achieve 17-level output voltage as compared to other HMLIs. Topologies [15], [16], [17], [22], [24] and [25] utilise almost twice the number of capacitors compared to the proposed topology for the same number of voltage levels attained. The number of capacitors in [13] and [14] is also very high to generate 17-level voltage levels. However, the proposed HMLI requires a lesser number of power devices as compared to others as given in Table 5. The topology [14] requires zero number of diodes but the number of capacitors is very high. Topology presented in [17], [24] and [15] possess larger TBV for obtaining a higher number of levels whereas topologies [15] and [25] need more diodes to generate the same output voltage levels. While topology [28] has lower PIV and the number of capacitors for generating a similar number of output voltage levels as HMLI, it has very limited boosting capacity with the maximum boosting possible as two and uses a higher number of switching devices than HMLI.

6 | EXPERIMENTAL VERIFICATION

In order to validate the performance of the proposed 17-level HMLI, a 550 W laboratory prototype is developed as shown in Figure 10 and the required components are given in Table 6. The dc source voltage is taken as 60 V and the experimentation is carried out using TI-TMS320F28335 DSP processor. The switching angles for the proposed 17-level HMLI for modulation index 0.7 are obtained as: $\theta_1 = 7.52$, $\theta_2 = 14.53$, $\theta_3 = 19.79$, $\theta_4 = 27.86$, $\theta_5 = 36.13$, $\theta_6 = 49.13$, $\theta_7 = 55.87$, $\theta_8 = 67.31$. For 10% capacitor ripple voltage and load resistance $R = 45 \Omega$, the respective capacitance values (C_1 , C_2 , C_3 and C_4) are calculated using Equations (29)–(31) and are obtained as approxi-

TABLE 6 Devices and parameters used

Microcontroller	TI-TMS320F28335
IGBT	HGTG12N60A4D
Gate driver	FOD3184
Diode	STP516150

TABLE 7 Harmonics order at $m_a = 0.7$

Harmonics order (h_s)	MGWO	GWO	PSO	GA
3rd	0.7116	0.8325	0.9834	1.2254
5th	0.4137	0.7431	0.8157	0.9767
7th	0.3539	0.9876	1.0625	1.2652
9th	2.1306	2.3241	2.4105	2.6834
11th	1.0652	1.4637	2.0855	2.5163
13th	0.2872	0.7205	1.0236	1.1154
15th	1.2147	1.5358	1.7462	2.1371

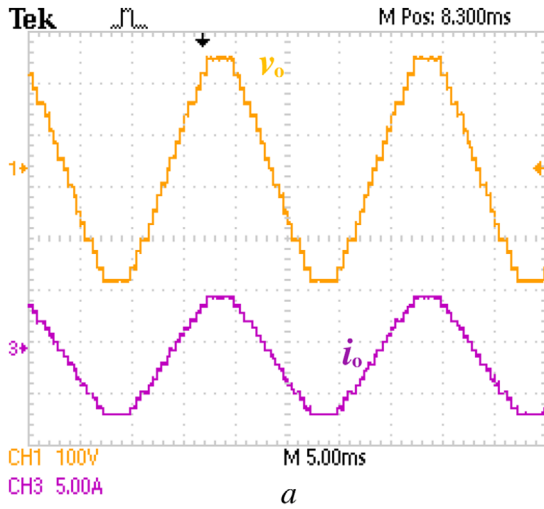
mately 2200, 2600, 2600 and 1500 μF , respectively. The output voltage V_0 and current I_0 experimental waveforms of the proposed 17-level HMLI for a resistive load ($R = 45 \Omega$) are shown in Figure 10a. The measured rms values of output voltage and current are 158.43 V and 3.47 A, respectively. The topology is also tested for R - L load ($R = 45 \Omega$, $L = 90$ mH) at input voltage 60 V. The output voltage V_0 and current I_0 are depicted in Figure 10b and measured as 158 V and 3.09 A, respectively. The harmonic spectrum of the V_0 is depicted in Figure 10c and %THD is measured as 7.14%.

The magnitude of lower order harmonics at m_a 0.7 for GA PSO, GWO and MGWO are given in Table 7. It can be noticed that magnitude of lower order harmonics in the output voltage of HMLI has been reduced significantly using MGWO technique as compared to other reported algorithms.

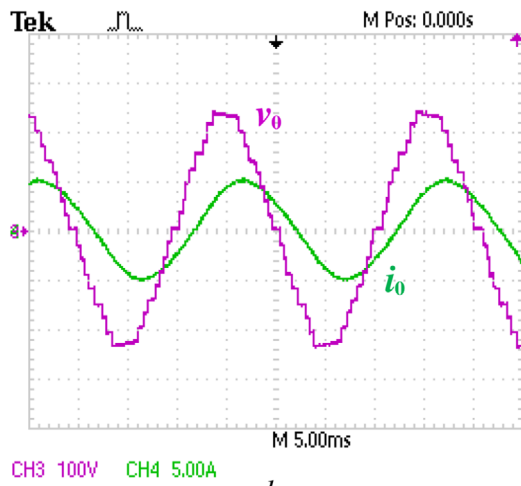
The capacitor voltages are shown in Figure 11. It can be observed that capacitor voltages V_{C1} , V_{C2} , V_{C3} and V_{C4} are balanced at 56.5, 57.1, 56.2 and 27.5 V, respectively. The voltage of capacitors is inherently self-balanced in the proposed HMLI. Capacitor ripples ΔV_{C1} , ΔV_{C2} , ΔV_{C3} and ΔV_{C4} across the four capacitors are 5.4, 5.1, 4.8 and 2.6 V, respectively.

6.1 | Dynamic performance of the proposed HMLI

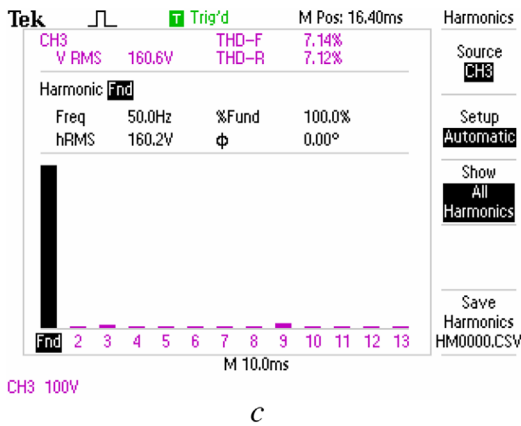
In order to verify the dynamic performance of the proposed HMLI, the load resistance is step changed from 45 to 90 Ω . The load current is step changed from 3.4 to 1.6 A for variation in resistance as depicted in Figure 12. It can be noticed that the output voltage does not have any significant effect for the change in load resistance. Therefore, the inherent capacitor voltage balance is confirmed in the 17-level proposed HMLI.



a



b



c

FIGURE 11 Experimental result of capacitor voltages: (a) v_o and i_o for resistive load ($R = 45 \Omega$), (b) v_o and i_o for inductive load ($R = 45 \Omega$, $L = 90 \text{ mH}$), (c) harmonic spectral analysis v_o

6.2 | Efficiency calculation

In order to calculate the efficiency of HMLI, V_{in} (input voltage), I_{in} (input current), V_o and I_o for R load ($R = 45 \Omega$) are measured experimentally from Figure 13. The calculated

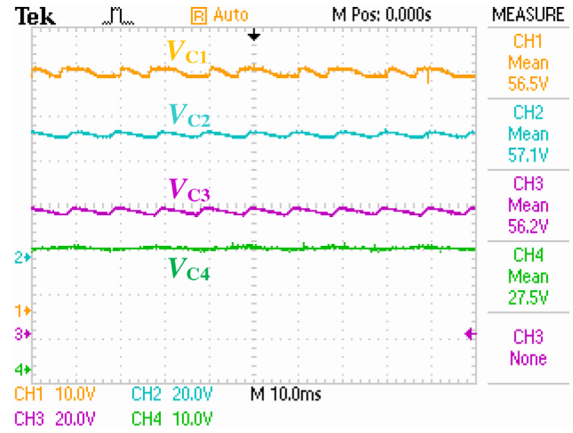


FIGURE 12 Experimental result of capacitor voltages

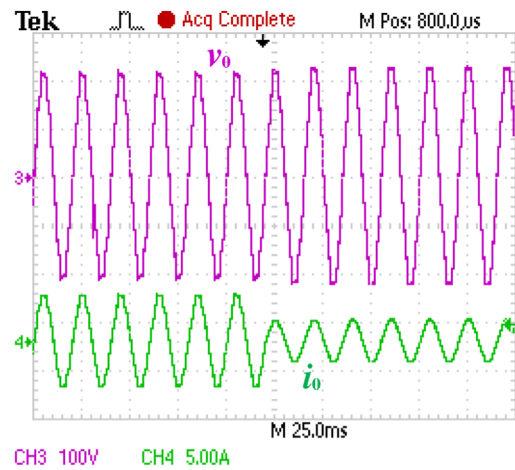


FIGURE 13 Dynamic behaviour of HMLI for step change in load resistance

input and output power and loss are given as $P_{in} = 601.07 \text{ W}$, $P_{out} = 548.66 \text{ W}$ and $P_{loss} = 52.41 \text{ W}$, respectively. Hence, the obtained efficiency for 550 W HMLI is approximately 91.28%.

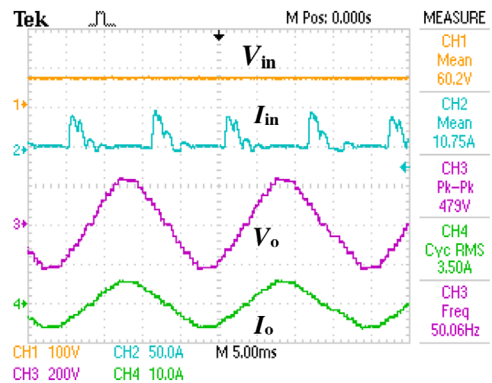


FIGURE 14 Input voltage, current and output voltage, current for R load ($R = 45 \Omega$) of HMLI

7 | CONCLUSION

A 17-level HMLI using a reduced number of circuit components is proposed in this paper. TBV of the proposed HMLI is low, thus enabling utilisation of lower-rated switches for higher power level applications. The proposed topology has reverse current carrying capability. Output voltage levels higher than 17 can also be obtained using the extended structure of the proposed HMLI. Capacitor voltages are inherently balanced in the proposed HMLI, thus it eliminates the requirement of any external capacitor balancing circuit. MGWO algorithm has been used to obtain optimal switching angles of HMLI by solving non-linear transcendental equations in this work. MGWO gives superior performance in terms of harmonic content, convergence speed and fitness value as compared to GA, PSO and GWO due to its improved local optima and ability to balance between exploration and exploitation. In order to verify the effectiveness of the proposed HMLI, a 550 W laboratory prototype has been developed and the obtained experimental results verify the precision of the proposed work.

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APPENDIX

The mathematical voltage balance of capacitor C_4 is derived below. The output voltage and current are assumed to have half-wave symmetry. The average current through C_4 for load resistance as R is given as follows:

$$\begin{aligned}
 I_{C, \frac{7V_{dc}}{2}}^+ &= \frac{4V_{dc}-V_{C_4}}{R_L} & I_{C, \frac{5V_{dc}}{2}}^+ &= \frac{3V_{dc}-V_{C_4}}{R_L} & I_{C, \frac{3V_{dc}}{2}}^+ &= \frac{2V_{dc}-V_{C_4}}{R_L} \\
 I_{C, \frac{V_{dc}}{2}}^+ &= \frac{V_{dc}-V_{C_4}}{R_L} & I_{C, \frac{V_{dc}}{2}}^- &= \frac{-V_{C_4}}{R_L} & I_{C, \frac{3V_{dc}}{2}}^- &= \frac{-V_{dc}-V_{C_4}}{R_L} \\
 I_{C, \frac{5V_{dc}}{2}}^- &= \frac{-2V_{dc}-V_{C_4}}{R_L} & I_{C, \frac{7V_{dc}}{2}}^- &= \frac{-3V_{dc}-V_{C_4}}{R_L}
 \end{aligned}$$

where I_C^+ and I_C^- are current flow through capacitor (C_4) in both the half cycle of output voltage. The total charge Q delivered/absorbed over a period T is calculated as follows:

$$\begin{aligned}
 Q &= I_{C, \frac{7V_{dc}}{2}}^+ \cdot \left(\frac{\theta_8 - \theta_7}{\pi}\right) \cdot T + I_{C, \frac{5V_{dc}}{2}}^+ \cdot \left(\frac{\theta_6 - \theta_5}{\pi}\right) \cdot T \\
 &+ I_{C, \frac{3V_{dc}}{2}}^+ \cdot \left(\frac{\theta_4 - \theta_3}{\pi}\right) \cdot T + I_{C, \frac{V_{dc}}{2}}^+ \cdot \left(\frac{\theta_2 - \theta_1}{\pi}\right) \cdot T \\
 &+ I_{C, \frac{3V_{dc}}{2}}^- \cdot \left(\frac{\theta_4 - \theta_3}{\pi}\right) \cdot T \\
 &+ I_{C, \frac{5V_{dc}}{2}}^- \cdot \left(\frac{\theta_6 - \theta_5}{\pi}\right) \cdot T + I_{C, \frac{7V_{dc}}{2}}^- \cdot \left(\frac{\theta_8 - \theta_7}{\pi}\right) \cdot T \quad (32) \\
 Q &= \left(\frac{V_{DC} - 2V_{C_4}}{R_L}\right) \\
 &\cdot \left(\frac{\theta_8 - \theta_7 + \theta_6 - \theta_5 + \theta_4 - \theta_3 + \theta_2 - \theta_1}{\pi}\right) \cdot T \\
 V_{C_4} &= \frac{V_{DC}}{2} \quad (33)
 \end{aligned}$$