Chapter 6

SB-USMC with reduced CMV

6.1 Introduction

In the preceding chapter, SB-USMC was introduced, featuring improved voltage gain with fewer passive elements. At the same time, the previous chapter covered aspects such as the working operation of SB-USMC, boosting factor calculation and impedance network design, load power factor analysis, and the relation of the voltage gain with various parameters. The control of switches in the SB-USMC was achieved through the conventional SVM method. This chapter focuses on calculating CMV in SB-USMC and analyzing peak CMV in SVM sectors. This chapter introduces a new SVM method called Three Vector SVM (TVSVM) to minimize the CMV in SB-USMC and also provides the relation between CMV and shoot-through time period. The switching sequence of the conventional SVM used for the SB-USMC is shown in Figure 6.1. This method uses active vectors states, zero vectors states and shoot-through states to complete the switching strategy. The calculation of CMV in each state is given below:

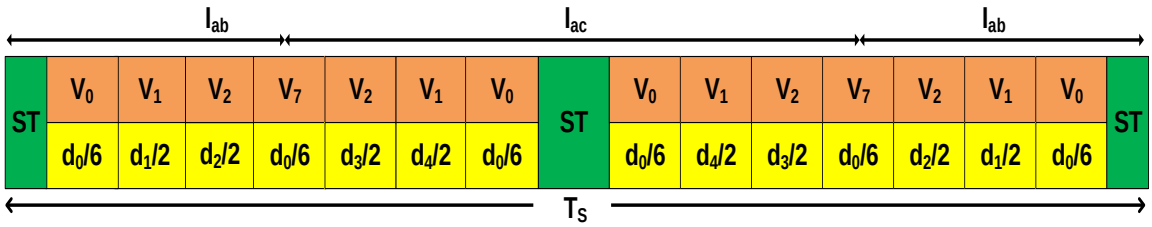


Figure 6.1: Switching strategy for the SB-USMC converter

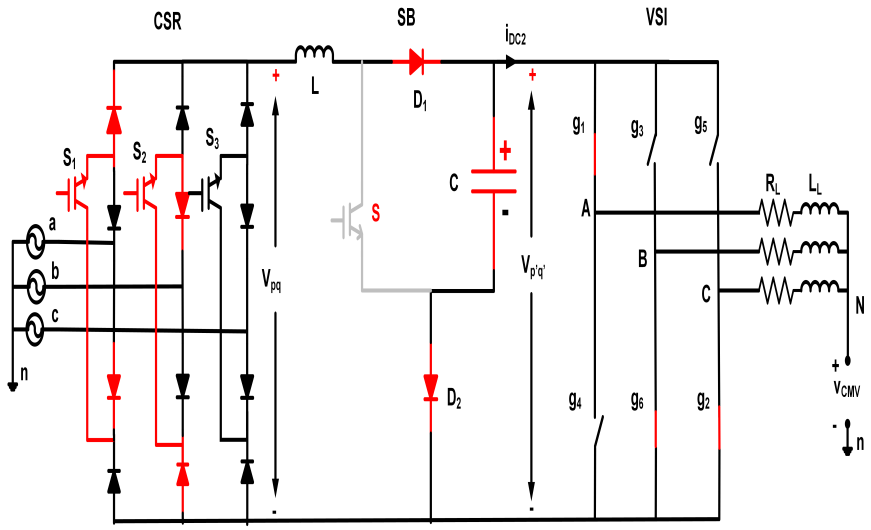


Figure 6.2: Equivalent circuit of the SB-USMC under both CSR and VSI are in sector 1

6.1.1 Calculation of CMV in SB-USMC for the conventional SVM

To calculate the CMV of the SB-USMC, consider three-phase RL load connected to the converter, as shown in Figure 6.2. From the circuit diagram, the following KVL equations can be written as

$$\begin{aligned} v_{An} &= R_L i_A + L_L \frac{di_A}{dt} + v_{CMV} \\ v_{Bn} &= R_L i_B + L_L \frac{di_B}{dt} + v_{CMV} \\ v_{Cn} &= R_L i_C + L_L \frac{di_C}{dt} + v_{CMV} \end{aligned} \tag{6.1}$$

Here v_{An}, v_{Bn}, v_{Cn} are output voltages with respect to the ground 'n'. For balanced three phase currents $i_A + i_B + i_C = 0$. Hence using equation (6.1),the CMV (v_{CMV}) is

$$v_{CMV} = \frac{v_{An} + v_{Bn} + v_{Cn}}{3} \tag{6.2}$$

From equation (6.2), CMV depends on the instantaneous values of the three phase output voltages. These instantaneous values of the three phase output voltages differ for different switching states. In the SVM technique, only active vectors are used at the CSR side and both active and zero vectors are used at the VSI side. For switching state I_{ab}, $V_1(pnn)$ (both CSR and VSI are in sector 1), switches S_1, S_2, g_1, g_2, and g_6

are switching ON, as shown in Figure 6.2. The output voltages are

$$\begin{aligned} v_{An} &= v_b + V_C \\ v_{Bn} &= v_b \\ v_{Cn} &= v_b \end{aligned} \tag{6.3}$$

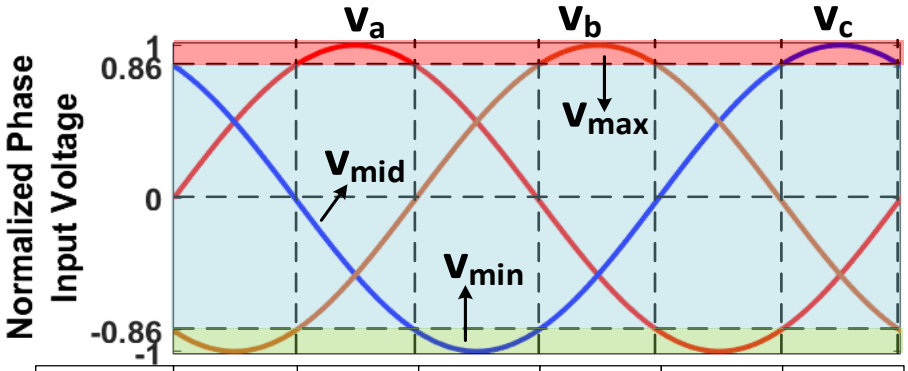
Here v_a, v_b, v_c are the input supply voltages and $V_C = V_{p'q'}$ is the voltage across capacitor. From equations (6.2) and (6.3) the CMV can be calculated as

$$v_{CMV} = v_b + \frac{V_{p'q'}}{3} \tag{6.4}$$

Similarly, for the active vectors I_{ab} and $V_2(ppn)$ switches S_1, S_2, g_1, g_2, and g_3 are switching ON. The output voltages the CMV for this switching state are

$$\begin{aligned} v_A &= v_b + V_{p'q'} \\ v_B &= v_b + V_{p'q'} \\ v_C &= v_b \\ v_{CMV} &= v_b + \frac{2V_{p'q'}}{3} \end{aligned} \tag{6.5}$$

From equations (6.4) and (6.5), the magnitude of the CMV depends on the magnitudes of input voltage and boosted voltage. The input voltage magnitude varies with CSR sectors as shown in Figure 6.3. From Figure 6.3, in sector 1 the input voltage v_b varies from $-\frac{\sqrt{3}}{2}\hat{V}_m$ to 0 V, $\hat{V}_m$ is the peak magnitude of the input voltage. So maximum



CSR sector	6	1	2	3	4	5
Clamp	S_2	S_1	S_3	S_2	S_1	S_3
Switching	S_1, S_3	S_2, S_3	S_1, S_2	S_1, S_3	S_2, S_3	S_1, S_2

Figure 6.3: Input voltage variation through CSR sectors

CMV in $I_{ab}V_2(ppn)$ switching states is

$$v_{CMVmax1} = \frac{2V_{p'q'}}{3} \tag{6.6}$$

Similarly remaining states CMV is calculated and provided in Table 6.1. From this information, the maximum CMV presented in the converter is

$$v_{CMVmax} = V_{p'q'} \tag{6.7}$$

Which is caused by VSI zero vector V_7. From Table 6.1 information, CMV magnitude

Table 6.1: CMV for CSR and VSI switching states (conventional)

CSR sector	VSI switching states	CMV	peak of the CMV
1,3,5	V_1, V_3, V_5	$\frac{3v_{mid}+V_{p'q'}}{3}$	$\frac{V_{p'q'}}{3}$
	V_2, V_4, V_6	$\frac{3v_{mid}+2V_{p'q'}}{3}$	$\frac{2V_{p'q'}}{3}$
	V_0	v_{mid}	$\frac{-\sqrt{3}\hat{V}_m}{2}$
	V_7	$\frac{3v_{mid}+3V_{p'q'}}{3}$	$V_{p'q'}$
	ST	v_{mid}	$\frac{-\sqrt{3}\hat{V}_m}{2}$
2, 4, 6	V_1, V_3, V_5	$\frac{3v_{min}+V_{p'q'}}{3}$	$\frac{-\sqrt{3}\hat{V}_m}{2} + \frac{V_{p'q'}}{3}$
	V_2, V_4, V_6	$\frac{3V_{min}+V_{p'q'}}{3}$	$\frac{-\sqrt{3}\hat{V}_m}{2} + \frac{V_{p'q'}}{3}$
	V_0	v_{min}	$-\hat{V}_m$
	V_7	$v_{min} + V_{p'q'}$	$\frac{-\sqrt{3}\hat{V}_m}{2} + V_{p'q'}$
	ST	v_{min}	$-\hat{V}_m$

is higher in zero vectors. So, to minimize the peak CMV in the SB-USMC, two modulation techniques, Three Vector Space Vector Modulation-1 (TVSVM-I) and Three Vector Space Vector Modulation-II (TVSVM-II) technique are implemented.

6.2 SB-USMC with TVSVM-I method

This modulation technique is similar to the [73], but it is implemented in the SB-USMC for the first time. In the TVSVM-I method, the CSR current reference vector is synthesized by two active vectors, and three active vectors synthesize the VSI voltage reference vector. Space vector diagrams for both CSR and VSI are shown in Figure

6.4(a) and Figure 6.4(b), respectively. The switching strategy of the TVSVM-I method is shown in Figure 6.9. Each state Duty periods are calculated using equation (6.8).

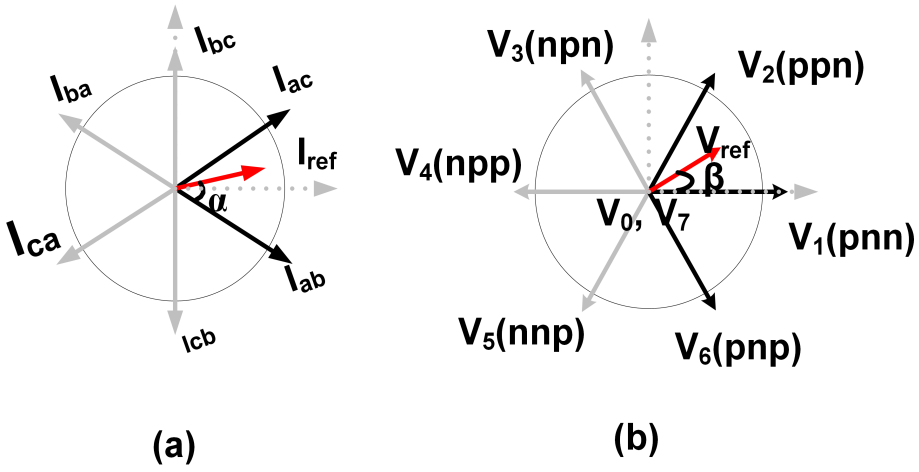


Figure 6.4: CSR and VSI space vector diagrams for TVSVM-I

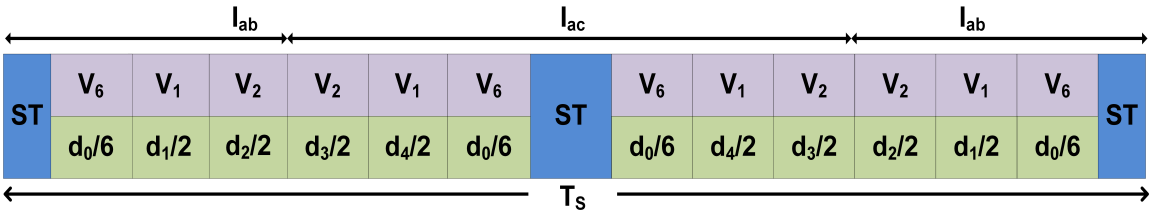


Figure 6.5: Switching strategy for TVSVM-I

$$
\begin{aligned}
dI_{ab} &= m_i sin(\frac{\pi}{3} - \alpha), \quad dI_{ac} = m_i sin(\alpha) \\
V_{ref} &= d_{V1} \times V_1 + d_{V2} \times V_2 + d_{V0} \times V_6 \\
1 &= d_{V1} + d_{V2} + d_{V6} \\
d_{V1} &= -1 + \sqrt{3} m_v cos(\beta) \\
d_{V2} &= 1 - m_v cos(\frac{\pi}{6} + \beta) \\
d_0 &= d_{V0} = 1 - m_v cos(\frac{\pi}{6} - \beta) \\
d_1 &= dI_{ab} \times d_{V1}, \quad d_2 = dI_{ab} \times d_{V2} \\
d_3 &= dI_{ac} \times d_{V2}, \quad d_4 = dI_{ac} \times d_{V1}
\end{aligned}
\tag{6.8}
$$

The boosting operation of the TVSVM-I is the same as the conventional SVM. Table 6.2 provides the peak CMV information for the TVSVM-I method. The maximum peak CMV obtained from this method is

$$v_{CMV(max)} = \frac{2V_{p'q'}}{3} \tag{6.9}$$

Percentage reduction of CMV by using TVSVM-I is given in equation (6.10).

Table 6.2: CMV for CSR and VSI switching states (TVSVM-I)

CSR sector	VSI switching states	CMV	peak of the CMV
1,3,5	V_1, V_3, V_5	$\frac{3v_{mid}+V_{p'q'}}{3}$	$\frac{V_{p'q'}}{3}$
	V_2, V_4, V_6	$\frac{3v_{mid}+2V_{p'q'}}{3}$	$\frac{2V_{p'q'}}{3}$
	ST	v_{mid}	$\frac{-\sqrt{3}\hat{V}_m}{2}$
2, 4, 6	V_1, V_3, V_5	$\frac{3v_{min}+V_{p'q'}}{3}$	$\frac{-\sqrt{3}\hat{V}_m}{2} + \frac{V_{p'q'}}{3}$
	V_2, V_4, V_6	$\frac{3V_{min}+V_{p'q'}}{3}$	$\frac{-\sqrt{3}\hat{V}_m}{2} + \frac{V_{p'q'}}{3}$
	ST	v_{min}	$-\hat{V}_m$

$$\begin{aligned} \%CMV_{reduced} &= \frac{v_{CMVmax} - v_{CMV(max)}}{v_{CMVmax}} \\ &= 33\% \end{aligned} \tag{6.10}$$

6.3 SB-USMC with TVSVM-II method

In this proposed TVSVM-II, three active vectors at CSR and two at VSI are selected for the switching sequence to reduce the CMV. SVM for CSR consists of six active vectors $[I_{ab}, I_{bc}, I_{ca}, I_{ba}, I_{cb}, I_{ac},]$ with six sectors as shown in Figure 6.6(a). Three neighbor

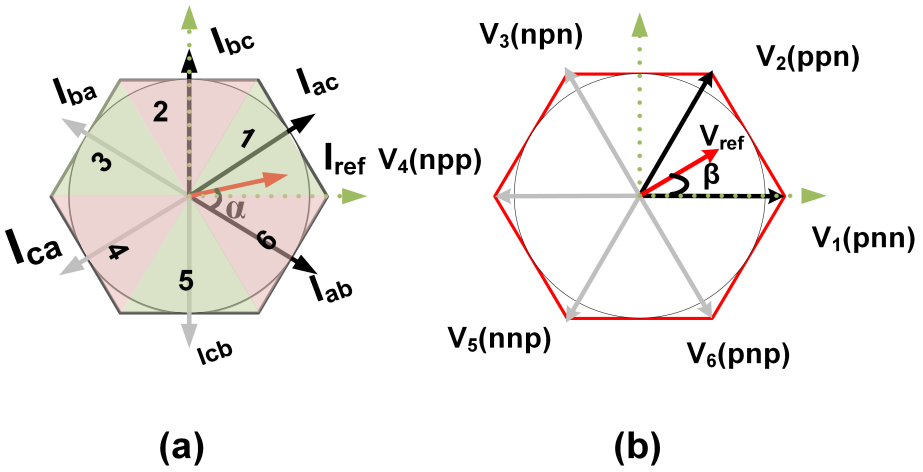


Figure 6.6: CSR and VSI space vector diagrams for TVSVM

active vectors can synthesize the reference current vector I_{ref}. The VSI space vector diagram has six active vectors $[V_1, V_2, V_3, V_4, V_5, V_6]$ with six sectors as shown in Figure

6.6(b). Two active vectors can synthesize the output voltage vector V_{ref}. For instance, consider the reference vectors are in sector 1, then CSR active vectors are I_{ab}, I_{ac} and I_{bc} and VSI active vectors are V_1 and V_2. Duty ratios for CSR and VSI vectors are given in equation (6.11).

$$\begin{aligned} I_{ref} &= dI_\mu \times I_{ab} + dI_\nu \times I_{ac} + d_0 \times I_{bc} \\ dI_\mu &= 1 - sin(\alpha + \frac{\pi}{6}) \\ dI_\nu &= -1 + \sqrt{3} sin(\alpha + \frac{\pi}{3}) \\ V_{ref} &= dV_1 \times V_1 + dV_2 \times V_2 \\ dV_1 &= m\frac{sin(\frac{\pi}{3} - \beta)}{cos(\beta - \frac{\pi}{6})}, \quad dV_2 = m\frac{sin(\beta)}{cos(\beta - \frac{\pi}{6})} \end{aligned} \tag{6.11}$$

α is the CSR vector angle in sector 1 and, β is the VSI vector angle in sector 1. m is the modulation index. Synchronization among CSR switches, switched network switch, and VSI switches are necessary for implementing SVM in SB-USMC. This synchronization can be done by multiplying CSR active vector duty ratios with VSI active vector duty ratios.

$$\begin{aligned} d_1 &= dI_\mu \times dV_1, \quad d_2 = dI_\mu \times dV_2 \\ d_3 &= dI_\nu \times dV_2, \quad d_4 = dI_\nu \times dV_1 \\ d_0 &= 1 - d_1 - d_2 - d_3 - d_4 \\ d_{01} &= d_0 dV_1 \quad d_{02} = d_0 dV_2, \quad m + d_{st} \leq 1 \end{aligned} \tag{6.12}$$

For instance, Figure 6.7 shows the switching sequence of the proposed topology for both CSR and VSI in sector 1. The sequence starts with switching ON S_1, S_2 (I_{ab}) in CSR and g_1, g_2, g_6 (V_1 state) in VSI while the impedance network switch (S) is OFF. After $\frac{d_1}{2}$, VSI changes state to V_2 by switching ON g_3. After $\frac{d_1}{2} + \frac{d_2}{2}$, the shoot-through (ST) state is applied by switching on S and shorting the VSI leg. Similarly, all switching states are arranged in one cycle (T_S). The CSR and VSI switching sequences are repeated after $\frac{T_S}{2}$ to improve the input and output. The SB-USMC duty ratios in sector 1 are given in equation (6.12). After applying this switching strategy, the obtained average DC-link voltage (V_{pq}) for three-phase balanced input supply $\hat{V}_m$ is given by equation (6.13).

$$V_{pq} = dI_\mu(V_{ab}) + dI_\nu(V_{ac}) + d_0(V_{bc}) = \frac{3\hat{V}_m}{2} \tag{6.13}$$

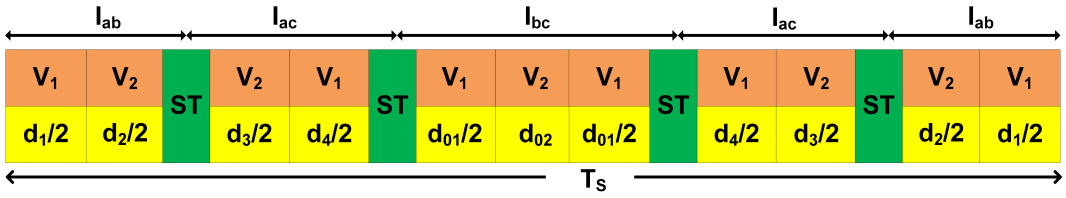


Figure 6.7: Switching sequence of the SB-USMC for complete cycle (T_S)

From equations (5.3) and (6.13), both methods produce the same average DC-link voltage V_{pq}. The boosting operation of the TVSVM is the same as the conventional SVM. The overall boosting factor (B) is given in equation (6.14), which is the same as equation (5.8).

$$B = \frac{\sqrt{3}m}{2}\frac{1}{1-2d_{st}}, \quad d_{st} = \frac{2B-\sqrt{3}m}{2B}, \quad \hat{V}_o = B\hat{V}_m \tag{6.14}$$

6.3.1 Calculation of CMV for the proposed TVSVM-II

Consider both reference vectors are in sector 1 and switching state $I_{ab}V_2(ppn)$ is applied. In this switching state $I_{ab}V_2(ppn)$, switches S_1, S_2, g_1, g_2, and g_3 are switching ON, as shown in Figure 6.2. The output voltages and the CMV are

$$\begin{aligned} v_{An} &= v_b + V_{p'q'} \quad v_{Bn} = v_b + V_{p'q'} \quad v_{Cn} = v_b \\ v_{CMV} &= v_b + \frac{2V_{p'q'}}{3} \end{aligned} \tag{6.15}$$

From Figure 6.8, in sector 1 v_b varies from $-\frac{1}{2}\hat{V}_m$ to $\frac{1}{2}\hat{V}_m$. So the maximum CMV in $I_{ab}V_2(ppn)$ switching states is

$$v_{CMV(max')} = \frac{1}{2}\hat{V}_m + \frac{2V_{p'q'}}{3} \tag{6.16}$$

Similarly, CMV for the remaining switching states is given in Table 6.3, in which Vector 1, Vector 2, and Vector 3 are three active vectors of the CSR in any sector. For example, in sector 1 of the CSR state I_{ab} is Vector 1, I_{ac} is Vector 2, and I_{bc} is Vector 3. The maximum CMV presented in the converter is

$$v_{CMV(max')} = \frac{\hat{V}_m}{2} + \frac{2V_{p'q'}}{3} \tag{6.17}$$

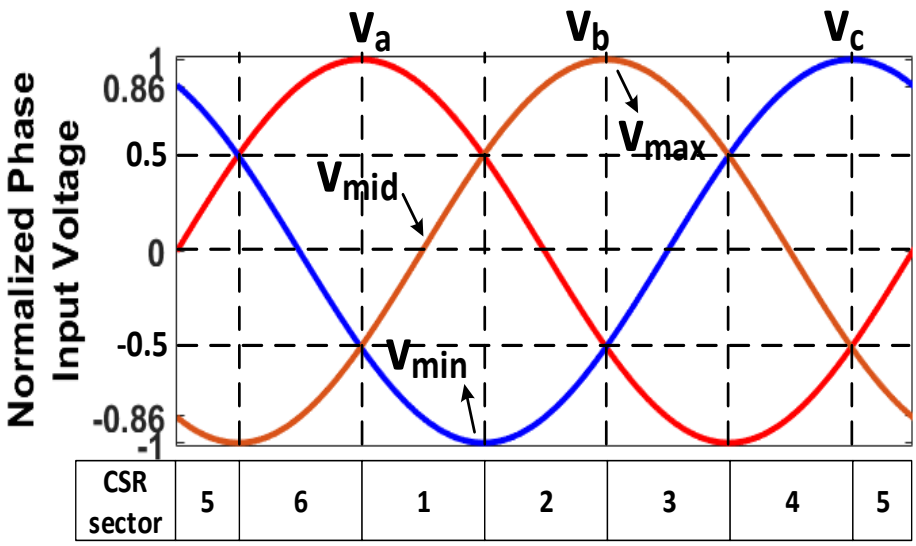


Figure 6.8: Input voltage variation through CSR sectors

In the proposed SB-USMC converter,

$$\begin{aligned} V_{pq} &= \frac{3}{2}V_m \\ v_{p'q'} &= \frac{1}{1-2d_{st}}v_{pq} \\ v_{p'q'} &= \frac{1}{1-2d_{st}}\frac{3}{2}V_m \end{aligned} \tag{6.18}$$

Here, V_{pq} is the DC-link voltage, and d_{st} is the shoot-through duty ratio. From equations (6.17) and (6.18), the peak CMV is

$$v_{CMV(max')} = (1 - \frac{2d_{st}}{3})V_{p'q'} \tag{6.19}$$

Percentage reduction of CMV by using modified SVM

$$\begin{aligned} \%CMV_{reduced} &= \frac{v_{CMVmax} - v_{CMV(max')}}{v_{CMVmax}} \\ &= \frac{2d_{st}}{3} \times 100\% \end{aligned} \tag{6.20}$$

For $d_{st} = 0.3$, the Percentage reduction of CMV by using TVSVM is 20%.

6.4 Simulation results for TVSVM-II

MATLAB is used to validate the proposed converter with 100 V/ph, 50 Hz input, and the remaining parameters are listed in Table 6.4. DC-link voltage (V_{pq}) is pulsed in nature with a frequency six times the supply frequency, as shown in Figure 6.9. The

Table 6.3: CMV for CSR and VSI switching states (TVSVM)

CSR sector	CSR states	VSI states	CMV	peak of the CMV
(1,3,5)	Vector 1	V_1, V_3, V_5	$\frac{3v_{mid}+V_{p'q'}}{3}$	$\frac{\hat{V}_m}{2}+\frac{V_{p'q'}}{3}$
		V_2, V_4, V_6	$\frac{3v_{mid}+2V_{p'q'}}{3}$	$\frac{\hat{V}_m}{2}+\frac{2V_{p'q'}}{3}$
		ST	v_{mid}	$\frac{-\hat{V}_m}{2}$
	Vector 2, Vector 3	V_1, V_3, V_5	$\frac{3v_{min}+V_{p'q'}}{3}$	$-\frac{\hat{V}_m}{2}+\frac{V_{p'q'}}{3}$
		V_2, V_4, V_6	$\frac{3v_{min}+2V_{p'q'}}{3}$	$-\frac{\hat{V}_m}{2}+\frac{2V_{p'q'}}{3}$
		ST	v_{min}	$-v_{min}$
2, 4, 6	Vectors 1,2	V_1, V_3, V_5	$\frac{3v_{min}+V_{p'q'}}{3}$	$\frac{-\hat{V}_m}{2}+\frac{V_{p'q'}}{3}$
		V_2, V_4, V_6	$\frac{3V_{min}+V_{p'q'}}{3}$	$-\frac{\hat{V}_m}{2}+\frac{2V_{p'q'}}{3}$
		ST	v_{min}	$-\hat{V}_m$
	Vector 3	V_1, V_3, V_5	$\frac{3v_{mid}+2V_{p'q'}}{3}$	$\frac{\hat{V}_m}{2}+\frac{V_{p'q'}}{3}$
		V_2, V_4, V_6	$v_{min}+V_{p'q'}$	$\frac{-\hat{V}_m}{2}+\frac{2V_{p'q'}}{3}$
		ST	v_{min}	$\frac{-\hat{V}_m}{2}$

Table 6.4: Simulation parameters

S. no	***Simulation parameter***	***Value***
1	supply voltage	100 V
2	input frequency	50 Hz
3	d_{st}	0.3
4	Output power	1.5 kW
5	SN capacitor (C)	120 uF
6	SN Inductor (L)	2.5 mH
7	Output frequency	50 Hz
8	Switching frequency	5 kHz

average value of (V_{pq}) is 149 V. This (V_{pq}) is input to the switched network. The nature of the inductor current and diode voltages in both ST and NST modes are shown in Figure 6.10. In ST mode, the voltage across the switch is 0 V, and the shorting of the VSI leg causes the boosted voltage to reach zero. The inductor current gets increased

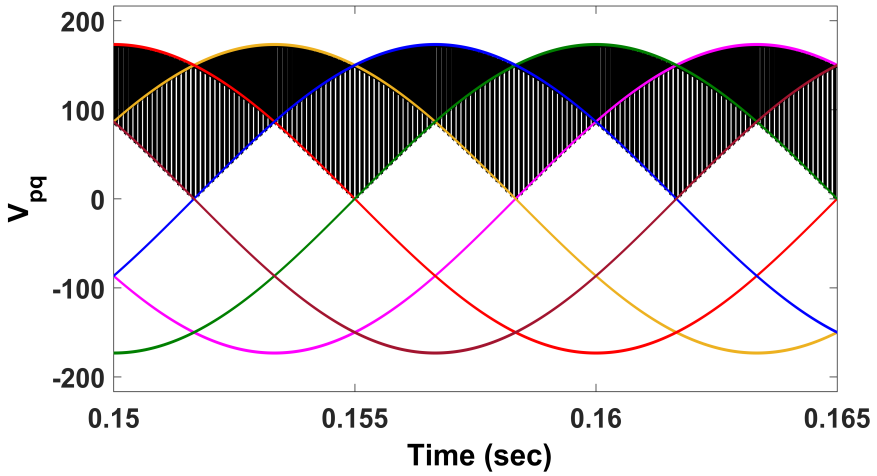


Figure 6.9: Three phase supply and DC-link voltage (V_{pq})

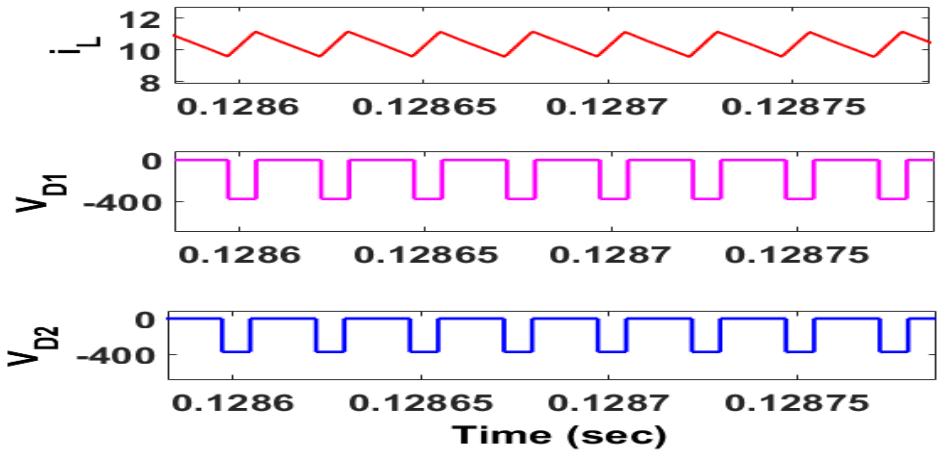


Figure 6.10: Behaviour of inductor current, diodes voltages

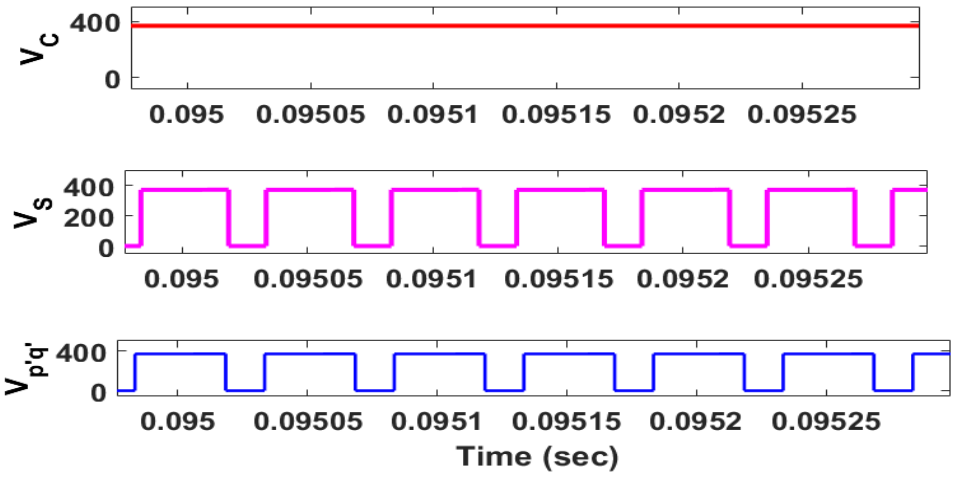


Figure 6.11: Capacitor voltage, SN switch voltage, and boosted output voltage

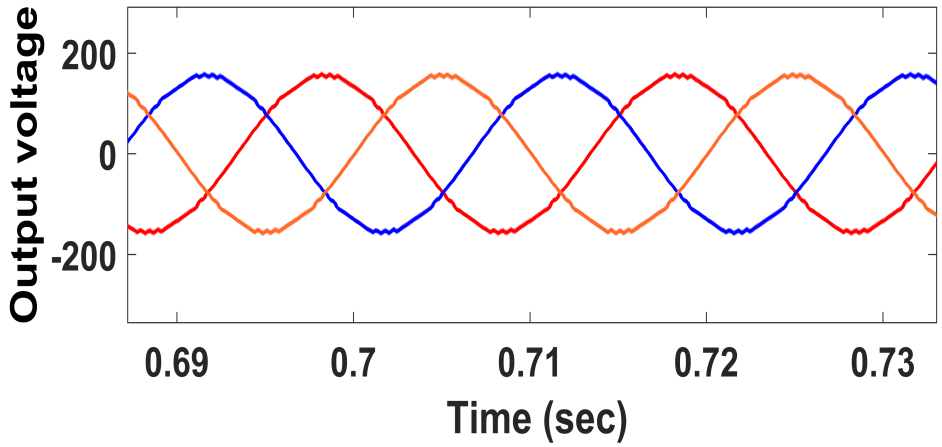


Figure 6.12: Three phase output voltages of the proposed converter

and reaches a maximum value of 12.2 A. Both diodes show a voltage stress of 372 V. The capacitor voltage, voltage stress across the switch S, and switched network output voltages ($V_{p'q'}$) are shown in Figure 6.11. In NST mode, the capacitor is parallel to the impedance network output terminals; hence, the voltage of the boosted terminal is constant at 372 V. In this mode, the inductor current falls in nature. Switch S is OFF and ($V_{p'q'}$) attains 372 V. This voltage drives the VSI. For ($m = 0.7$), the output

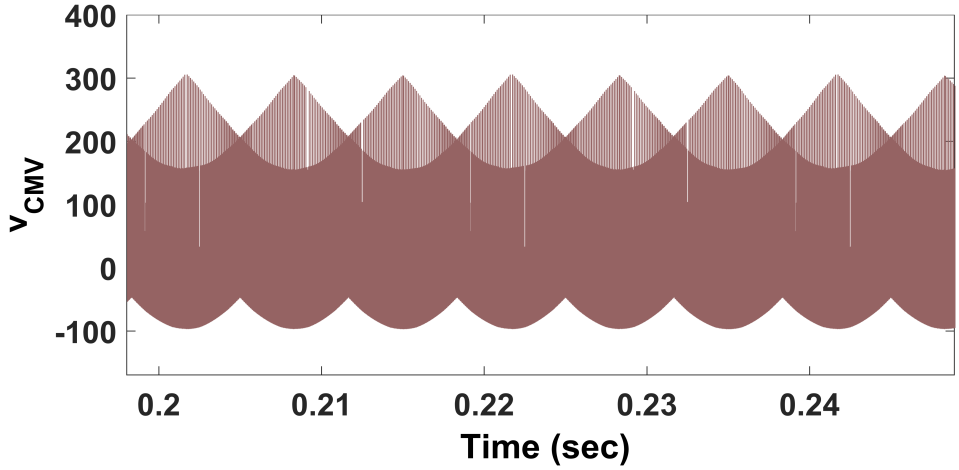


Figure 6.13: Behaviour of the CMV

voltage is 150 V, shown in Figure 6.12. Figure 6.13 shows that CMV profile varies from -100 V ($-\hat{V}_m$) to 300 V ($\frac{\hat{V}_m}{2} + \frac{2V_{p'q'}}{3}$). The switching strategy reported in the previous chapter produces the maximum peak CMV of $V_{p'q'}$ (375 V). The proposed switching scheme gives a 20% lower peak CMV than these methods.

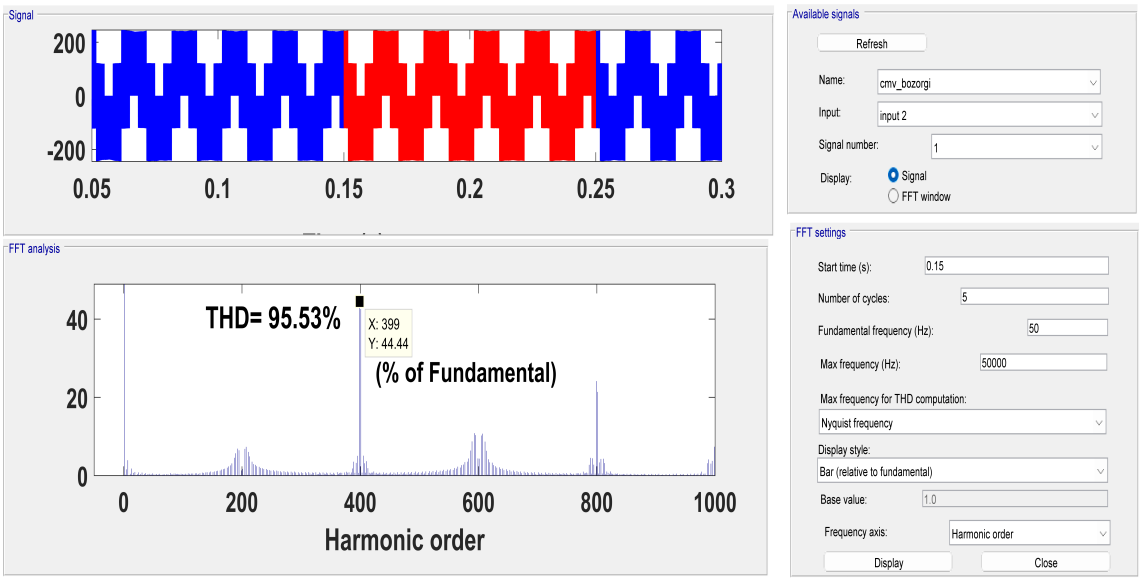


Figure 6.14: FFT analysis on output voltage (50 Hz) of the TVSVM-I

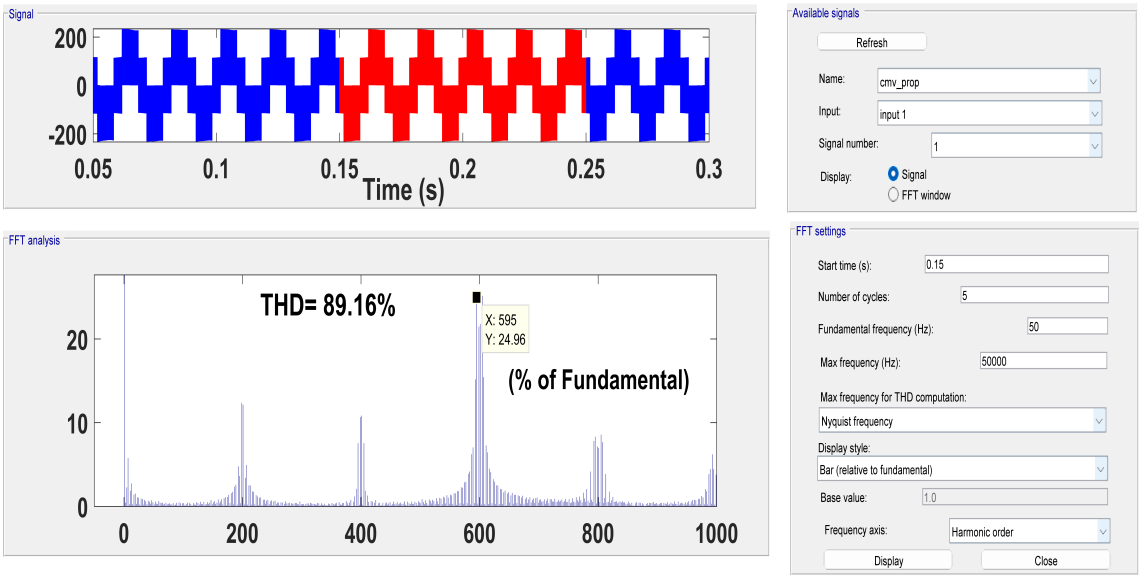


Figure 6.15: FFT analysis on output voltage (50 Hz) of the TVSVM-II

6.5 FFT analysis on TVSVM-I and TVSVM-II

FFT analysis is performed for both methods with the parameters listed in Table 6.4. In TVSVM-I, the dominated harmonics are around 400 for 50 Hz output frequency, as shown in Fig. 6.14. For the TVSVM-II method, dominated harmonics are 600 for 50 Hz, as shown in Fig. 6.15. The TVSVM-II method shows better THD (89.16%) than the TVSVM-I method (95.53%) in both figures. Further, the duty ratio varies from 0.2 to 0.4, and the corresponding THD is observed, as shown in Fig. 6.16. The TVSVM-II

method always shows better THD than the TVSVM-I method for this duty range. Fig. 6.17 shows the % CMV reduction comparison between TVSVM-I and TVSVM-II methods.

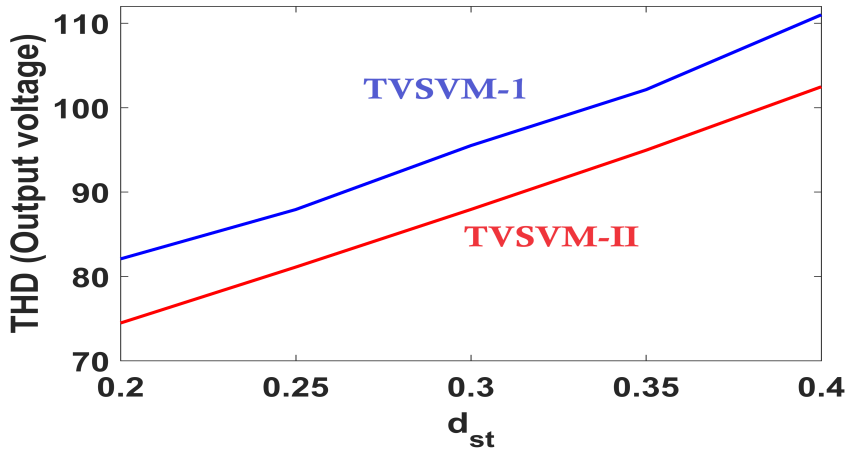


Figure 6.16: Output voltage THD comparison between TVSVM-I and TVSVM-II

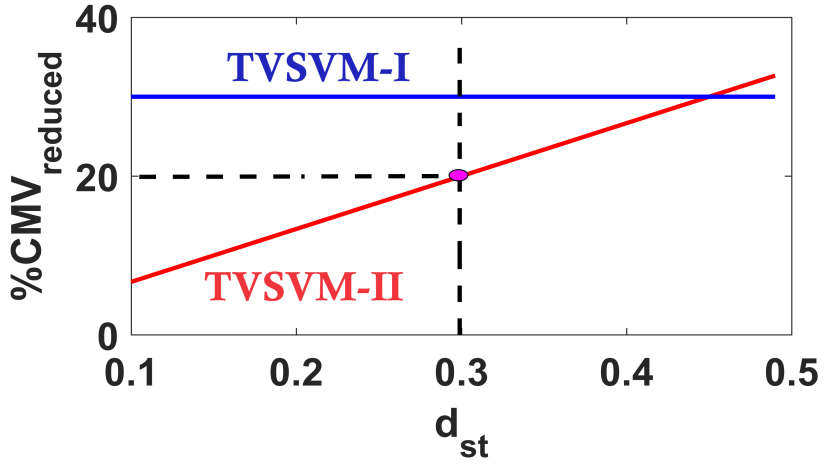


Figure 6.17: % CMV reduction comparison between TVSVM-I and TVSVM-II

6.6 Experimental results for TVSVM-II

The proposed converter is also validated through an experimental prototype. This experiment has been conducted with the input phase supply $\hat{V}_{an} = 50$ V, 50 Hz at 250 W output power. The remaining parameters are the same as the simulation parameters. By supplying this input to the CSR, a rectified output voltage with an average value of 74 V is obtained. The obtained voltage is pulsating in nature with a frequency six times

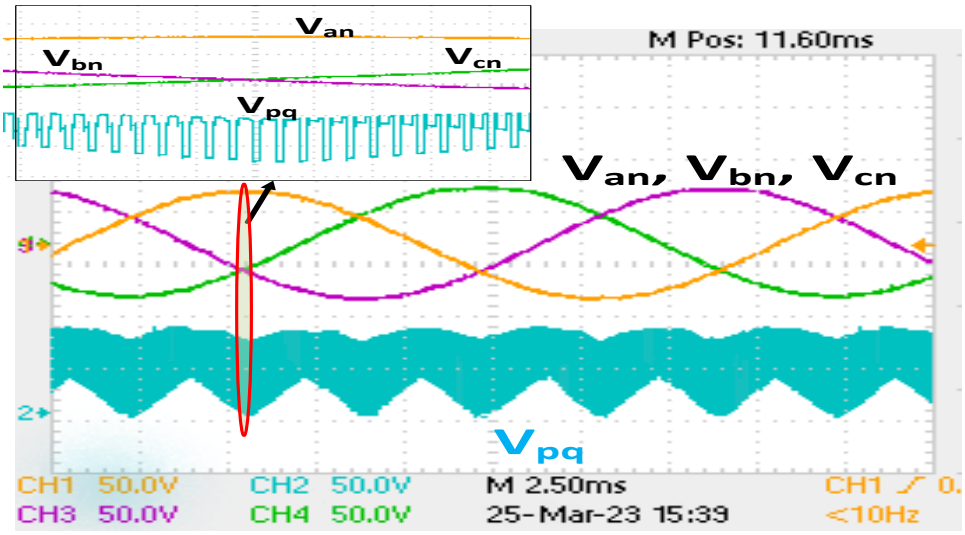


Figure 6.18: Input supply and CSR output voltage

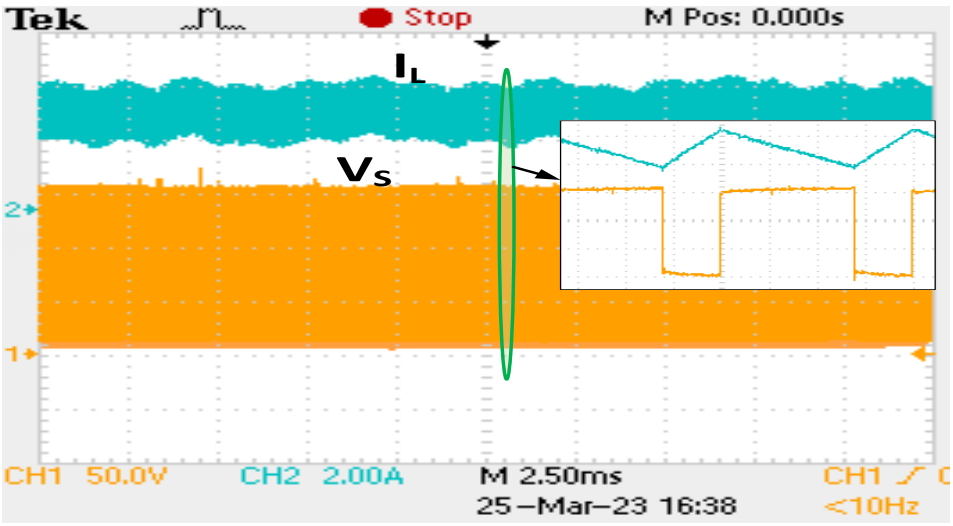


Figure 6.19: Switch voltage and current through inductor

the input frequency. The nature of the rectified output voltage is shown in Figure 6.18. Applying shoot-through duty ratio and modulation index are 0.3 and 0.7, respectively. Voltage stress across the impedance network switch is depicted in Figure 6.19. During the NST mode, the switch attained 185 V; during ST mode, the switch is in conduction. From the exact Figure 6.19, during ST mode, the inductor current rises and reaches 4.2 A. During NST mode, the inductor current falls and attains 2.8 A. Figure 6.20 shows the proposed converter able to boost the input voltage from 50 V to 74 V, 50 Hz. From Figs. 6.18 and 6.20, it is observed that the output voltage is more than (1.5 times) the input supply. Hence, voltage gain greater than unity is achieved.

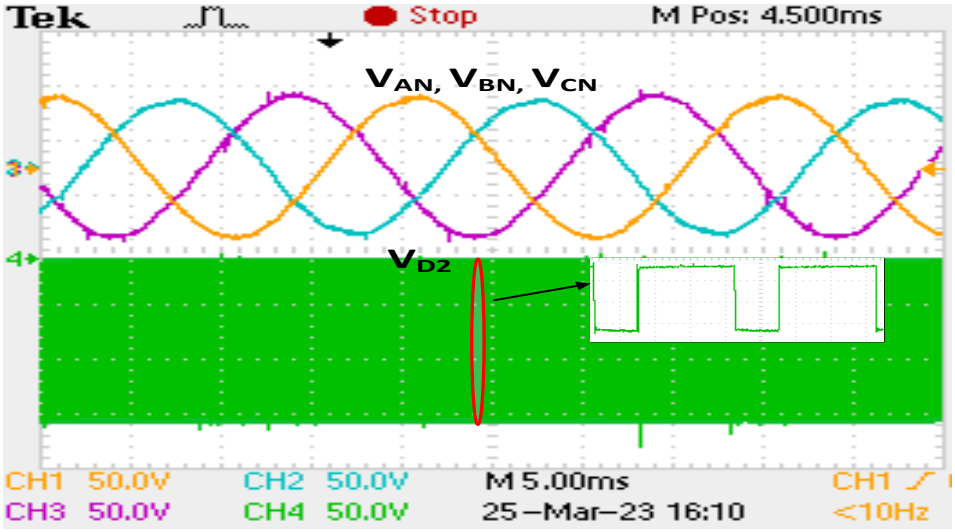


Figure 6.20: SB-USMC output voltage and voltage stress across D_2

6.7 Summary

This chapter provides a solution to minimize the common mode voltage in switched boost ultra sparse matrix converters. TVSVM-I and TVSVM-II methods successfully reduced the peak CMV in the SB-USMC. TVSVM-I reduces peak CMV by 33%. At the same time, the reduction of peak CMV depends on the duty shoot-through period in TVSVM-II. TVSVM-II reduces the peak CMV by 20% for the duty shoot-through period of 0.3. TVSVM-II showed better THD performance than the TVSVM-I method.