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Dedicated
to
My Family and VLPERI

Content

Abstract

Renewable energy sources, particularly solar photovoltaic (PV) systems, have emerged as a prominent solution to address the current power crisis and pressing environmental concerns. In recent years, there has been a substantial increase in the installation capacity of solar PV systems worldwide. However, the power generated from solar PV systems is non-linear and depends on unpredictable environmental and shading conditions. So, a reliable and efficient power converter integrated with maximum power point tracking (MPPT) control is needed to harness and utilize solar power effectively. Photovoltaic (PV) systems employ silicon-based cells to convert solar energy into electrical energy. When the solar irradiance falling on the solar panel is uniform, a power-voltage curve (PV curve) with a single peak is observed. In contrast, a multi-peak PV curve is observed when there is any obstruction in the path of sunlight or when panels are shaded. Using conventional maximum power point tracking (MPPT) algorithms like perturb and observe (P&O) and incremental conductance (INC), maximum power can be harnessed. However, the conventional algorithm faces difficulty under a multi-peak PV curve and fails to harness the power at the global maxima point. A heuristic algorithm is required to harness maximum under multi-peak PV curves. Since solar power is of a DC nature, a DC-DC or DC-AC power converter can be employed for the power interface. The isolated class DC-DC converter can be preferred over the non-isolated one for DC-DC converters when high voltage application, safety, and compliance are top priorities. The galvanic isolation of the isolated DC-DC converter ensures safe and leakage-free operation for two-stage DC-AC topologies. The high-frequency operation of the isolated DC-DC converter reduces the volume and size of the converter concurrently, increasing the switching losses of the converter. Some isolated DC-DC converters, like a dual active bridge, use their transformer leakage inductance to achieve zero voltage switching operation. However, they suffer from light load efficiencies. Resonant tanks can reduce switching losses by releasing the energy stored within the switching devices. A resonant tank can be employed in series, parallel, or series-parallel combinations. However, they pose various design complexities and constraints. These isolated resonant converters can be further categorized as load resonant converters and quasi-resonant converters based on utilizing the switching cycle. These isolated converters often use switching schemes with complementary gating signals that require a small dead-band time between them to avoid the short circuit between the power rails. The dead-band time needed for these converters can be optimized to enhance soft-switching while affecting the tank

elements. In power converters, electrolytic capacitors are often utilized as voltage-smoothening filters to stabilize the DC voltage despite their vulnerable and unreliable operation. These electrolytic capacitors suffer from the aging effect; as their electrolytes evaporate with time, their capacitance decreases, and equivalent series resistance increases with time. If these electrolytic capacitors are employed for voltage smoothening in solar PV converters, they may need to be replaced several times over a single solar panel life span. Besides this, continuous health monitoring is also required to track their physical degradation to avoid future consequences. The film capacitor can be a better alternative for low to medium-power applications as it doesn't age with time and has no physical limitations, making it more suitable for solar PV applications. Besides this, the rms current rating per unit capacitance of the film capacitor can be twenty to fifty times higher than that of the electrolytic capacitors. To address the vulnerability of the electrolytic capacitors, some electrolytic capacitor-less isolated two-stage topologies have been given. However, the voltage at the DC link is pulsating, requiring a novel modulation scheme to operate the inverter. Due to the pulsating voltage at the DC link, energy storage systems can't be integrated at the DC link. Also, these topologies have not been tested for solar PV integration.

To resolve the issue associated with the use of electrolytic capacitors, electrolytic capacitor-less isolated DC-DC converters, dual half-active bridge resonant converters (DHABRC) for low power application, and asymmetrical dual half-active bridge resonant converters (ADABRC) for low to medium-power applications have been proposed. The proposed converters utilize film capacitors for voltage smoothening for better reliability. The proposed converters have been analyzed and designed using the fundamental harmonics approximation. The sufficient and necessary conditions for soft-switching have been derived to optimize the dead band time required to operate the proposed converter. An optimized LLC resonant tank has improved the converter's efficiency. The film capacitor of the *LLC* tank blocks the DC current, preventing DC voltage imbalances, particularly those arising from output-side film capacitors, from saturating the high-frequency transformer. The efficacy of the FHA technique has been verified by comparing the theoretical data obtained from the analysis with simulation and experimental results. A hardware setup of 500W is developed and tested for steady-state and soft-switching conditions. From the experimental results, the zero-voltage switching operation of all the active switches has been verified. The feasibility of using film capacitors has also been verified by measuring the voltage under startup transient, load dynamics, and steady-state conditions.

The proposed converter is further integrated with solar PV. For this, a solar PV emulator ((Chroma 62100H-600S) has been used, and multiple PV curves of different power ratings are generated for uniform and non-uniform irradiance conditions (partial shading conditions). The simulation and experimental tests have been performed for the 500 W converter. The maximum power at the global maxima point has been drawn using particle swarm optimization and grey wolf optimization. The heuristic algorithm offers many advantages, such as tracking global peak power under PSC, adaptability to dynamic conditions, fewer oscillations, less sensitivity to noise, less mathematical complexities, and a direct control approach, causing the elimination of the control loops. The steady-state oscillations in voltage and current waveforms are also negligible around the steady-state conditions.

Next, the proposed converter is connected to a three-phase voltage source inverter (VSI) to feed the power to the resistive load and AC grid, forming a pseudo-DC link-based isolated two topology. In the two-stage topology, the need for the DC link capacitor is eliminated, and the outer film capacitor leg of the isolated DC-DC converter is utilized to act like a DC link. The inverter output is synchronized to the grid's characteristics using a synchronous reference frame-based phase-locked loop. The control loop designed for the topology ensures the quality of the grid current with over-current protection. The voltage control loop provides the stable DC link voltage while balancing the power flow at the DC link. The PI controller of the inner current control loop is tuned using the modulus optimum tuning criterion. The PI controller of the outer voltage control loop is tuned using the symmetrical optimum tuning criterion. The proposed two-stage is first tested for resistive load and then tested to feed the power to the three-phase AC grid. The proposed pseudo-DC link-based two-stage topology easily transfers the solar power to the AC grid.

The low voltage output generated from solar PV needs to be stepped up to the utility/microgrid voltage level for efficient utilization. An impedance network is added at the input side of the electrolytic capacitor-less isolated DC-DC converters. The impedance network accommodates a wide range of input PV voltage while ensuring a regulated DC output. This is achieved by dynamically adjusting the duty cycle. Furthermore, the impedance network enhances system resilience by mitigating the risk of shoot-through faults and short circuits that may occur due to misfiring events, thereby improving the system's immunity to electromagnetic interference (EMI). The utilized impedance network exhibits an expandable architecture. With each additional stage added to the network, the overall voltage gain of the system increases. Thus, an expandable input impedance-sourced isolated resonant converter

(EIISIRC) with electrolytic capacitor-less properties is formed. For the proposed EIISIRC, a hardware prototype of 500 W is built, which is later tested for steady-state and partial-shaded conditions.

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(Prakash Ji Barnawal)

List of Figures

List of Tables

List of Acronyms

PV	Photovoltaic
MPPT	Maximum power point tracking
P&O	Perturb and observe
INC	Incremental Conductance
DHABRC	Dual half active bridge resonant converter
ADABRC	Asymmetrical dual half-active bridge resonant converters
UIC	Uniform irradiance conditions
PSC	Partial shading conditions
VSI	Voltage source inverter
EMI	Electromagnetic interference
EIISIRC	Expandable input impedance-sourced isolated resonant converter
DC	Direct current
EV	Electric vehicle
ZVS	Zero voltage switching
ZCS	Zero current switching
DAB	Dual active bridge
PSM	Phase-shift modulation
SRC	Series resonant converter
PRC	Parallel resonant converter
SPRC	Series-parallel resonant converter
qZSI	Quasi-Z-source Inverter
EC	Electrolytic capacitor

FC	Film capacitor
PSO	Particle swarm optimization
GWO	Grey wolf optimization
SRF	Synchronous reference frame
PLL	Phase locked loop
HFT	High-frequency transformer
FHA	Fundamental harmonics approximation
GP	Global peak
LP	Local peak
SP	Shading pattern
OLTF	Open loop transfer function
CLTF	Closed loop transfer function
GM	Gain margin
PM	Phase margin
SPWM	Sinusoidal pulse width modulation
ADC	Analog to digital conversion
MOTC	Modulus optimum tuning criterion
SOTC	Symmetrical optimum tuning criterion
THD	Total harmonics distortion
EIIS	Expandable input impedance source
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
GMP	Global maxima point
LMP	Local maxima point

Symbols Used

V_{in}, V_{PV}	DC Input voltage
I_{in}, I_{PV}	Input current
P_{PV}	Input PV power
V_o	Output voltage
I_o	Output current
P_o	Output power
C_1-C_4	Film capacitors
V_{C1}-V_{C4}	Voltage across film capacitors
L_r	Resonant inductance
C_r	Resonant capacitor
K	Inductance ratio
V_{Cr}	Voltage across resonant capacitor
L_m	Parallel inductance
S_1-S_4	Active switches
D_1-D_4	Body diode of active switches
n_t	Turns ratio
V_{AB}	Primary bridge voltage
i_r	Primary bridge current
V_{CD}	Secondary bridge voltage
i_s	Secondary bridge current
ϕ	Phase angle
F_s	Switching frequency of DC-DC converter
I_{S1}-I_{S4}	Switch current

V_{GS1} - V_{GS4}	Gating signals for DC-DC converter
f_r	Resonant frequency
V_B	Base voltage
Z_B	Base impedance
ω_B	Base frequency
M, λ	Voltage gain
F	Normalized switching frequency
Q	Quality factor
Z_{ac}	AC impedance
α	Lagging angle of primary bridge current
β	Leading angle of secondary bridge current
C_{S1}-C_{S4}	Parasitic capacitance of active switches
T_{D_P}	Dead time primary switch
T_{D_S}	Dead time secondary switch
K	Iteration number
x_i	Position vector
v_i	Velocity vector
P_b	Personal best
G_b	Global best
w	Inertia coefficient
c_1 - c_2	Cognitive and social weighting factor
r_1 - r_2	Random number
α_g	Alpha wolves
β_g	Beta wolves

ω_g	Omega wolves
δ_g	Delta wolves
X_p, X	Position vector
A, C_g	Coefficient vector
V_{DC}	DC link voltage
i_a, i_b, i_c	Phase currents of grid
E_a, E_b, E_c	Grid line voltages
v_a, v_b, v_c	Grid phase voltages
f_g	Grid frequency
L_f and C_f	Filtering capacitor
TF	Transfer function
G_P	Plant transfer function of PLL
G_{P1}	OLTF of PLL with PI controller
G_{P2}	OLTF of PLL with K-factor controller
K_{pi}	Proportional gain for inner current control loop
K_{ii}	Integral gain for inner current control loop
T_i	Integral time constant for inner current control loop
K_{po}	Proportional gain for outer voltage control loop
K_{io}	Integral gain for outer voltage control loop
T_o	Integral time constant for outer voltage control loop
G_I	OLTF of current control loop
G_{Il}	OLTF of current control loop with PI controller
G_{CLI}	CLTF of current control loop
G_V	OLTF of voltage control loop plant

G_{V1}	OLTF of voltage control loop with PI controller
D	Duty
$C_a - C_d$	Film Capacitor
L_1, L_2, L_3	Inductors
V_{Do}, V_{D1}, V_{D2}	Voltage across the diodes